

FAIRCHILD SEMICONDUCTOR

MADE IN
FAIRCHILD

THE LINEAR INTEGRATED CIRCUITS DATA CATALOG

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FEBRUARY 1973

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CONTENTS AND SECTION SELECTOR

INTRODUCTION 1

NUMERICAL INDEX 2

OPERATIONAL AMPLIFIERS 3

COMPARATORS 4

VOLTAGE REGULATORS 5

COMPUTER/INTERFACE 6

CONSUMER 7

TRANSISTOR/DIODE ARRAYS/ANALOG SWITCHES 8

PACKAGE OUTLINES 9

ORDER INFORMATION 10

MIL-M-38510/MIL-STD-883 11

DICE 12

INDUSTRY CROSS REFERENCE GUIDE 13

APPLICATION INFORMATION 14

Each Product
Section Contains The
Following Categories
Organized By Function
Index
Selection Guide
Data Sheets
Glossary

LINEAR LINEAR LINEAR LINEAR

The Linear Integrated Circuits Data Catalog

Since its founding in 1957, Fairchild has grown from the original group of eight scientist/engineers to a world-wide industry leader. Large modern plants in Mountain View and San Rafael, California; Shiprock, New Mexico; and South Portland, Maine are complemented by off-shore facilities in Australia, Germany, Hong Kong, Korea, Mexico and Singapore.

Total Linear Capability is a reality at Fairchild Analog Products. Fairchild is the largest and most experienced manufacturer of linear devices in the world and takes pride in its ability to design and mass produce linear products which meet the needs of a large and diverse industry. Over the years, Fairchild's unique combination of design talent and production expertise has resulted in the most comprehensive line of linear microcircuits ever assembled.

This advanced line of products is backed by years of production experience — experience which enables Fairchild to maintain the position of leadership it has enjoyed since the delivery of the first order for μ A709 operational amplifiers in the early 1960s.

The tremendous possibilities inherent in silicon Planar* technology are still not exhausted and forward-thinking research continues at Fairchild. This type of research made possible the industry's first linear integrated circuit, the first consumer-oriented linear device, the first "universal" operational amplifier, and the first monolithic voltage regulator.

Fairchild's advanced technological capability and vast production experience combined make possible the most advanced, most reliable, and lowest cost line of linear integrated circuits in the industry today. The fact that the name "Fairchild" has always been synonymous with quality, reliability, and leadership is no mere coincidence, and the fact that Fairchild will remain in this position is not just a promise, but a pledge to Total Linear Capability.

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Mountain View, California 94040

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*Planar is a patented Fairchild process.

LINEAR LINEAR LINEAR LINEAR

CONTENTS AND SECTION SELECTOR

NUMERICAL INDEX	2
OPERATIONAL AMPLIFIERS	3
COMPARATORS	4
VOLTAGE REGULATORS	5
COMPUTER/INTERFACE	6
CONSUMER	7
TRANSISTOR/DIODE ARRAYS/ANALOG SWITCHES	8
PACKAGE OUTLINES	9
ORDER INFORMATION	10
MIL-M-38510/MIL-STD-883	11
DICE	12
INDUSTRY CROSS REFERENCE GUIDE	13
APPLICATION INFORMATION	14

DEVICES	DESCRIPTION	PAGE
μ A702	Wideband DC Amplifier	3-9
μ A703	RF-IF Amplifier	7-9
μ A704	Television Sound System	7-96
μ A705	Dual Channel Power Audio Amplifier	7-96
μ A706	5 Watt Audio Amplifier	7-11
μ A709	High Performance Operational Amplifier	3-16
μ A710	High Speed Differential Comparator	4-5
μ A711	Dual Comparator	4-9
μ A715	High Speed Operational Amplifier	3-23
μ A720	AM Radio System	7-16
μ A722	10-Bit Current Source	6-9
μ A723	Precision Voltage Regulator	5-7
μ A725	Instrumentation Operational Amplifier	3-30
μ A726	Temperature-Controlled Differential Pair	8-3
μ A727	Temperature-Controlled Differential Preamplifier	3-39
μ A728	Precision Voltage Reference	5-44
μ A730	Differential Amplifier	3-43
μ A732	FM Stereo Multiplex Decoder	7-21
μ A733	Differential Video Amplifier	6-12
μ A734	Precision Voltage Comparator	4-13
μ A739	Dual Low Noise Audio Preamplifier	7-24
μ A740	FET Input Operational Amplifier	3-49
μ A741	Frequency Compensated Operational Amplifier	3-53
μ A741A	Frequency Compensated Operational Amplifier	3-60
μ A741E	Frequency Compensated Operational Amplifier	3-60
μ A742	Zero Crossing AC Trigger-Trigac	7-28
μ A746	Chroma Demodulator	7-32
μ A747	Dual Frequency Compensated Operational Amplifier	3-65
μ A747A	Dual Frequency Compensated Operational Amplifier	3-72
μ A747E	Dual Frequency Compensated Operational Amplifier	3-72
μ A748	High Performance Operational Amplifier	3-77
μ A749	Dual Audio Preamplifier	7-36
μ A750	Dual Comparator Subsystem	4-20
μ A753	FM Gain Block	7-44
μ A757	Gain Controlled IF Amplifier	7-47
μ A758	Phase Locked Loop FM Stereo Multiplex Decoder	7-53
μ A760	High Speed Differential Comparator	4-24
μ A767	FM Stereo Multiplex Decoder	7-57
μ A768	FM Stereo Multiplex Decoder	7-21
μ A769	FM Stereo Multiplex Decoder	7-57
μ A771	Instrumentation Amplifier	3-138
μ A772	High Slew Rate Operational Amplifier	3-138
μ A776	Multi-Purpose Programmable Operational Amplifier	3-84
μ A777	Precision Operational Amplifier	3-93

DEVICE	DESCRIPTION	PAGE
μ A780	Chroma Subcarrier Regenerator (Phase Locked Loop)	7-60
μ A781	Gain Controlled IF Amplifier	7-66
μ A786	PAL TV Chroma Demodulator	7-71
μ A791	Power Operational Amplifier	3-100
μ A796	Double-Balanced Modulator/Demodulator	7-74
μ A7350	Tachometer Subsystem	7-97
μ A7351	Triple Operational Amplifier	7-97
μ A7805	Three Terminal Positive Voltage Regulator	5-14
μ A7806	Three Terminal Positive Voltage Regulator	5-14
μ A7808	Three Terminal Positive Voltage Regulator	5-14
μ A7812	Three Terminal Positive Voltage Regulator	5-14
μ A7815	Three Terminal Positive Voltage Regulator	5-14
μ A7818	Three Terminal Positive Voltage Regulator	5-14
μ A7824	Three Terminal Positive Voltage Regulator	5-14
μ A78M05	Three Terminal Positive Voltage Regulator	5-45
μ A78M06	Three Terminal Positive Voltage Regulator	5-45
μ A78M08	Three Terminal Positive Voltage Regulator	5-45
μ A78M12	Three Terminal Positive Voltage Regulator	5-45
μ A78M15	Three Terminal Positive Voltage Regulator	5-45
μ A78M20	Three Terminal Positive Voltage Regulator	5-45
μ A78M24	Three Terminal Positive Voltage Regulator	5-45
μ A78N00	Three Terminal Negative Voltage Regulators	5-51
μ A78T00	Tracking Voltage Regulators	5-44
SH0013	Two-Phase MOS Clock Driver	6-126
SH2001	High Voltage, High Current Driver	6-131
SH2002	DTL High Power Driver	6-135
SH2200	High Voltage, High Current Driver	6-139
SH3002	SPDT Analog Switch	8-22
SH8090	10-Bit D/A Converter	6-143
TBA510	Chroma Processing Circuit	7-98
TBA920	Horizontal Oscillator, Phase Comparator and Sync Separator	7-99
TBA970	Television Video Amplifier	7-99
8T13	Dual Single-Ended Line Driver	6-114
8T14	Triple Line Receiver	6-117
8T23	Dual Single-Ended Line Driver	6-120
8T24	Triple Line Receiver	6-123
101	General Purpose Operational Amplifier	3-106
101A	General Purpose Operational Amplifier	3-109
102	Voltage Follower	3-127
104	Negative Voltage Regulator	5-25
105	Voltage Regulator	5-30
107	General Purpose Operational Amplifier	3-116
108	Super Beta Operational Amplifier	3-121
108A	Super Beta Operational Amplifier	3-121

DEVICE	DESCRIPTION	PAGE
109	Five Volt Regulator	5-36
110	Voltage Follower	3-127
111	Voltage Comparator	4-29
201	General Purpose Operational Amplifier	3-106
201A	General Purpose Operational Amplifier	3-109
207	General Purpose Operational Amplifier	3-116
208	Super Beta Operational Amplifier	3-121
208A	Super Beta Operational Amplifier	3-121
209	Five Volt Regulator	5-36
301A	General Purpose Operational Amplifier	3-109
302	Voltage Follower	3-127
304	Negative Voltage Regulator	5-25
305	Voltage Regulator	5-30
305A	Voltage Regulator	5-30
307	General Purpose Operational Amplifier	3-116
308	Super Beta Operational Amplifier	3-121
308A	Super Beta Operational Amplifier	3-121
309	Five Volt Regulator	3-36
310	Voltage Follower	3-127
311	Voltage Comparator	4-29
376	Voltage Regulator	5-30
1326	Chroma Demodulator	7-100
1458	Internally Compensated, High Performance Dual Monolithic Operational Amplifier	3-132
1458C	Internally Compensated, High Performance Dual Monolithic Operational Amplifier	3-132
1558	Internally Compensated, High Performance Dual Monolithic Operational Amplifier	3-132
2136	FM IF Amplifier & Detector	7-101
3018	Transistor Array	8-6
3018A	Transistor Array	8-6
3019	Diode Array	8-6
3026	Transistor Array	8-6
3036	Transistor Array	8-6
3039	Diode Array	8-6
3045	Transistor Array	8-6
3046	Transistor Array	8-6
3054	Transistor Array	8-6
3064	TV Automatic Fine Tuning Circuit	7-78
3065	TV Sound System	7-82
3066	TV Chroma Processor	7-85
3067	Chroma Demodulator	7-89
3075	FM IF Amplifier-Limiter, Detector, Audio Preamplifier	7-92
3076	FM Gain Block	7-101
3086	Transistor Array	8-6

DEVICE	DESCRIPTION	PAGE
7524	Two Channel Core Memory Sense Amplifier	6-87
7525	Two Channel Core Memory Sense Amplifier	6-87
9307	Seven Segment Decoder	6-18
9317B	Seven Segment Decoder/Driver	6-19
9317C	Seven Segment Decoder/Driver	6-19
9368	Seven Segment Decoder/Driver/Latch	6-20
9369	Seven Segment Decoder/Driver/Latch	6-21
9370	Seven Segment Decoder/Driver/Latch	6-22
9614	Dual Differential Line Driver	6-23
9615	Dual Differential Line Receiver	6-27
9616	Triple EIA RS-232-C/MIL-STD-188C Line Driver	6-31
9617	Triple EIA RS-232-C Line Receiver	6-34
9620	Dual Differential Line Receiver	6-36
9621	Dual Line Driver	6-42
9622	Dual Line Receiver	6-48
9624	Dual TTL, MOS Interface Element	6-52
9625	Dual TTL, MOS Interface Element	6-52
9627	Dual EIA RS-232-C/MIL-STD-188C Line Receiver	6-57
9650	4-Bit Current Source	6-60
9660	Seven Segment Decoder/Programmable Current Driver	6-146
9661	Quad Programmable Current Segment Driver	6-146
9662	LED/Lamp Digit Driver	6-147
9663	LED/Lamp Digit Driver	6-147
55107A	Dual Line Receiver	6-69
55108A	Dual Line Receiver	6-69
55109	Dual Line Driver	6-75
55110	Dual Line Driver	6-75
55325	Memory Driver	6-79
75107A	Dual Line Receiver	6-69
75108A	Dual Line Receiver	6-69
75109	Dual Line Driver	6-75
75110	Dual Line Driver	6-75
75325	Memory Driver	6-79
75450A	5 V Dual Peripheral Driver	6-91
75451A	5 V Dual Peripheral Driver	6-91
75452	5 V Dual Peripheral Driver	6-91
75453	5 V Dual Peripheral Driver	6-91
75454	5 V Dual Peripheral Driver	6-91
75460A	5 V Dual Peripheral Driver	6-91
75461A	5 V Dual Peripheral Driver	6-91
75462A	5 V Dual Peripheral Driver	6-91
75463A	5 V Dual Peripheral Driver	6-91
75464A	5 V Dual Peripheral Driver	6-91
75491	MOS to LED Segment and Digit Driver	6-110
75492	MOS to LED Segment and Digit Driver	6-110

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product.
No other circuit patent licenses are implied.

LINEAR LINEAR LINEAR LINEAR LINEAR

CONTENTS AND SECTION SELECTOR

OPERATIONAL AMPLIFIERS	3
COMPARATORS	4
VOLTAGE REGULATORS	5
COMPUTER/INTERFACE	6
CONSUMER	7
TRANSISTOR/DIODE ARRAYS/ANALOG SWITCHES	8
PACKAGE OUTLINES	9
ORDER INFORMATION	10
MIL-M-38510/MIL-STD-883	11
DICE	12
INDUSTRY CROSS REFERENCE GUIDE	13
APPLICATION INFORMATION	14

INDEX

Selection Guide 3-4

DATA SHEETS

General Purpose

μ A702	Wideband DC Amplifier.....	3-9
μ A709	High Performance Operational Amplifier	3-16
μ A730	Differential Amplifier	3-43
μ A739	Dual Low Noise Audio Preamplifier	7-24
μ A741	Frequency Compensated Operational Amplifier	3-53
μ A741A	Frequency Compensated Operational Amplifier	3-60
μ A741E	Frequency Compensated Operational Amplifier	3-60
μ A747	Dual Frequency Compensated Operational Amplifier	3-65
μ A747A	Dual Frequency Compensated Operational Amplifier	3-72
μ A747E	Dual Frequency Compensated Operational Amplifier	3-72
μ A748	High Performance Operational Amplifier	3-77
μ A749	Dual Audio Preamplifier	7-36
μ A776	Multi-Purpose Programmable Operational Amplifier	3-84
μ A777	Precision Operational Amplifier	3-93
101	General Purpose Operational Amplifier	3-106
101A	General Purpose Operational Amplifier	3-109
102	Voltage Follower	3-127
107	General Purpose Operational Amplifier	3-116
110	Voltage Follower	3-127
201	General Purpose Operational Amplifier	3-106
201A	General Purpose Operational Amplifier	3-109
207	General Purpose Operational Amplifier	3-116
301A	General Purpose Operational Amplifier	3-109
302	Voltage Follower	3-127
307	General Purpose Operational Amplifier	3-116
310	Voltage Follower	3-127
1458	Internally Compensated, High Performance Dual Monolithic Operational Amplifier	3-132
1458C	Internally Compensated, High Performance Dual Monolithic Operational Amplifier	3-132
1558	Internally Compensated, High Performance Dual Monolithic Operational Amplifier	3-132

Low Input Current/Low Drift

μ A725	Instrumentation Operational Amplifier	3-30
μ A727	Temperature-Controlled Differential Preamplifier ...	3-39
μ A740	FET Input Operational Amplifier	3-49
μ A771	Instrumentation Amplifier.....	3-138

μ A776	Multi-Purpose Programmable Operational Amplifier	3-84
μ A777	Precision Operational Amplifier	3-93
108	Super Beta Operational Amplifier	3-121
108A	Super Beta Operational Amplifier	3-121
208	Super Beta Operational Amplifier	3-121
208A	Super Beta Operational Amplifier	3-121
308	Super Beta Operational Amplifier	3-121
308A	Super Beta Operational Amplifier	3-121
High Speed		
μ A715	High Speed Operational Amplifier	3-23
μ A772	High Slew Rate Operational Amplifier	3-138
μ A776	Multi-Purpose Programmable Operational Amplifier	3-84
μ A777	Precision Operational Amplifier	3-93
110	Voltage Follower	3-127
310	Voltage Follower	3-127
Low Power		
μ A776	Multi-Purpose Programmable Operational Amplifier	3-84
High Current/Power		
μ A791	Power Operational Amplifier	3-100
Products to be Announced		3-137
Glossary		3-139

INTRODUCTION

With the development of the μ A709 in 1967, Fairchild pioneered the development of monolithic operational amplifiers and has remained the industry leader. The μ A709 industry standard was followed by such other standards as the μ A741 internally compensated amplifier, the μ A740 FET input operational amplifier, the μ A715 high speed operational amplifier, the μ A725 high gain, low noise operational amplifier and the μ A791 power operational amplifier.

Today the Fairchild line of operational amplifiers covers every conceivable requirement from low drift to high slew rate and from low noise to high input impedance. Whatever the application, there is a Fairchild operational amplifier designed to perform it — precisely, economically and reliably.

SELECTION GUIDE FOR COMMERCIAL OPERATIONAL AMPLIFIERS

		GENERAL PURPOSE								
		TAILORED RESPONSE								
		μ A702*	μ A709	μ A739	μ A748	μ A749	μ A777	201	201A	301A
		DC Wide Band		Dual Low Noise		Dual				
Input Offset Voltage	Max (mV)	5.0	7.5	6.0	6.0	6.0	7.5	7.5	2.0	7.5
Input Offset Current	Max (nA)	2000	500	1000	200	500	50	200	10	50
Input Bias Current	Max (nA)	7500	1500	2000	500	1000	250	500	75	250
Voltage Gain	Min (V/mV)	2.0	15	6.5	20	15	25	20	25	25
Operating Supply Voltage Range	Min (V)	+6.0, -3.0	\pm 9.0	\pm 4.0	\pm 5.0	\pm 4.0	\pm 5.0	\pm 5.0	\pm 5.0	\pm 5.0
	Max (V)	+14, -7.0	\pm 18	\pm 18	\pm 18	\pm 18	\pm 20	\pm 20	\pm 20	\pm 20
Unity Gain Bandwidth	Typ (MHz)	30	1.0	10	1.0	10	1.0	1.0	1.0	1.0
Slew Rate	$A_{CL} = 1$	Typ (V/ μ s)	3.5	0.3	1.0	0.5	1.5	0.5	0.5	0.5
	$A_{CL} = -1$		3.5	0.3	2.5	6.0	2.5	6.0	6.0	6.0
	$A_{CL} = 10$		5.0	3.0	8.0	2.0	8.0	2.0	2.0	2.0
Input Voltage Range	Max (V)	+1.5, -6.0	\pm 10	\pm 15	\pm 15	\pm 15	\pm 15	\pm 15	\pm 15	\pm 15
Differential Input Voltage	Max (V)	\pm 5.0	\pm 5.0	\pm 5.0	\pm 30	\pm 5.0	\pm 30	\pm 30	\pm 30	\pm 30
Input Offset Voltage Drift	Typ (μ V/ $^{\circ}$ C)	10	10	4.0	7.0	3.0	3.0	7.0	3.0	6.0
Offset Adjust					X		X	X	X	X
Output Short Circuit Protection					X		X	X	X	X
Compensated										
Dual				X		X				

SELECTION GUIDE FOR MILITARY OPERATIONAL AMPLIFIERS

		GENERAL PURPOSE							
		TAILORED RESPONSE							
		μ 702*	μ A709A	μ A709	μ A748	μ A749	μ A777	101	101A
		DC Wide Band				Dual			
Input Offset Voltage	Max (mV)	2.0	2.0	5.0	5.0	3.0	2.0	5.0	2.0
Input Offset Current	Max (nA)	500	50	200	200	400	10	200	10
Input Bias Current	Max (nA)	5000	200	500	500	750	75	500	75
Voltage Gain	Min (V/mV)	2.5	25	25	50	25	50	50	50
Operating Supply Voltage Range	Min (V)	+6.0, -3.0	\pm 9.0	\pm 9.0	\pm 5.0	\pm 4.0	\pm 5.0	\pm 5.0	\pm 5.0
	Max (V)	+14, -7.0	\pm 18	\pm 18	\pm 22	\pm 18	\pm 20	\pm 20	\pm 20
Unity Gain Bandwidth	Typ (MHz)	30	5.0	5.0	1.0	10	1.0	1.0	1.0
Slew Rate	$A_{CL} = 1$	Typ (V/ μ s)	3.5	0.3	0.3	0.5	1.5	0.5	0.5
	$A_{CL} = -1$		3.5	0.3	0.3	6.0	2.5	6.0	6.0
	$A_{CL} = 10$		5.0	3.0	3.0	2.0	8.0	2.0	2.0
Input Voltage Range	Max (V)	+1.5, -6.0	\pm 10	\pm 10	\pm 15	\pm 15	\pm 15	\pm 15	\pm 15
Differential Input Voltage	Max (V)	\pm 5.0	\pm 5.0	\pm 5.0	\pm 30	\pm 5.0	\pm 30	\pm 30	\pm 30
Input Offset Voltage Drift	Typ (μ V/ $^{\circ}$ C)	10	1.8	3.0	7.0	3.0	3.0	3.0	3.0
	Max (μ V/ $^{\circ}$ C)						15		15
Offset Adjust					X		X	X	X
Output Short Circuit Protection					X		X	X	X
Compensated									
Dual						X			

* $V_S = +12, -6.0$ V

$V_S = \pm 15$ V, $T_A = 25^{\circ}$ C unless otherwise specified

GENERAL PURPOSE							HIGH POWER	LOW POWER
COMPENSATED								
307	310	$\mu A741$	$\mu A741E$	$\mu A776$	$\mu A747$	1458	$\mu A791$	$\mu A776$
	Voltage Follower	Industry Standard	High Performance	Programable ISET = 15 μA	Dual Industry Standard	Dual	1 Amp	150 μW Programable ISET = 1.5 μA
7.5	7.5	6.0	3.0	6.0	6.0	6.0	6.0	6.0
50	—	200	30	25	200	200	200	6.0
250	7.0	500	80	50	500	500	500	10
25	$.999 \times 10^{-3}$	20	50	50	20	20	20	50
± 5.0	± 5.0	± 5.0	± 5.0	± 1.2	± 5.0	± 5.0	± 5.0	± 1.2
± 18	± 18	± 18	± 22	± 18	± 18	± 18	± 18	± 18
1.0	20	1.0	1.0	1.0	1.0	1.0	0.2	0.2
0.5	30	0.5	0.7	0.7	0.5	0.5	0.5	0.1
0.5	—	0.5	0.7	0.7	0.5	0.5	1.0	0.1
0.5	—	0.5	0.7	0.7	0.5	0.5	6.0	0.1
± 15	± 10	± 15	± 15	± 15	± 15	± 15	± 15	± 15
± 30	—	± 30	± 30	± 30	± 30	± 30	± 30	± 30
6.0	10	7.0	3.0	3.0	7.0	7.0	15	3.0
X	X	X	X	X	X		X	X
X	X	X	X	X	X	X	X	X
X	X	X	X	X	X	X		X
					X	X		

3

GENERAL PURPOSE							HIGH POWER	LOW POWER
COMPENSATED								
107	110	$\mu A741$	$\mu A741A$	$\mu A776$	$\mu A747$	1558	$\mu A791$	$\mu A776$
	Voltage Follower	Industry Standard	High Performance	Programable ISET = 15 μA	Dual Industry Standard	Dual	1 Amp	150 μW Programable ISET = 1.5 μA
2.0	4.0	5.0	3.0	5.0	5.0	5.0	5.0	5.0
10	—	200	30	15	200	200	200	3.0
75	3.0	500	80	50	500	500	500	7.5
50	$.999 \times 10^{-3}$	50	50	50	50	50	50	50
± 5.0	± 5.0	± 5.0	± 5.0	± 1.2	± 5.0	± 5.0	± 5.0	± 1.2
± 20	± 18	± 22	± 22	± 18	± 22	± 22	± 22	± 18
1.0	20	1.0	1.0	1.0	1.0	1.0	0.2	0.2
0.5	30	0.5	0.6	0.7	0.5	0.5	0.5	0.1
0.5	—	0.5	0.6	0.7	0.5	0.5	1.0	0.1
0.5	—	0.5	0.6	0.7	0.5	0.5	6.0	0.1
± 15	± 10	± 15	± 15	± 15	± 15	± 15	± 15	± 15
± 30	—	± 30	± 30	± 30	± 30	± 30	± 30	± 30
3.0	6.0	7.0	5.0	3.0	7.0	7.0	10	3.0
15			15					
	X	X	X	X	X		X	X
X	X	X	X	X	X	X	X	X
X	X	X	X	X	X	X	X	X
					X	X		

SELECTION GUIDE FOR COMMERCIAL OPERATIONAL AMPLIFIERS

		HIGH ACCURACY INSTRUMENTATION						
		LOW BIAS CURRENT						
		FET	BIPOLAR		SUPER BETA			
		μ A740	μ A776	μ A777	208	308	208A	308A
		High Z_{IN} 10 ¹² Ω High Slew Rate	Low Power $I_{SET} = 1.5 \mu A$					
Input Offset Voltage	Max (mV)	100	6.0	7.5	2.0	7.5	0.5	0.5
Input Offset Current	Max (nA)	0.3	6.0	50	0.2	1.0	0.2	1.0
Input Bias Current	Max (nA)	2.0	10	250	2.0	7.0	2.0	7.0
Voltage Gain	Min (V/mV)	25	50	25	50	15	80	80
Operating Supply Voltage Range	Min (V)	± 5.0	± 1.2	± 5.0	± 5.0	± 5.0	± 5.0	± 5.0
	Max (V)	± 22	± 18	± 20	± 20	± 18	± 20	± 20
Unity Gain Bandwidth	Typ (MHz)	3.0	0.2	1.0	1.0	1.0	1.0	1.0
Slew Rate	$A_{CL} = 1$	6.0	0.1	0.5	0.3	0.3	0.3	0.3
	$A_{CL} = -1$	6.0	0.1	6.0	0.6	0.6	0.6	0.6
	$A_{CL} = 10$	6.0	0.1	2.0	—	—	—	—
Input Voltage Range	Max (V)	± 15	± 15	± 15	± 15	± 15	± 15	± 15
Differential Input Voltage	Max (V)	± 30	± 30	± 30	± 0.5	± 0.5	± 0.5	± 0.5
Input Offset Voltage Drift	Typ ($\mu V/^{\circ}C$)	20	3.0	3.0	3.0	6.0	1.0	1.0
	Max ($\mu V/^{\circ}C$)	—	—	—	15	30	5.0	5.0
Offset Adjust		X	X	X				
Output Short Circuit Protection		X	X	X	X	X	X	X
Compensated		X	X					

SELECTION GUIDE FOR MILITARY OPERATIONAL AMPLIFIERS

		HIGH ACCURACY INSTRUMENTATION				
		LOW BIAS CURRENT				
		FET	BIPOLAR		SUPER BETA	
		μ A740	μ A776	μ A777	108	108A
		High Z_{IN} 10 ¹² Ω High Slew Rate	Low Power $I_{SET} = 1.5 \mu A$			
Input Offset Voltage	Max (mV)	20	5.0	2.0	2.0	0.5
Input Offset Current	Max (nA)	0.15	3.0	10	0.2	0.2
Input Bias Current	Max (nA)	0.2	7.5	75	2.0	2.0
Voltage Gain	Min (V/mV)	50	50	50	50	80
Operating Supply Voltage Range	Min (V)	± 5.0	± 1.2	± 5.0	± 5.0	± 5.0
	Max (V)	± 22	± 18	± 20	± 20	± 20
Unity Gain Bandwidth	Typ (MHz)	3.0	0.2	1.0	1.0	1.0
Slew Rate	$A_{CL} = 1$	6.0	0.1	0.5	0.3	0.3
	$A_{CL} = -1$	6.0	0.1	6.0	0.6	0.6
	$A_{CL} = 10$	6.0	0.1	2.0	—	—
Input Voltage Range	Max (V)	± 15	± 15	± 15	± 15	± 15
Differential Input Voltage	Max (V)	± 30	± 30	± 30	± 0.5	± 0.5
Input Offset Voltage Drift	Typ ($\mu V/^{\circ}C$)	20	3.0	3.0	3.0	1.0
	Max ($\mu V/^{\circ}C$)	—	—	15	15	5.0
Offset Adjust		X	X	X		
Output Short Circuit Protection		X	X	X	X	X
Compensated		X	X			

HIGH ACCURACY INSTRUMENTATION						HIGH SPEED							
LOW DRIFT													
OP AMPS					PREAMPS								
μ A725C	μ A725E	μ A741E	208A	308A	μ A726	μ A727	μ A715	μ A748	μ A776	μ A777	301A	310	
					$I_C = 10 \mu A$ Temp. 0 to +85°C	Temp. -20 to +85°C		Feed-Forward	Programable $I_{SET} = 500 \mu A$	Feed-Forward	Feed-Forward	Voltage Follower	
2.5	0.5	3.0	0.5	0.5	3.0	10	7.5	6.0	6.0	7.5	7.5	7.5	
35	5.0	30	100	1.0	100	25	250	200	6.0	50	50	—	
125	75	80	300	7.0	300	75	1500	500	10	250	250	7.0	
250	1000	50	—	80	—	0.06	10	20	50	25	25	$.999 \times 10^{-3}$	
± 3.0	± 3.0	± 5.0	± 5.0	± 5.0	± 5.0	± 9.0	± 6.0	± 5.0	± 1.2	± 5.0	± 5.0	± 5.0	
± 22	± 22	± 22	± 18	± 20	± 18	± 18	± 18	± 18	± 18	± 20	± 20	± 18	
1.0	1.0	1.0	1.0	1.0	20	1.0	65	1.0	1.2	1.0	1.0	20	
—	—	0.6	0.3	0.3	—	—	18	0.5	15	0.5	0.5	30	
—	—	0.6	0.6	0.6	—	—	100	6.0	15	6.0	15	—	
—	—	0.6	—	—	—	—	38	2.0	15	2.0	5.0	—	
± 22	± 22	± 15	± 15	± 15	± 30	± 10	± 15	± 15	± 15	± 15	± 15	± 15	
± 22	± 22	± 30	± 0.5	± 0.5	± 5.0	± 15	± 15	± 30	± 30	± 30	± 30	—	
0.5	0.5	4.0	1.0	1.0	0.2	0.6	6.0	7.0	3.0	3.0	6.0	10	
5.0	2.0	15	5.0	5.0	1.0	1.5							
X	X	X		X	X		X	X	X	X	X	X	
X	X	X		X	X	X		X	X	X	X	X	
		X			X								

3

HIGH ACCURACY INSTRUMENTATION						HIGH SPEED					
LOW DRIFT											
OP AMPS				PREAMPS							
μ A725	μ A725A	μ A741A	108A	μ A726	μ A727	μ A715	μ A748	μ A776	μ A777	101A	110
				$I_C = 10 \mu A$			Feed-Forward	Programable $I_{SET} = 500 \mu A$	Feed-Forward	Feed-Forward	Voltage Follower
1.0	0.5	3.0	0.5	2.5	10	5.0	5.0	5.0	2.0	2.0	4.0
20	5.0	30	0.2	50	15	250	200	3.0	10	10	—
100	75	80	2.0	150	40	750	500	7.5	75	75	3.0
1000	1000	50	80	—	0.06	15	50	50	50	50	$.999 \times 10^{-3}$
± 3.0	± 3.0	± 5.0	—	± 5.0	± 9.0	± 6.0	± 5.0	± 1.2	± 5.0	± 5.0	± 5.0
± 22	± 22	± 22	± 20	± 18	± 18	± 18	± 22	± 18	± 20	± 20	± 18
1.0	1.0	1.0	1.0	20	1.0	65	1.0	1.2	1.0	1.0	20
—	—	0.6	0.3	—	—	18	0.5	15	0.5	0.5	30
—	—	0.6	0.6	—	—	100	6.0	15	6.0	6.0	—
—	—	0.6	—	—	—	38	2.0	15	2.0	2.0	—
± 22	± 22	± 15	± 15	± 30	± 10	± 15	± 15	± 15	± 15	± 15	± 15
± 22	± 22	± 30	± 0.5	± 5.0	± 15	± 15	± 30	± 30	± 30	± 30	—
0.5	0.5	3.0	1.0	0.2	0.6	6.0	7.0	3.0	3.0	3.0	6.0
5.0	2.0	15	5.0	1.0	1.5					15	
X	X	X		X		X	X	X	X	X	X
X	X	X	X	X	X		X	X	X	X	X
		X		X							

μA702

WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA702 is a monolithic DC Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from dc to 30 MHz.

- **LOW OFFSET VOLTAGE**
- **LOW OFFSET VOLTAGE DRIFT**
- **WIDE BANDWIDTH — 20 MHz TYP.**
- **HIGH SLEW RATE — 5 V/μs TYP.**

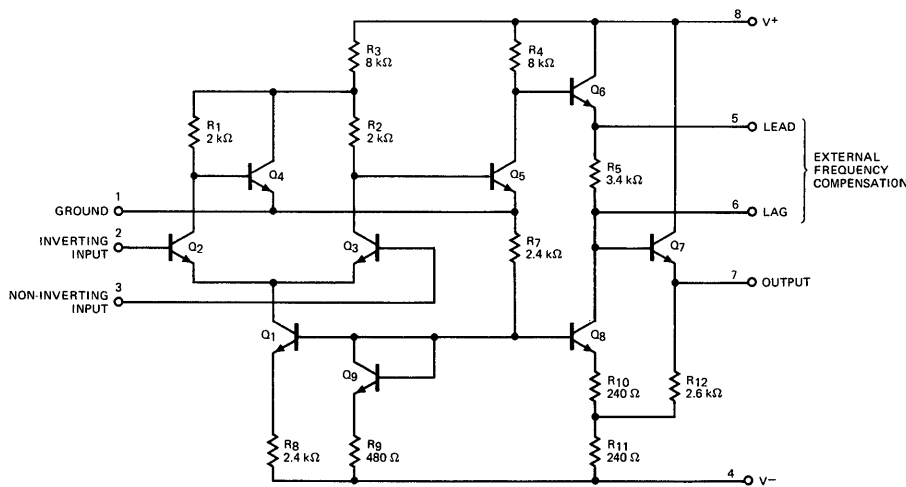
ABSOLUTE MAXIMUM RATINGS

Voltage Between V ⁺ and V ⁻ Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to -6.0 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (702)	-55°C to +125°C
Commercial (702C)	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

NOTE

Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for DIP and 7.1mW/°C for the Flatpak.

EQUIVALENT CIRCUIT

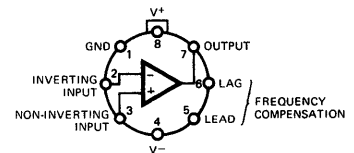


Pin numbers are shown for Metal Can only.

CONNECTION DIAGRAMS

8-LEAD METAL CAN (TOP VIEW)

PACKAGE OUTLINE 5B



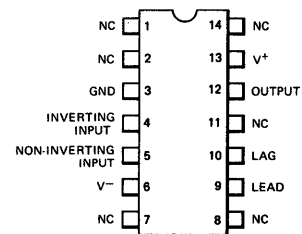
NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
702	702HM
702C	702HC

14-LEAD DIP (TOP VIEW)

PACKAGE OUTLINE 6A

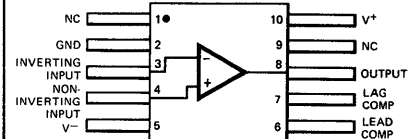


ORDER INFORMATION

TYPE	PART NO.
702	702DM
702C	702DC

10-LEAD FLATPAK (TOP VIEW)

PACKAGE OUTLINE 3F



ORDER INFORMATION

TYPE	PART NO.
702	702FM

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A702$

702

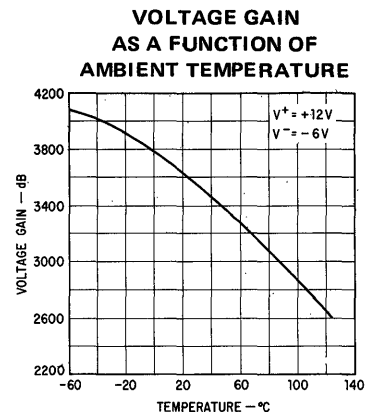
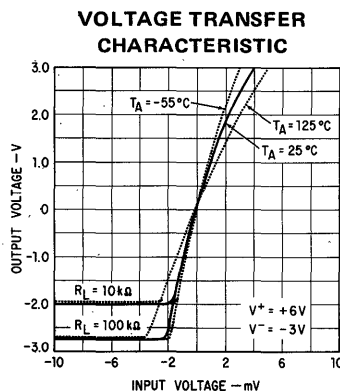
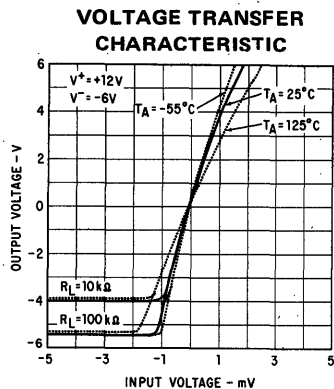
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	CONDITIONS	$V_+ = 12.0\text{ V}, V_- = -6.0\text{ V}$			$V_+ = 6.0\text{ V}, V_- = -3.0\text{ V}$			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 2\text{ k}\Omega$		0.5	2.0		0.7	3.0	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2.0	5.0		1.2	3.5	μA
Input Resistance			16	40		22	67	k Ω
Input Voltage Range			-4.0	+0.5		-1.5	+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\text{ k}\Omega, f \leq 1\text{ kHz}$		80	100		80	100	dB
Large Signal Voltage Gain	$R_L \geq 100\text{ k}\Omega, V_{OUT} = \pm 5.0\text{ V}$		2500	3600		600	900	
	$R_L \geq 100\text{ k}\Omega, V_{OUT} = \pm 2.5\text{ V}$			6000		1500		
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{OUT} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{OUT} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_1 = 0.01\text{ }\mu\text{F}, R_1 = 20\text{ }\Omega, R_L \geq 100\text{ k}\Omega, V_{IN} = 10\text{ mV}, C_L \leq 100\text{ pF}$	Risetime		25				ns
		Overshoot		10				
Transient Response (x100 gain)	$C_3 = 50\text{ pF}, R_L \geq 100\text{ k}\Omega, V_{IN} = 1\text{ mV}$	Risetime		10				ns
		Overshoot		20				

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$:

Input Offset Voltage	$R_S \leq 2\text{ k}\Omega$		3.0		4.0		mV	
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\text{ }\Omega, T_A = 25^\circ\text{C to } +125^\circ\text{C}$		2.5	10		3.5	15	$\mu\text{V}/^\circ\text{C}$
	$R_S = 50\text{ }\Omega, T_A = 25^\circ\text{C to } -55^\circ\text{C}$		2.0	10		3.0	15	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$T_A = +125^\circ\text{C}$		80	500		50	500	nA
	$T_A = -55^\circ\text{C}$		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25^\circ\text{C to } +125^\circ\text{C}$		1.0	5.0		0.7	4.0	nA/ $^\circ\text{C}$
	$T_A = 25^\circ\text{C to } -55^\circ\text{C}$		3.0	16		2.0	13	nA/ $^\circ\text{C}$
Input Bias Current	$T_A = -55^\circ\text{C}$		4.3	10		2.6	7.5	μA
Input Resistance			6.0			8.0		k Ω
Common Mode Rejection Ratio	$R_S \leq 2\text{ k}\Omega, f \leq 1\text{ kHz}$		70	95		70	95	dB
Supply Voltage Rejection Ratio	$V_+ = 12\text{ V}, V_- = -6\text{ V to } V_+ = 6\text{ V}, V_- = -3\text{ V}$		75	200		75	200	$\mu\text{V}/\text{V}$
	$R_S \leq 2\text{ k}\Omega$							
Large Signal Voltage Gain	$R_L \geq 100\text{ k}\Omega, V_{OUT} = \pm 5.0\text{ V}$		2000	7000				
	$R_L \geq 100\text{ k}\Omega, V_{OUT} = \pm 2.5\text{ V}$					500	1750	
Output Voltage Swing	$R_L \geq 100\text{ k}\Omega$		± 5.0	± 5.3		± 2.5	± 2.7	V
	$R_L \geq 10\text{ k}\Omega$		± 3.5	± 4.0		± 1.5	± 2.0	V
Supply Current	$T_A = +125^\circ\text{C}, V_{OUT} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55^\circ\text{C}, V_{OUT} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125^\circ\text{C}, V_{OUT} = 0$		80	120		15	30	mW
	$T_A = -55^\circ\text{C}, V_{OUT} = 0$		90	135		19	35	mW

TYPICAL PERFORMANCE CURVES FOR 702



FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A702$

702C

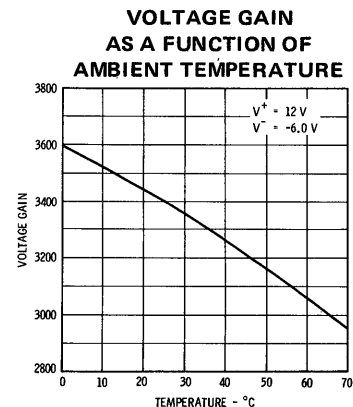
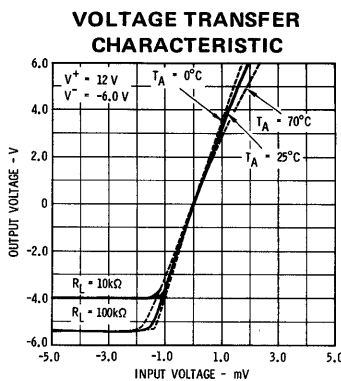
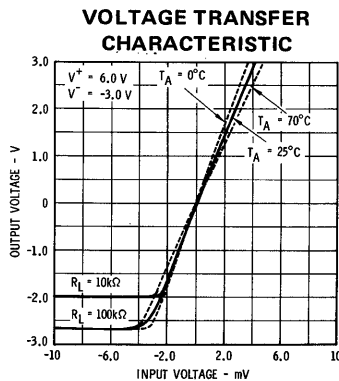
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	CONDITIONS	$V_+ = 12.0\text{ V}, V_- = -6.0\text{ V}$			$V_+ = 6.0\text{ V}, V_- = -3.0\text{ V}$			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 2\text{ k}\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance			10	32		16	55	$\text{k}\Omega$
Input Voltage Range		-4.0		+0.5	-1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\text{ k}\Omega, f \leq 1\text{ kHz}$	70	92		70	92		dB
Large Signal Voltage Gain	$R_L \geq 100\text{ k}\Omega, V_{OUT} = \pm 5.0\text{ V}$	2000	3400	6000				
	$R_L \geq 100\text{ k}\Omega, V_{OUT} = \pm 2.5\text{ V}$				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{OUT} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{OUT} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_1 = 0.01\text{ }\mu\text{F}, R_1 = 20\text{ }\Omega$ $R_L \leq 100\text{ k}\Omega, V_{IN} = 10\text{ mV}$ $C_L \leq 100\text{ pF}$	Risetime		25	120			ns
		Overshoot		10	50			%
Transient Response (x100 gain)	$C_3 = 50\text{ pF}, R_L \geq 100\text{ k}\Omega,$ $V_{IN} = 1\text{ mV}$	Risetime		10	30			ns
		Overshoot		20	40			%

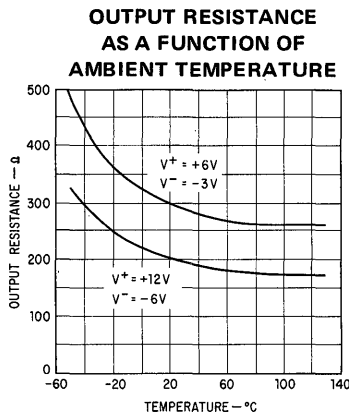
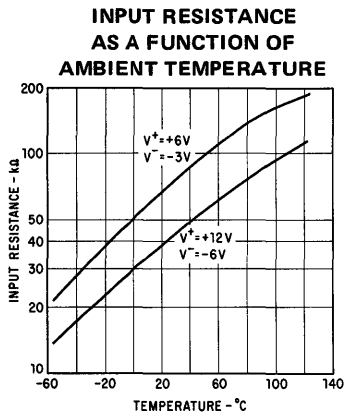
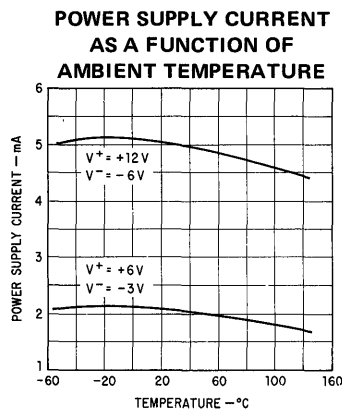
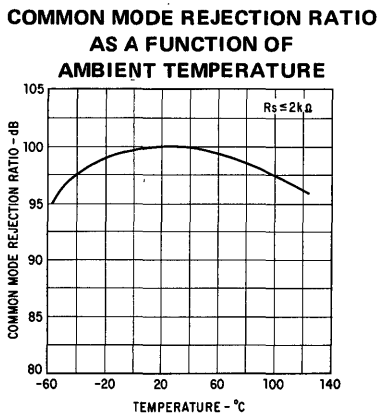
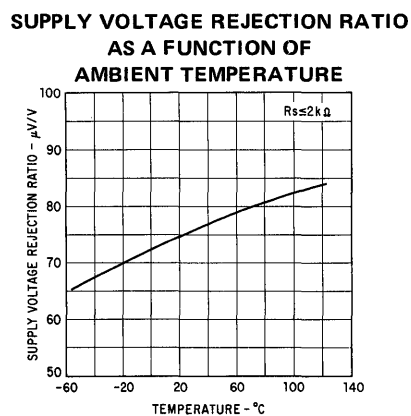
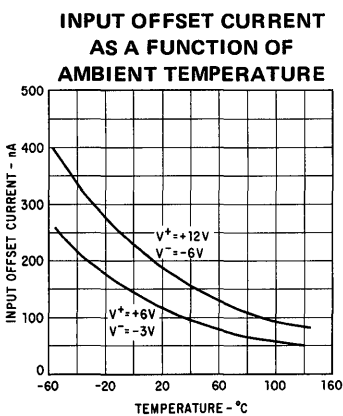
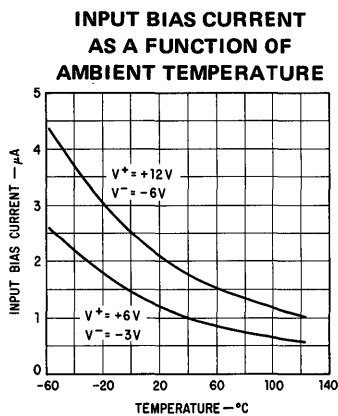
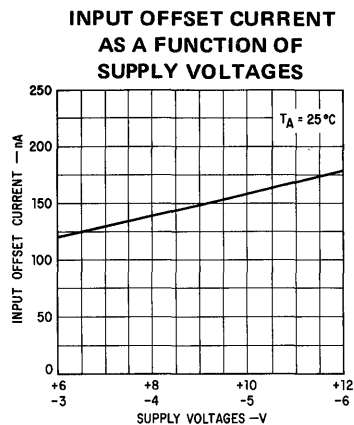
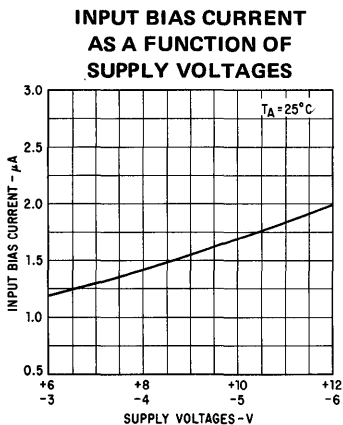
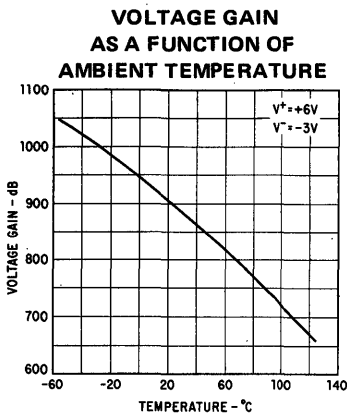
The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$:

Input Offset Voltage	$R_S \leq 2\text{ k}\Omega$			6.5		7.5		mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\text{ }\Omega,$ $T_A = +70^\circ\text{C to } 0^\circ\text{C}$		5.0	20		7.5	25	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25^\circ\text{C to } +70^\circ\text{C}$ $T_A = 25^\circ\text{C to } 0^\circ\text{C}$		4.0	10		3.0	8.0	$\text{nA}/^\circ\text{C}$
			6.0	20		5.5	18	$\text{nA}/^\circ\text{C}$
Input Bias Current	$T_A = 0^\circ\text{C}$		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		$\text{k}\Omega$
Common Mode Rejection Ratio	$R_S \leq 2\text{ k}\Omega, f \leq 1\text{ kHz}$	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V_+ = 12\text{ V}, V_- = 6\text{ V to } 3\text{ V}$ $V_+ = 6\text{ V}, V_- = 3\text{ V}$ $R_S \leq 2\text{ k}\Omega$		90	300		90	300	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	$R_L \geq 100\text{ k}\Omega, V_{OUT} = \pm 5.0\text{ V}$ $R_L \geq 100\text{ k}\Omega, V_{OUT} = \pm 2.5\text{ V}$	1500		7000				
					400		1750	
Output Voltage Swing	$R_L \geq 100\text{ k}\Omega$ $R_L \geq 10\text{ k}\Omega$	± 5.0	± 5.3		± 2.5	± 2.7		V
		± 3.5	± 4.0		± 1.5	± 2.0		V
Supply Current	$V_{OUT} = 0$		5.0	7.0		2.1	3.9	mA
Power Consumption	$V_{OUT} = 0$		90	125		19	35	mW

TYPICAL PERFORMANCE CURVES FOR 702C

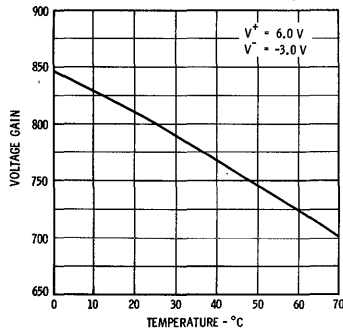


TYPICAL PERFORMANCE CURVES FOR 702

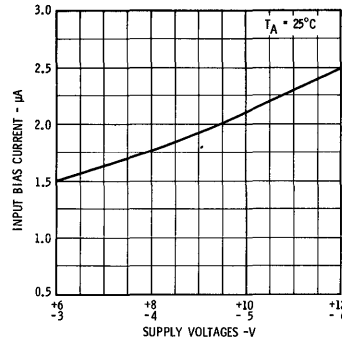


TYPICAL PERFORMANCE CURVES FOR 702C

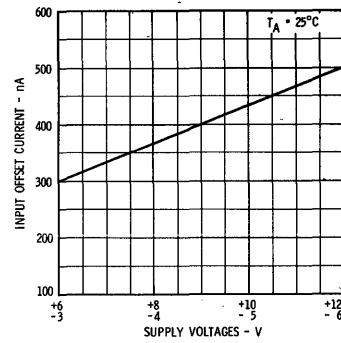
VOLTAGE GAIN
AS A FUNCTION OF
AMBIENT TEMPERATURE



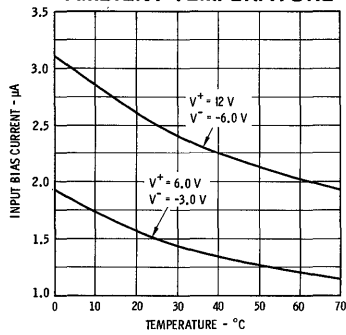
INPUT BIAS CURRENT
AS A FUNCTION OF
SUPPLY VOLTAGES



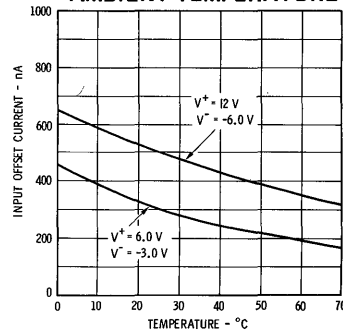
INPUT OFFSET CURRENT
AS A FUNCTION OF
SUPPLY VOLTAGES



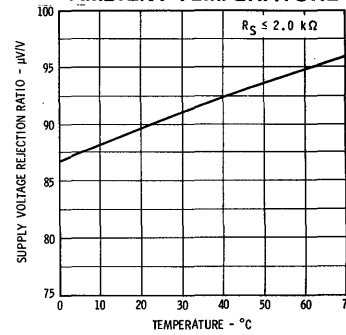
INPUT BIAS CURRENT
AS A FUNCTION OF
AMBIENT TEMPERATURE



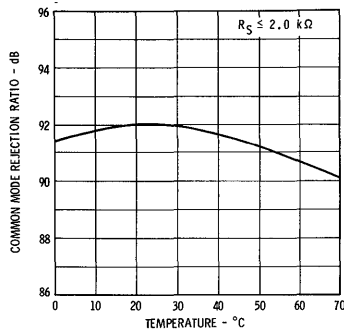
INPUT OFFSET CURRENT
AS A FUNCTION OF
AMBIENT TEMPERATURE



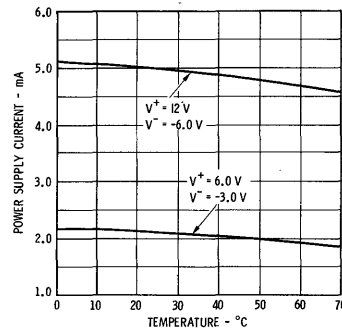
SUPPLY VOLTAGE REJECTION RATIO
AS A FUNCTION OF
AMBIENT TEMPERATURE



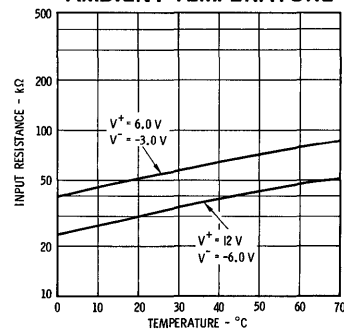
COMMON MODE REJECTION RATIO
AS A FUNCTION OF
AMBIENT TEMPERATURE



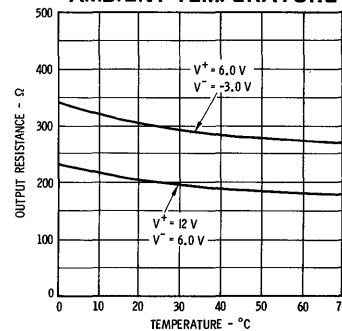
POWER SUPPLY CURRENT
AS A FUNCTION OF
AMBIENT TEMPERATURE



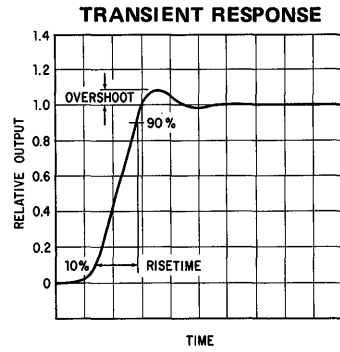
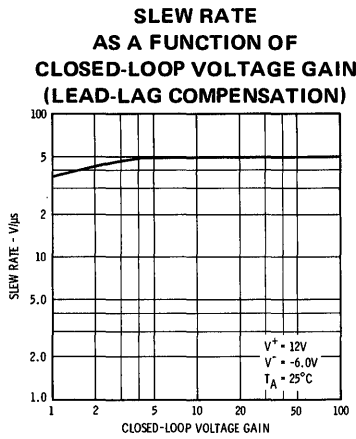
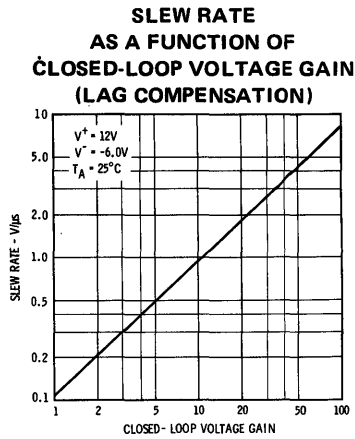
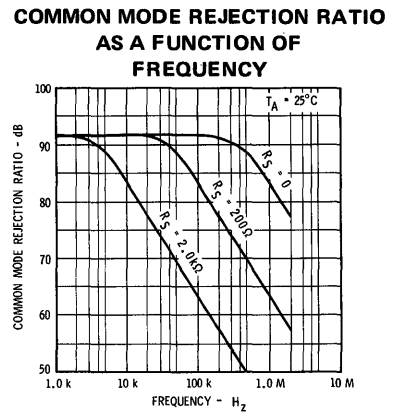
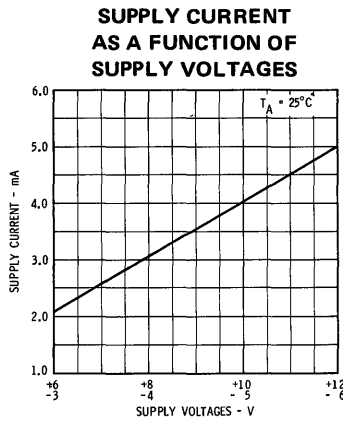
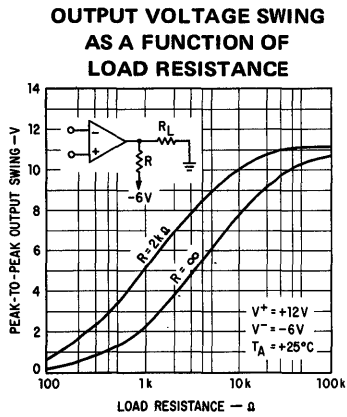
INPUT RESISTANCE
AS A FUNCTION OF
AMBIENT TEMPERATURE



OUTPUT RESISTANCE
AS A FUNCTION OF
AMBIENT TEMPERATURE

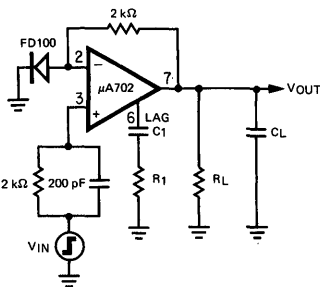


TYPICAL PERFORMANCE CURVES FOR 702 AND 702C

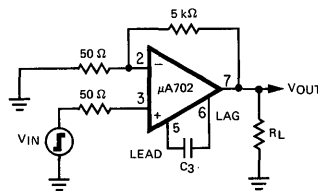


TRANSIENT RESPONSE TEST CIRCUITS

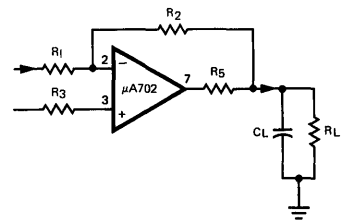
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



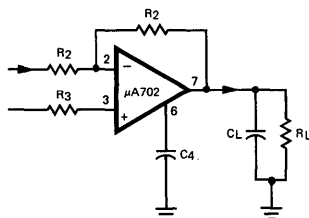
X100 AMPLIFIER (LEAD COMPENSATION)



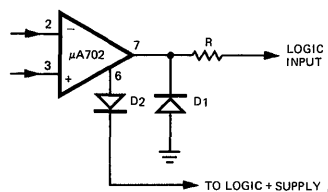
SERIES RESISTANCE LIMITING*



OUTPUT RISE-TIME LIMITING*



LOGIC COMPATIBILITY

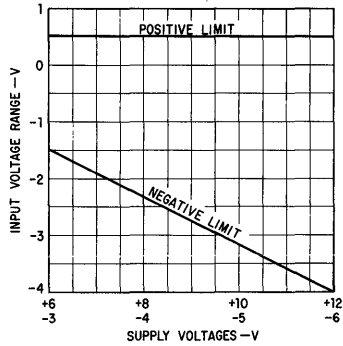


*Peak Current Limiting with Capacitive Loads.

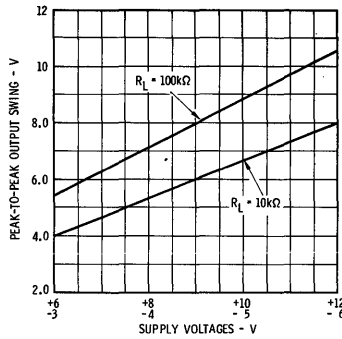
Pin numbers are shown for Metal Can only.

TYPICAL PERFORMANCE CURVES FOR 702 AND 702C

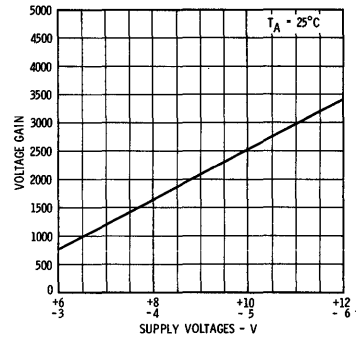
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



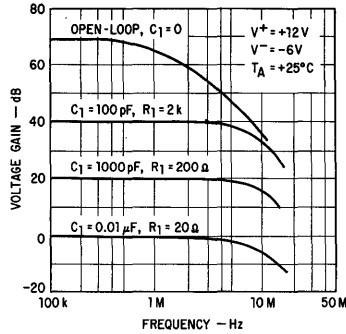
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



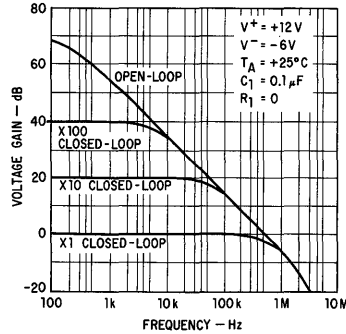
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



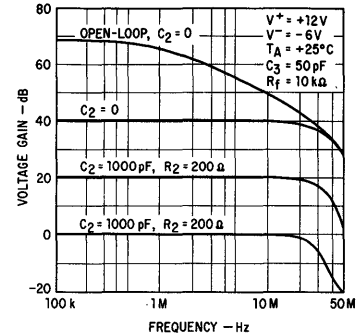
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



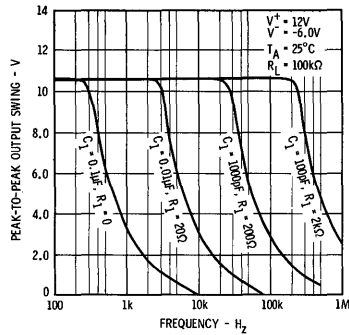
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



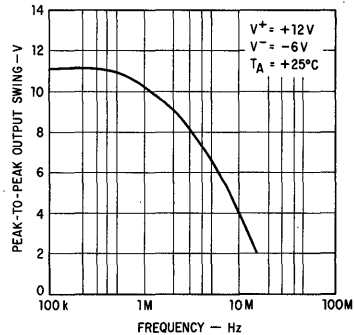
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

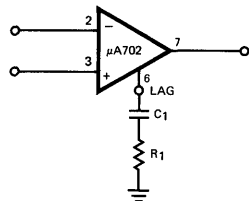


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION

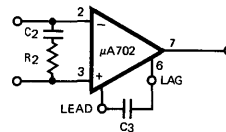


FREQUENCY COMPENSATION CIRCUITS

LAG COMPENSATION



LEAD-LAG COMPENSATION



Pin numbers are shown for Metal Can only.

μA709

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

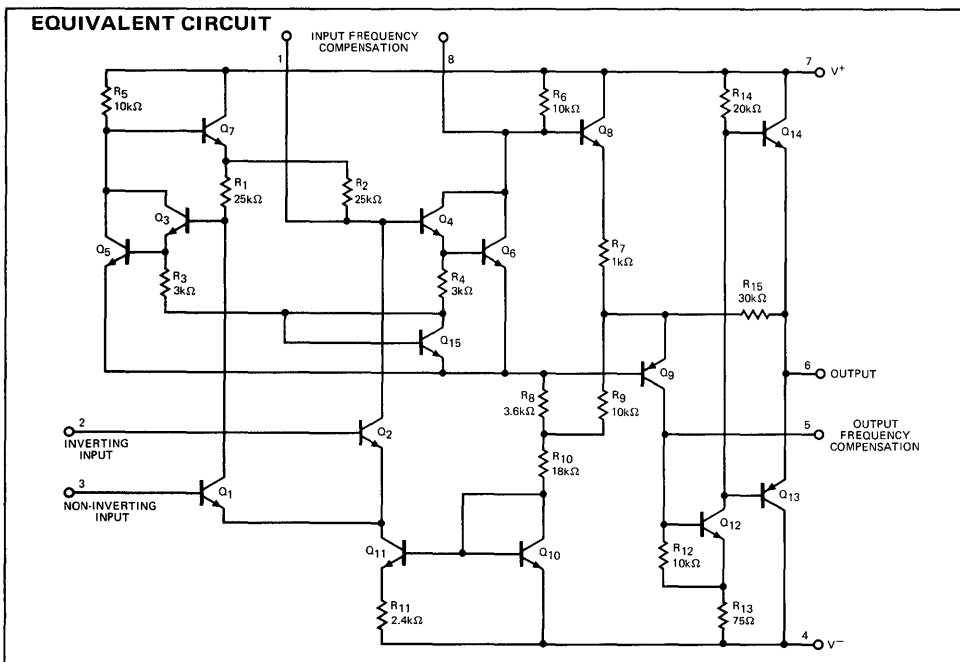
GENERAL DESCRIPTION — The μA709 is a monolithic High Gain Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in dc servo systems, high impedance analog computers, low level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 18 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Differential Input Voltage	± 5.0 V
Input Voltage	± 10 V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	-65°C to +150°C
Operating Temperature Range	
Military (709A and 709)	-55°C to +125°C
Commercial (709C)	0°C to +70°C
Lead Temperature	
Metal Can, DIP and Flatpak (Soldering 60 seconds)	300°C
Output Short Circuit Duration	5 seconds

NOTE

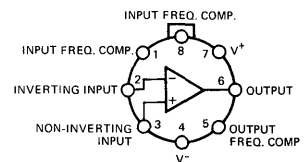
Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for DIP and 7.1mW/°C for the Flatpak.



CONNECTION DIAGRAMS

8-LEAD METAL CAN (TOP VIEW)

PACKAGE OUTLINE 5B



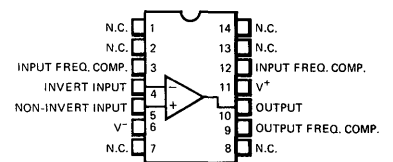
NOTE: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
709A	709AHM
709	709HM
709C	709HC

14-LEAD DIP (TOP VIEW)

PACKAGE OUTLINE 6A

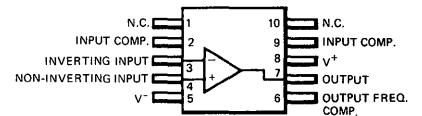


ORDER INFORMATION

TYPE	PART NO.
709A	709ADM
709	709DM
709C	709DC

10-LEAD FLATPAK (TOP VIEW)

PACKAGE OUTLINE 3F



ORDER INFORMATION

TYPE	PART NO.
709A	709AFM
709	709FM

* Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A709

709A

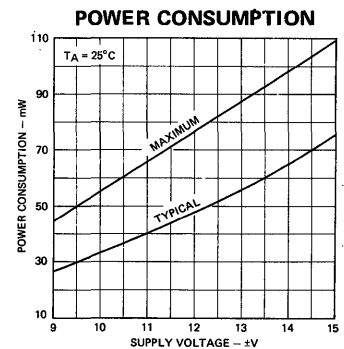
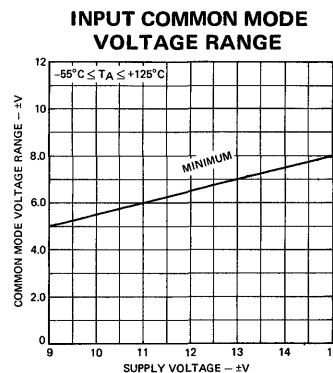
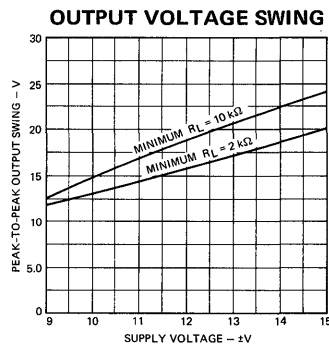
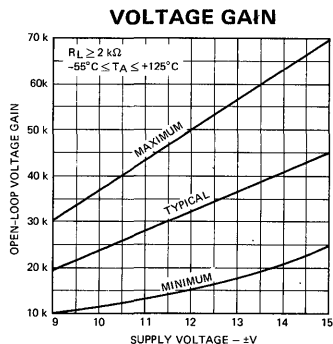
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $\pm 9\text{ V} \leq V_S \leq \pm 15\text{ V}$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$		0.6	2.0	mV
Input Offset Current			10	50	nA
Input Bias Current			100	200	nA
Input Resistance		350	700		k Ω
Output Resistance			150		Ω
Supply Current	$V_S = \pm 15\text{ V}$		2.5	3.6	mA
Power Consumption	$V_S = \pm 15\text{ V}$		75	108	mW
Transient Response	Risetime	$V_S = \pm 15\text{ V}$, $V_{IN} = 20\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_1 = 5\text{ nF}$, $R_1 = 1.5\text{ k}\Omega$, $C_2 = 200\text{ pF}$, $R_2 = 50\Omega$		1.5	μs
	Overshoot			30	%

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$:

Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = +25^\circ\text{C}$ to $+125^\circ\text{C}$		1.8	10	$\mu\text{V}/^\circ\text{C}$
	$R_S = 50\Omega$, $T_A = +25^\circ\text{C}$ to -55°C		1.8	10	$\mu\text{V}/^\circ\text{C}$
	$R_S = 10\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ to $+125^\circ\text{C}$		2.0	15	$\mu\text{V}/^\circ\text{C}$
	$R_S = 10\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ to -55°C		4.8	25	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$T_A = +125^\circ\text{C}$		3.5	50	nA
	$T_A = -55^\circ\text{C}$		40	250	nA
Average Temperature Coefficient of Input Offset Current	$T_A = +25^\circ\text{C}$ to $+125^\circ\text{C}$		0.08	0.5	$\text{nA}/^\circ\text{C}$
	$T_A = +25^\circ\text{C}$ to -55°C		0.45	2.8	$\text{nA}/^\circ\text{C}$
Input Bias Current	$T_A = -55^\circ\text{C}$		300	600	nA
Input Resistance	$T_A = -55^\circ\text{C}$	85	170		k Ω
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 8.0			V
Common Mode Rejection Ratio	$R_S \leq 10\text{ k}\Omega$	80	110		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{ k}\Omega$		40	100	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	25,000		70,000	V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$	± 12	± 14		V
	$V_S = \pm 15\text{ V}$, $R_L \geq 2\text{ k}\Omega$	± 10	± 13		V
Supply Current	$T_A = +125^\circ\text{C}$, $V_S = \pm 15\text{ V}$		2.1	3.0	mA
	$T_A = -55^\circ\text{C}$, $V_S = \pm 15\text{ V}$		2.7	4.5	mA
Power Consumption	$T_A = +125^\circ\text{C}$, $V_S = \pm 15\text{ V}$		63	90	mW
	$T_A = -55^\circ\text{C}$, $V_S = \pm 15\text{ V}$		81	135	mW

PERFORMANCE CURVES FOR 709A



FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A709$

709

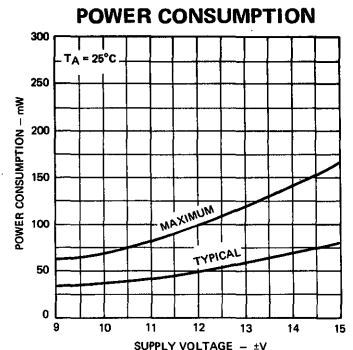
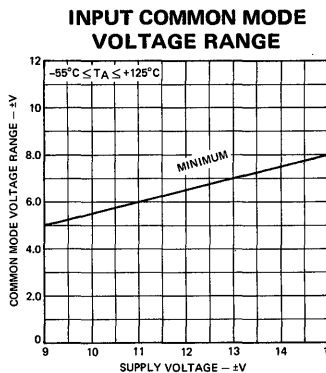
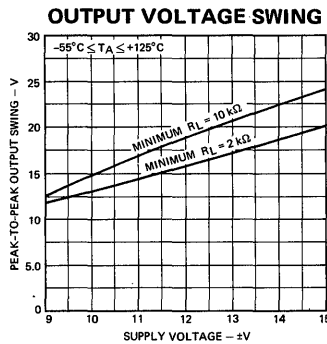
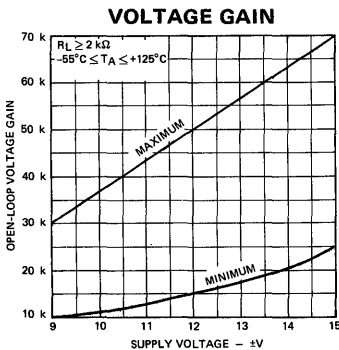
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ C, \pm 9 V \leq V_S \leq \pm 15 V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10 k\Omega$		1.0	5.0	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		$k\Omega$
Output Resistance			150		Ω
Power Consumption	$V_S = \pm 15 V$		80	165	mW
Transient Response	$V_{IN} = 20 mV, R_L = 2 k\Omega,$ $C_1 = 5000 pF, R_1 = 1.5 k\Omega,$ $C_2 = 200 pF, R_2 = 50\Omega$		0.3	1.0	μs
	Overshoot		10	30	%

The following specifications apply for $-55^\circ C \leq T_A \leq +125^\circ C$:

Input Offset Voltage	$R_S \leq 10 k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		3.0		$\mu V/^\circ C$
	$R_S \leq 10 k\Omega$		6.0		$\mu V/^\circ C$
Large Signal Voltage Gain	$V_S = \pm 15 V, R_L \geq 2 k\Omega,$ $V_{OUT} = \pm 10 V$	25,000	45,000	70,000	V/V
Output Voltage Swing	$V_S = \pm 15 V, R_L \geq 10 k\Omega$	± 12	± 14		V
	$V_S = \pm 15 V, R_L \geq 2 k\Omega$	± 10	± 13		V
Input Voltage Range	$V_S = \pm 15 V$	± 8.0	± 10		V
Common Mode Rejection Ratio	$R_S \leq 10 k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10 k\Omega$		25	150	$\mu V/V$
Input Offset Current	$T_A = +125^\circ C$		20	200	nA
	$T_A = -55^\circ C$		100	500	nA
Input Bias Current	$T_A = -55^\circ C$		0.5	1.5	μA
Input Resistance		40	100		$k\Omega$

PERFORMANCE CURVES FOR 709



FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A709$

709C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

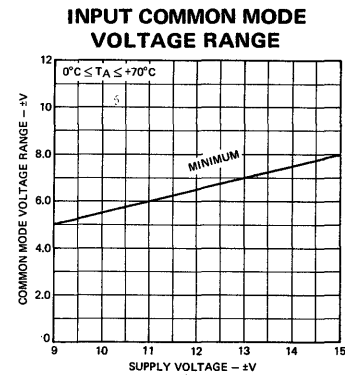
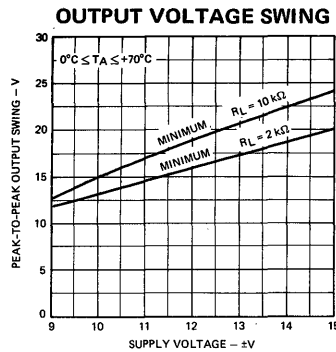
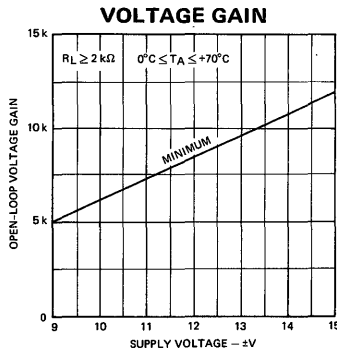
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$, $\pm 9\text{ V} \leq V_S \leq \pm 15\text{ V}$		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		$\text{k}\Omega$
Output Resistance			150		Ω
Large Signal Voltage Gain	$R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	15,000	45,000		V/V
Output Voltage Swing	$R_L \geq 10\text{ k}\Omega$	± 12	± 14		V
	$R_L \geq 2\text{ k}\Omega$	± 10	± 13		V
Input Voltage Range		± 8.0	± 10		V
Common Mode Rejection Ratio	$R_S \leq 10\text{ k}\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{ k}\Omega$		25	200	$\mu\text{V/V}$
Power Consumption			80	200	mW
Transient Response	$V_{IN} = 20\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_1 = 5000\text{ pF}$, $R_1 = 1.5\text{ k}\Omega$, $C_2 = 200\text{ pF}$, $R_2 = 50\Omega$, $C_L \leq 100\text{ pF}$	Risetime		0.3	μs
		Overshoot		10	%

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$:

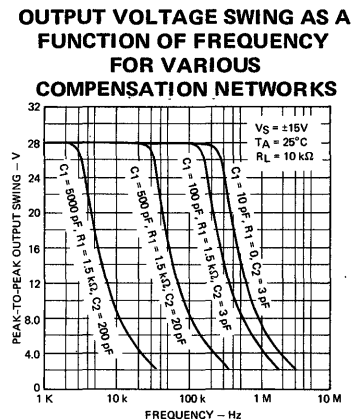
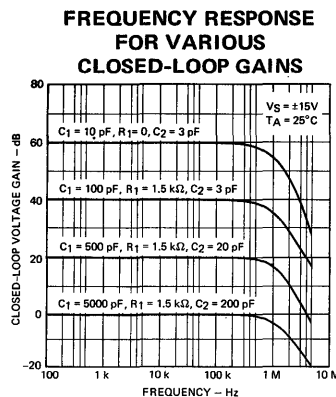
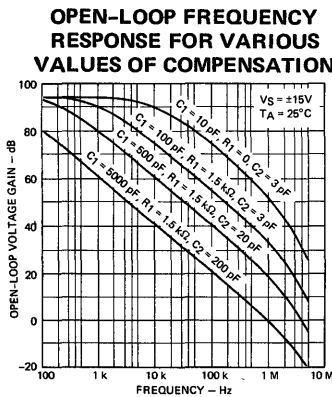
Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$, $\pm 9\text{ V} \leq V_S \leq \pm 15\text{ V}$			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large Signal Voltage Gain	$R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	12,000			V/V
Input Resistance		35			$\text{k}\Omega$

3

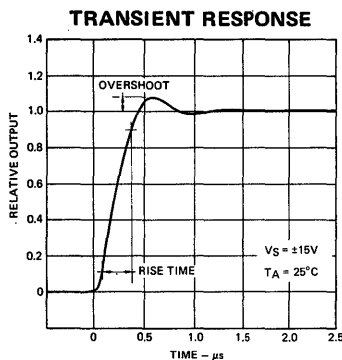
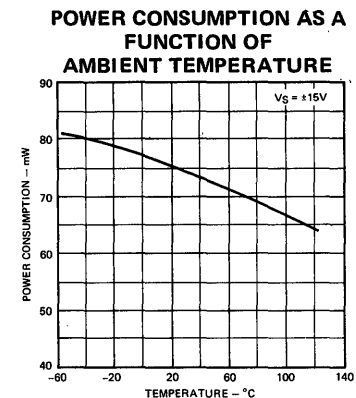
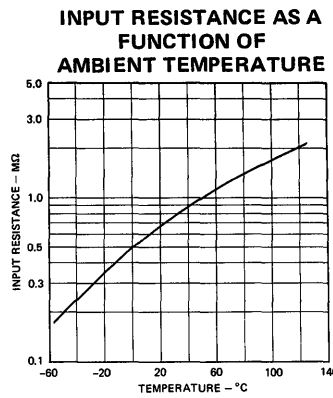
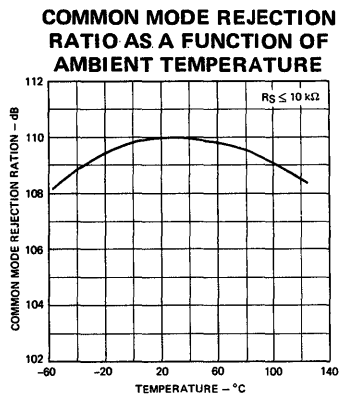
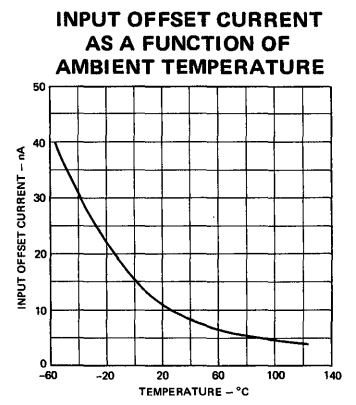
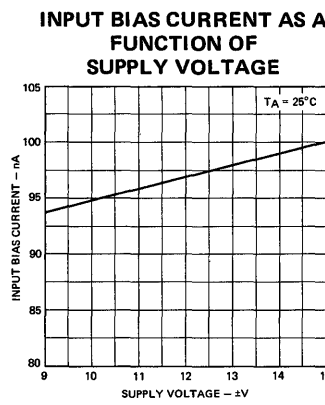
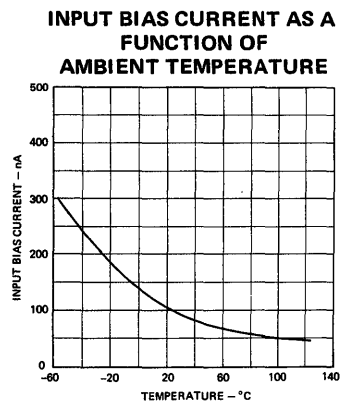
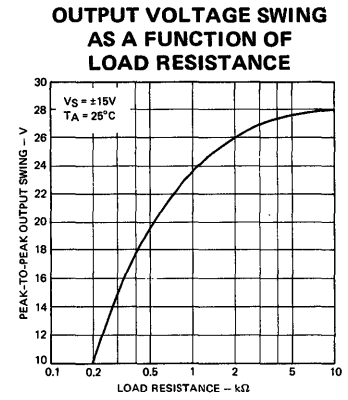
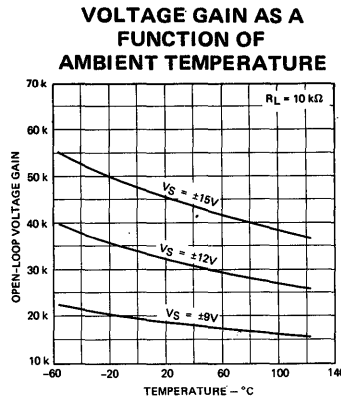
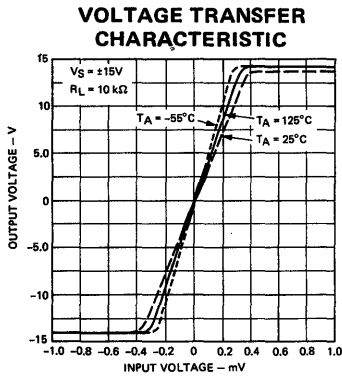
PERFORMANCE CURVES FOR 709C



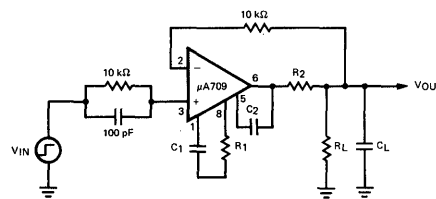
FREQUENCY COMPENSATION CURVES FOR ALL TYPES



TYPICAL PERFORMANCE CURVES FOR 709A

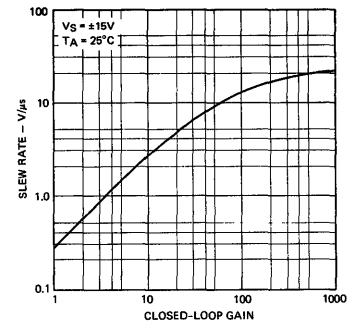


TRANSIENT RESPONSE TEST CIRCUIT

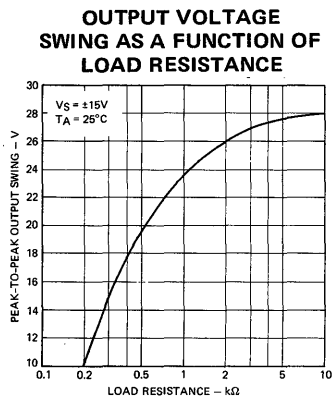
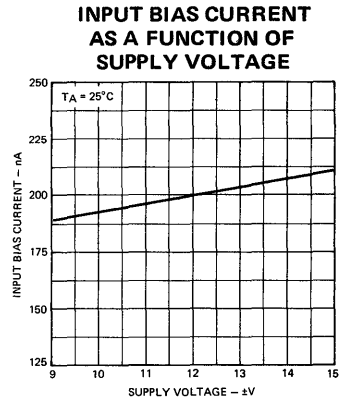
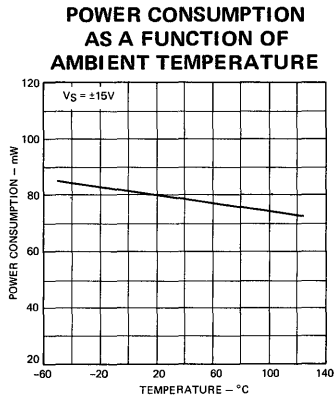
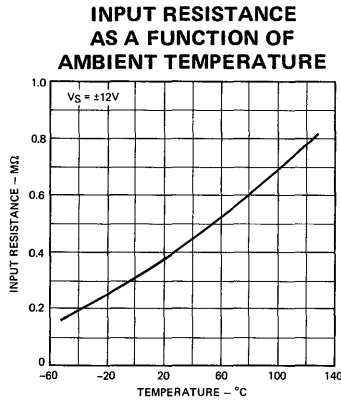
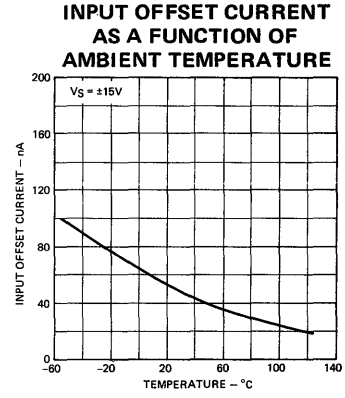
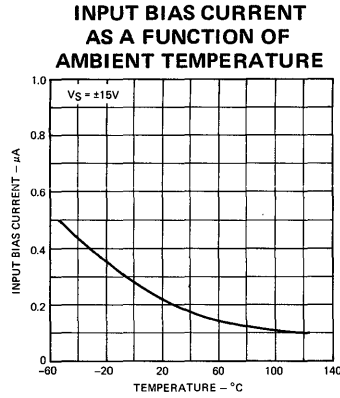
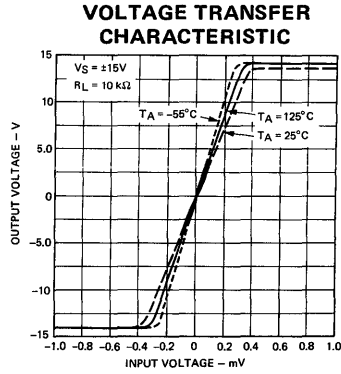


Pin numbers only apply to metal can package.

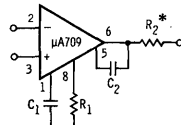
SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



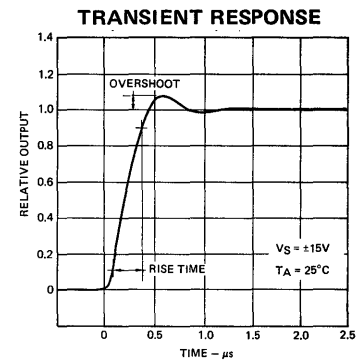
TYPICAL PERFORMANCE CURVES FOR 709 AND 709C



FREQUENCY COMPENSATION CIRCUIT

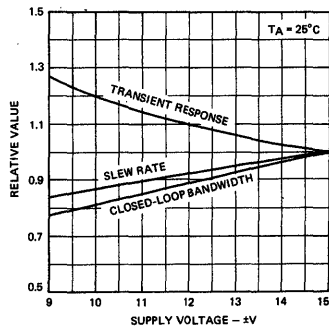


* Use $R_2 = 50 \Omega$ when the amplifier is operated with capacitive loading.

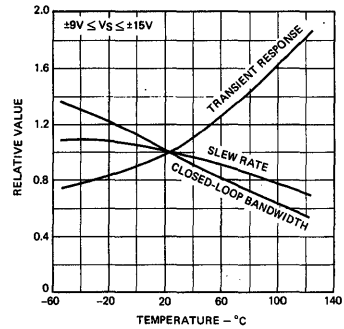


TYPICAL PERFORMANCE CURVES FOR 709 AND 709C

FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

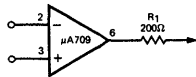


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

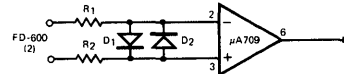


PROTECTION CIRCUITS

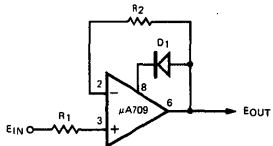
OUTPUT SHORT-CIRCUIT PROTECTION



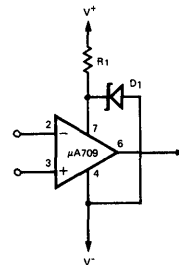
INPUT BREAKDOWN PROTECTION



LATCH-UP PROTECTION



SUPPLY OVERVOLTAGE PROTECTION



Pin numbers only apply to metal can package.

μA715

HIGH SPEED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

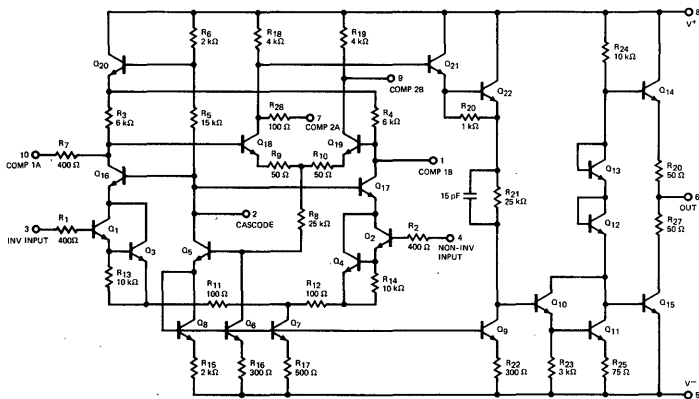
GENERAL DESCRIPTION — The μA715 is a High Speed, High Gain, monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The μA715 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The μA715 is ideally suited for use in A to D and D to A converters, active filters, deflection amplifiers, video amplifiers, phase locked loops, multiplexed analog gates, precision comparators, sample and holds, and general feedback applications requiring dc wide bandwidth operation.

- HIGH SLEW RATE 100 V/μs
- FAST SETTLING TIME 300 ns
- WIDE BANDWIDTH 65 MHz
- WIDE OPERATING SUPPLY RANGE
- WIDE INPUT VOLTAGE RANGES

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	±15 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP	-65°C to +150°C
Operating Temperature Range	
Military (715)	-55°C to +125°C
Commercial (715C)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can, DIP	300°C

EQUIVALENT CIRCUIT

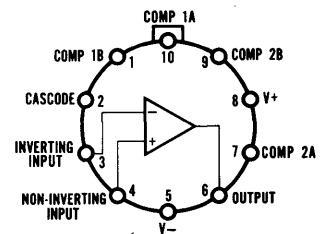


All Pin numbers shown refer to 10-lead TO-5 package

Notes on following pages.

CONNECTION DIAGRAMS

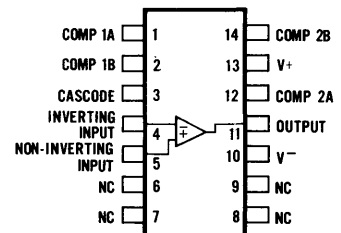
**10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F**



ORDER INFORMATION

TYPE	PART NO.
715	715HM
715C	715HC

**14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A**



ORDER INFORMATION

TYPE	PART NO.
715	715DM
715C	715DC

*Planar is a patented Fairchild process.

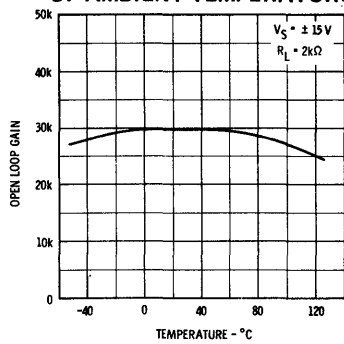
FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A715

ELECTRICAL CHARACTERISTICS FOR 715 ($V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$ unless otherwise specified)

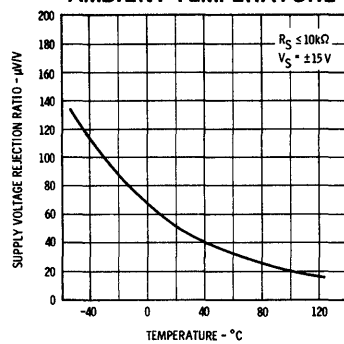
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ k Ω		2.0	5.0	mV
Input Offset Current			70	250	nA
Input Bias Current			400	750	nA
Input Resistance			1.0		M Ω
Input Voltage Range		± 10	± 12		V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	15,000	30,000		
Output Resistance			75		Ω
Supply Current			5.5	7.0	mA
Power Consumption			165	210	mW
Acquisition Time (Unity Gain)	$V_{OUT} = +5$ V		800		ns
Settling Time (Unit Gain)			300		ns
Transient Response (Unity Gain)	$V_{IN} = 400$ mV		30	60	ns
		Risetime		25	40
Slew Rate	$A_v = 100$		70		V/ μ s
	$A_v = 10$		38		V/ μ s
	$A_v = 1$ (non-inverting)	15	18		V/ μ s
	$A_v = 1$ (inverting)		100		V/ μ s
The following apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$:					
Input Offset Voltage	$R_S \leq 10$ k Ω			7.5	mV
Input Offset Current	$T_A = +125^\circ\text{C}$			250	nA
	$T_A = -55^\circ\text{C}$			800	nA
Input Bias Current	$T_A = +125^\circ\text{C}$			750	nA
	$T_A = -55^\circ\text{C}$			4.0	μ A
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ k Ω		45	300	μ V/V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	10,000			
Output Voltage Swing	$R_L \geq 2$ k Ω	± 10	± 13		

TYPICAL PERFORMANCE CURVES FOR 715

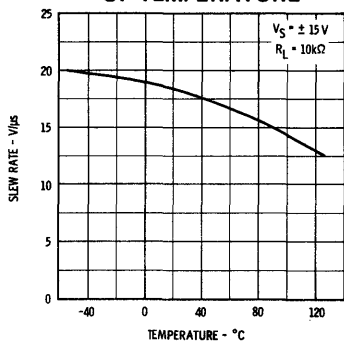
OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



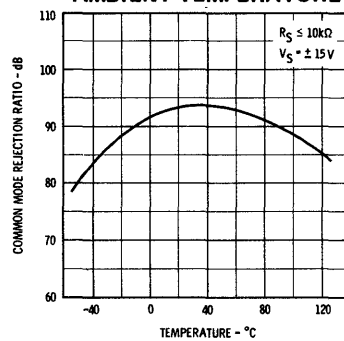
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



SLEW RATE AS A FUNCTION OF TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



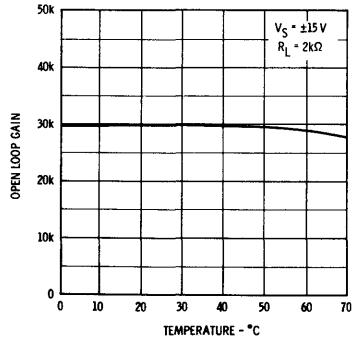
FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A715$

ELECTRICAL CHARACTERISTICS FOR 715C ($V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$ unless otherwise specified)

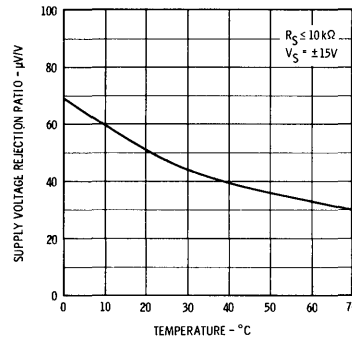
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ k Ω		2.0	7.5	mV
Input Offset Current			70	250	nA
Input Bias Current			0.4	1.5	μA
Input Resistance			1.0		M Ω
Input Voltage Range		± 10	± 12		V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ k Ω		45	400	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{\text{OUT}} = \pm 10$ V	10,000	30,000		
Output Resistance			75		Ω
Supply Current			5.5	10	mA
Power Consumption			165	300	mW
Acquisition Time (Unity Gain)	$V_{\text{OUT}} = +5$ V		800		ns
Settling Time (Unity Gain)			300		ns
Transient Response (Unity Gain)	Risetime	$V_{\text{IN}} = 400$ mV	30	75	ns
	Overshoot		25	50	%
Slew Rate		$A_v = 100$	70		V/ μs
		$A_v = 10$	38		V/ μs
		$A_v = 1$ (non-inverting)	10	18	V/ μs
		$A_v = 1$ (inverting)		100	V/ μs
The following apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$:					
Input Offset Voltage	$R_S \leq 10$ k Ω			10	mV
Input Offset Current	$T_A = +70^\circ\text{C}$			250	nA
	$T_A = 0^\circ\text{C}$			750	nA
Input Bias Current	$T_A = +70^\circ\text{C}$			1.5	μA
	$T_A = 0^\circ\text{C}$			7.5	μA
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{\text{OUT}} = \pm 10$ V	8,000			
Output Voltage Swing	$R_L \geq 2$ k Ω	± 10	± 13		V

TYPICAL PERFORMANCE CURVES FOR 715C

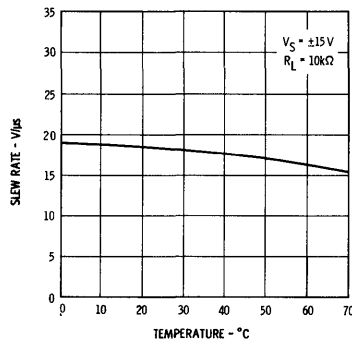
OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



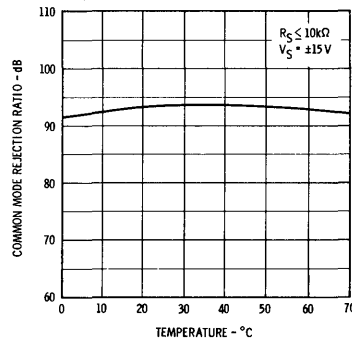
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



SLEW RATE AS A FUNCTION OF TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



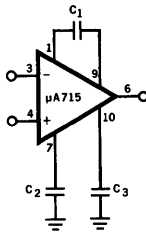
TYPICAL PERFORMANCE CURVES FOR 715 AND 715C

NON-INVERTING COMPENSATION COMPONENTS VALUES

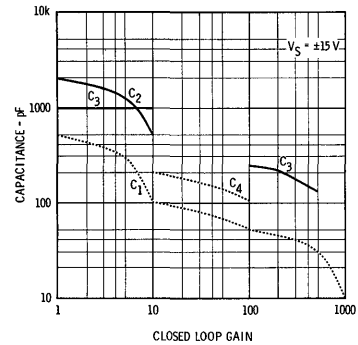
CLOSED LOOP GAIN	C_1	C_2	C_3
1000	10 pF	—	—
100	50 pF	—	250 pF
10 *	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

*For Gain 10, compensation may be simplified by removing C_2 , C_3 and adding a 200 pF capacitor (C_4) between Pin 7 and 10.

FREQUENCY COMPENSATION CIRCUIT

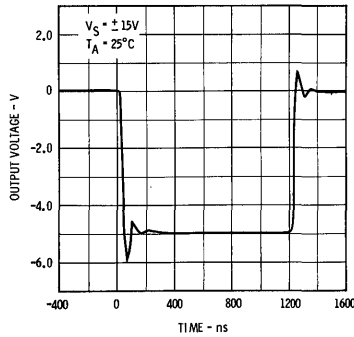


SUGGESTED VALUES OF COMPENSATION CAPACITORS AS A FUNCTION OF THE CLOSED LOOP GAIN

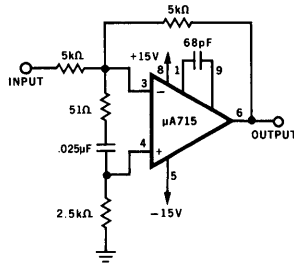


INVERTING UNITY GAIN

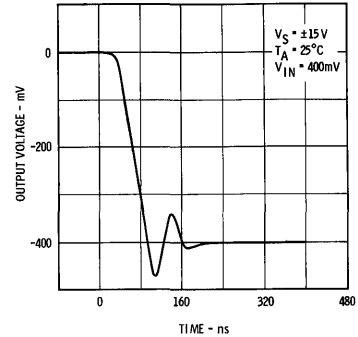
LARGE SIGNAL PULSE RESPONSE



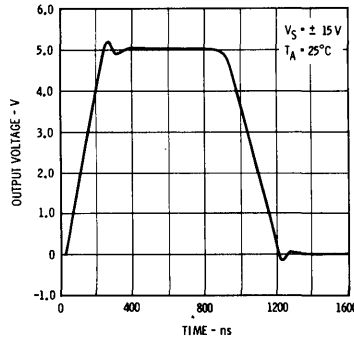
HIGH SLEW RATE CIRCUIT



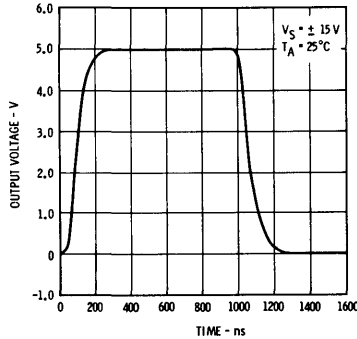
SMALL SIGNAL PULSE RESPONSE INVERTING UNITY GAIN



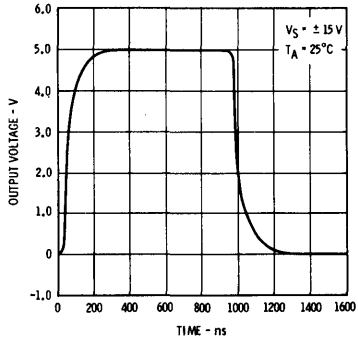
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



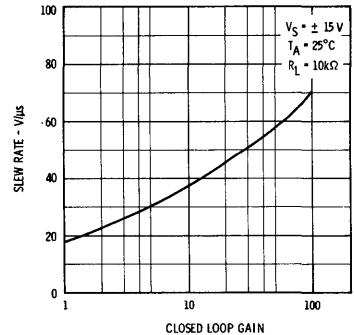
LARGE SIGNAL PULSE RESPONSE FOR GAIN 10



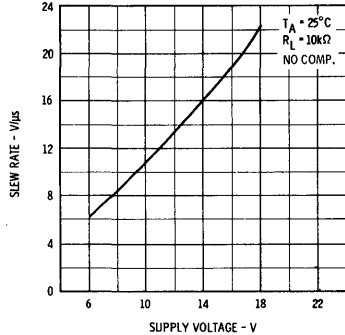
LARGE SIGNAL PULSE RESPONSE FOR GAIN 100



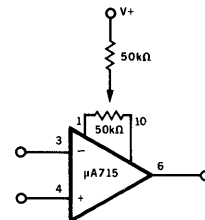
SLEW RATE AS A FUNCTION OF THE CLOSED LOOP GAIN



SLEW RATE AS A FUNCTION OF SUPPLY VOLTAGE

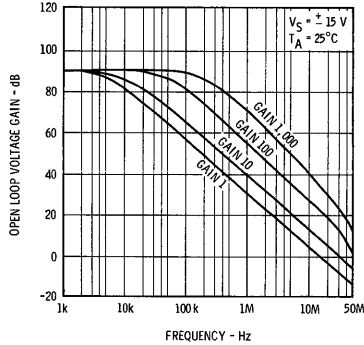


VOLTAGE OFFSET NULL CIRCUIT

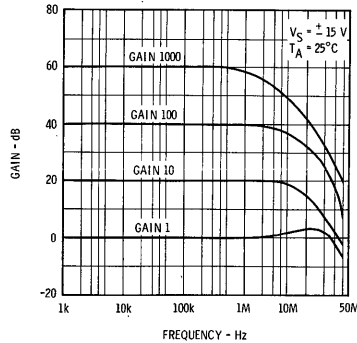


TYPICAL PERFORMANCE CURVES FOR 715 AND 715C

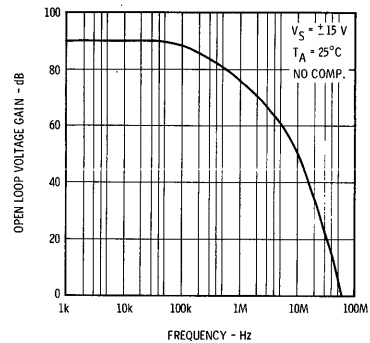
OPEN LOOP RESPONSE WITH COMPENSATION NECESSARY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



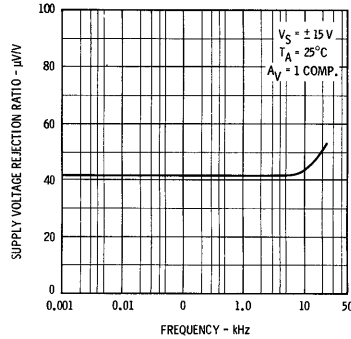
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



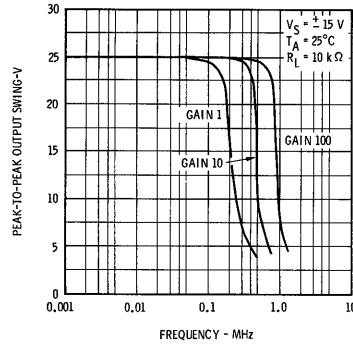
OPEN LOOP GAIN AS A FUNCTION OF FREQUENCY



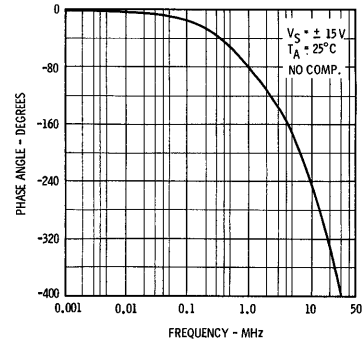
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF FREQUENCY



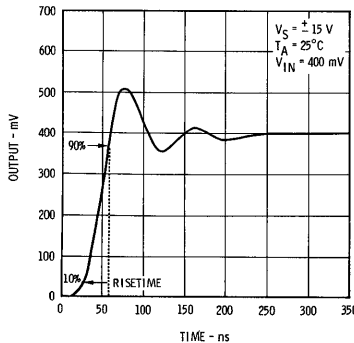
OUTPUT SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



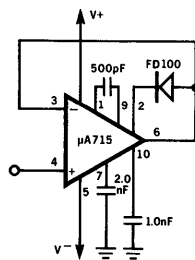
OPEN LOOP PHASE AS A FUNCTION OF FREQUENCY



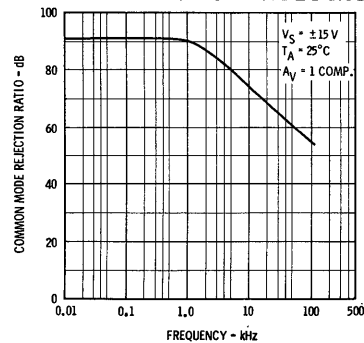
VOLTAGE FOLLOWER TRANSIENT RESPONSE



VOLTAGE FOLLOWER



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

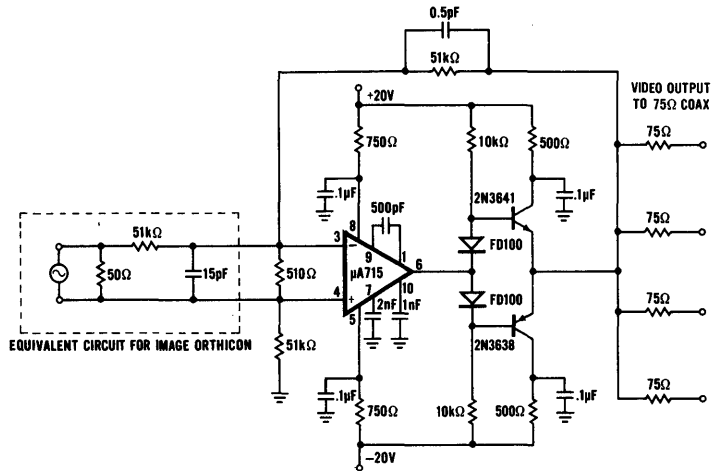
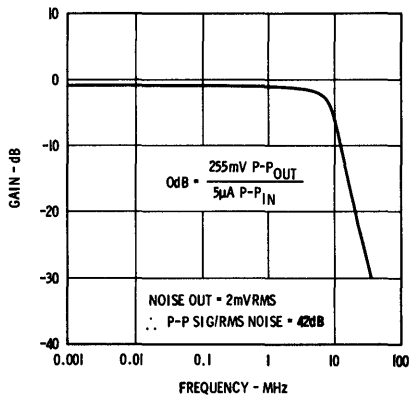


NOTES

1. Rating applies to ambient temperature up to $70^\circ C$. Above $70^\circ C$ ambient derate linearly at $6.3 mW/^\circ C$ for Metal Can and $8.3 mW/^\circ C$ for the DIP.
2. For supply voltages less than $\pm 15 V$, the absolute maximum input voltage is equal to the supply voltage.

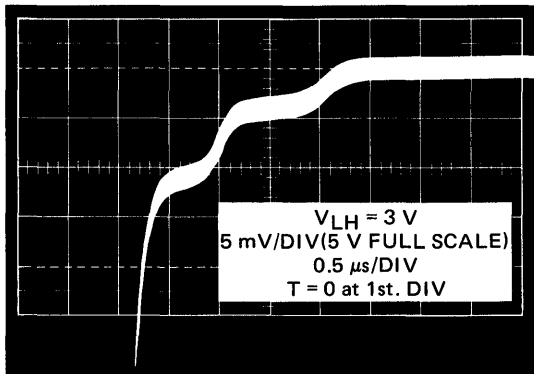
TYPICAL APPLICATIONS

WIDE BAND VIDEO AMPLIFIER WITH 75 Ω COAX CABLE DRIVE CAPABILITY

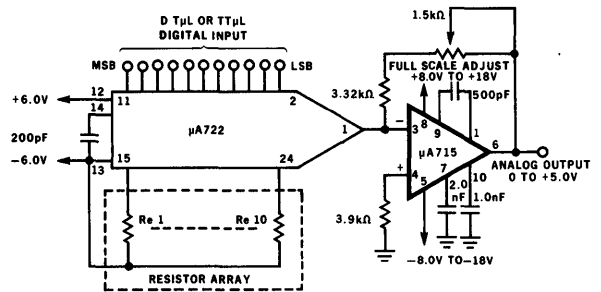


HIGH SPEED 10-BIT DIGITAL TO ANALOG CONVERTER

ANALOG OUTPUT 0 TO +5.0 V



μ A722/ μ A715 op amp switching ON, as it should with typical logic voltage on least significant bits. Note complete absence of ringing.

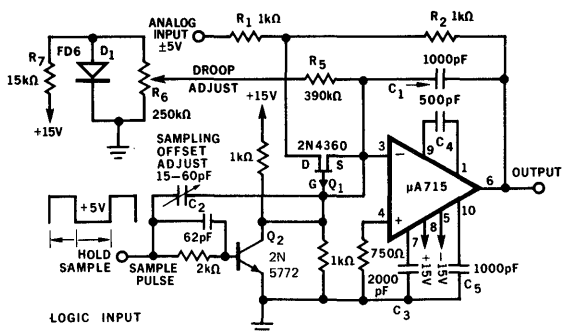


Conversion Rate
 6 bits - 300 ns
 8 bits - 600 ns
 10 bits - 1000 ns

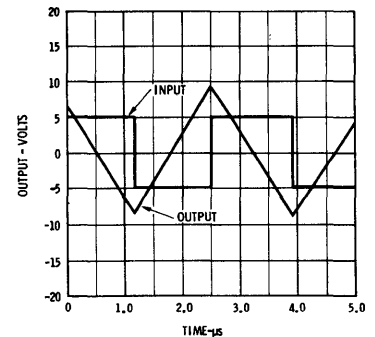
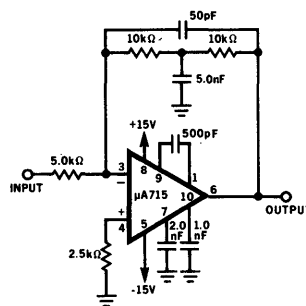
NOTE:

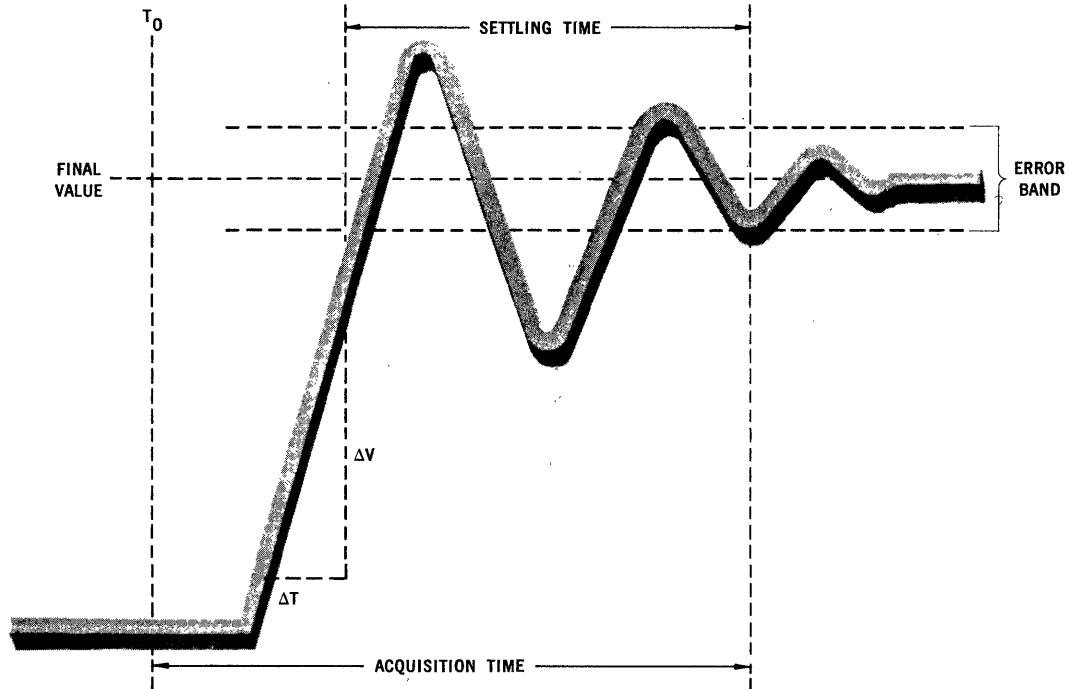
Contact Fairchild for additional information including how to increase conversion speed by clamping LSB's and how to obtain bipolar outputs.

HIGH SPEED SAMPLE AND HOLD



HIGH SPEED INTEGRATOR





HELPFUL HINTS

LAYOUT — The layout should be such that stray capacitance is minimal.

SUPPLIES — The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.

RINGING — Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100 Ω . Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.

LATCH UP — This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between pins 6 and 2 with the cathode towards pin 2 is the recommended preventive.

μA725

INSTRUMENTATION OPERATIONAL AMPLIFIER

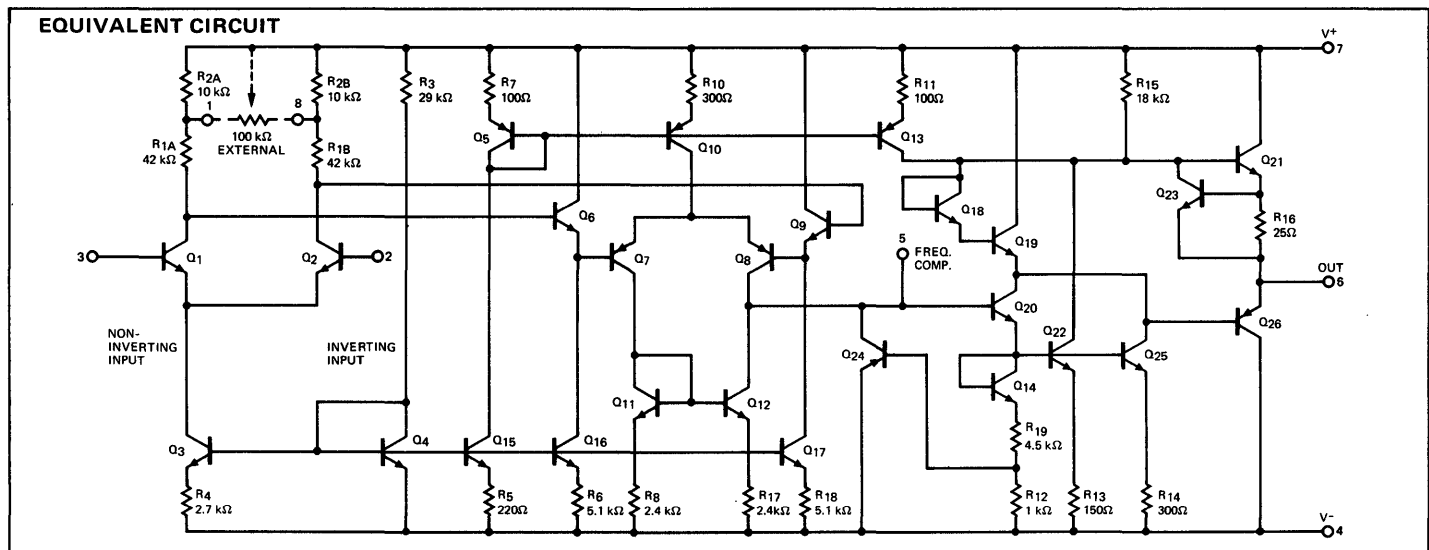
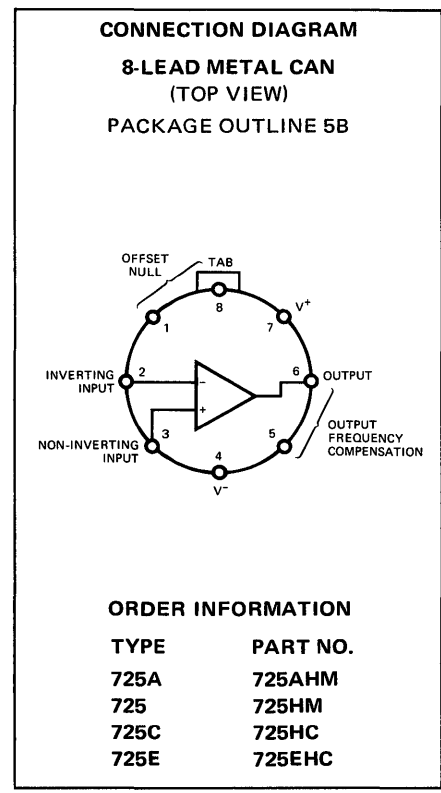
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA715 is a monolithic Instrumentation Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA715 is pin compatible with the popular μA741 operational amplifier.

- **LOW INPUT NOISE CURRENT** $0.15 \text{ pA} \sqrt{\text{Hz}}$
- **HIGH OPEN LOOP GAIN** **3,000,000**
- **LOW INPUT OFFSET CURRENT** **2 nA**
- **LOW INPUT VOLTAGE DRIFT** $0.6 \text{ } \mu\text{V}/^\circ\text{C}$
- **HIGH COMMON MODE REJECTION** **120 dB**
- **HIGH INPUT VOLTAGE RANGE** $\pm 14 \text{ V}$
- **WIDE POWER SUPPLY RANGE** $\pm 3 \text{ V TO } \pm 22 \text{ V}$
- **OFFSET NULL CAPABILITY**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±22 V
Voltage Between Offset Null and V ⁺	±0.5 V
Storage Temperature Range	
Metal Can	−65° C to +150° C
Operating Temperature Range	
Military (725A, 725)	−55° C to +125° C
Commercial (725E, 725C)	0° C to +70° C
Lead Temperature	
Metal Can (Soldering, 60 Seconds)	300° C



Notes on following pages

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A725

725A

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25^\circ$ C unless otherwise specified)

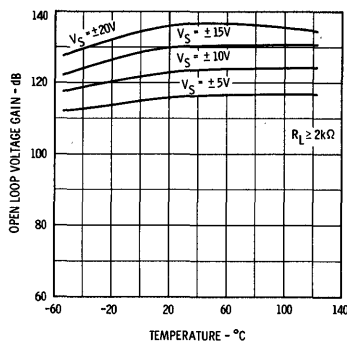
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ k Ω			0.5	mV
Input Offset Current				5.0	nA
Input Bias Current				75	nA
Input Noise Voltage	$f_o = 10$ Hz			15	nV/ $\sqrt{\text{Hz}}$
	$f_o = 100$ Hz			9.0	nV/ $\sqrt{\text{Hz}}$
	$f_o = 1$ kHz			7.5	nV/ $\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10$ Hz			1.2	pA/ $\sqrt{\text{Hz}}$
	$f_o = 100$ Hz			0.6	pA/ $\sqrt{\text{Hz}}$
	$f_o = 1$ kHz			0.25	pA/ $\sqrt{\text{Hz}}$
Input Resistance			1.5		M Ω
Input Voltage Range		± 13.5	± 14		V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	1,000,000	3,000,000		V/V
	$R_L \geq 500$ Ω , $V_{OUT} = \pm 0.5$ V, $V_S = \pm 3$ V	100,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	120	130		dB
Power Supply Rejection Ratio	$R_S \leq 10$ k Ω		2.0	5.0	μ V/V
Output Voltage Swing	$R_L \geq 10$ k Ω	± 12.5			V
	$R_L \geq 2$ k Ω	± 10			V
Output Resistance			150		Ω
Power Consumption			80	120	mW
	$V_S = \pm 3$ V			6.0	mW

The following specifications apply for -55° C $\leq T_A \leq +125^\circ$ C unless otherwise specified:

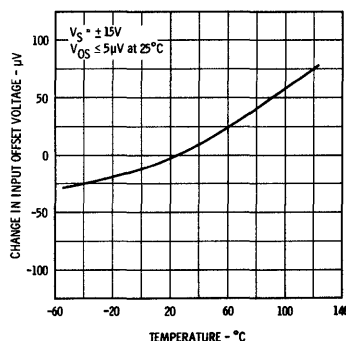
Input Offset Voltage (Without External trim)	$R_S \leq 10$ k Ω			0.75	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50$ Ω			2.0	μ V/ $^\circ$ C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50$ Ω		0.6	1.0	μ V/ $^\circ$ C
Input Offset Current	$T_A = +125^\circ$ C			4.0	nA
	$T_A = -55^\circ$ C		5.0	18	nA
Average Input Offset Current Drift				90	pA/ $^\circ$ C
Input Bias Current	$T_A = +125^\circ$ C			70	nA
	$T_A = -55^\circ$ C			180	nA
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $T_A = +125^\circ$ C	1,000,000			V/V
	$R_L \geq 2$ k Ω , $T_A = -55^\circ$ C	500,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	110			dB
Power Supply Rejection Ratio	$R_S \leq 10$ k Ω			8.0	μ V/V
Output Voltage Swing	$R_L \geq 2$ k Ω	± 10			V

TYPICAL PERFORMANCE CURVES FOR 725A AND 725

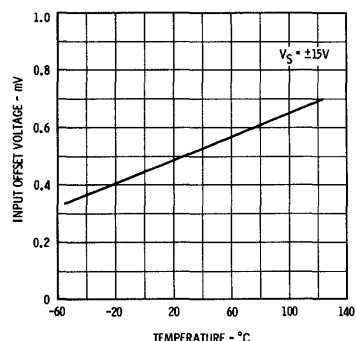
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A725

725

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ k Ω		0.5	1.0	mV
Input Offset Current			2.0	20	nA
Input Bias Current			42	100	nA
Input Noise Voltage	$f_o = 10$ Hz		15		nV/ $\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		9.0		nV/ $\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		8.0		nV/ $\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10$ Hz		1.0		pA/ $\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		0.3		pA/ $\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		0.15		pA/ $\sqrt{\text{Hz}}$
Input Resistance			1.5		M Ω
Input Voltage Range		± 13.5	± 14		V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	1,000,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	110	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ k Ω		2.0	10	$\mu\text{V/V}$
Output Voltage Swing	$R_L \geq 10$ k Ω	± 12	± 13.5		V
	$R_L \geq 2$ k Ω	± 10	± 13.5		V
Output Resistance			150		Ω
Power Consumption			80	105	mW

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ unless otherwise specified:

Input Offset Voltage (Without external trim)	$R_S \leq 10$ k Ω			1.5	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50\Omega$		2.0	5.0	$\mu\text{V}/^\circ\text{C}$
Average Input Offset Voltage Drift (With external trim)	$R_S = 50\Omega$		0.6		$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$T_A = +125^\circ\text{C}$		1.2	20	nA
	$T_A = -55^\circ\text{C}$		7.5	40	nA
Average Input Offset Current Drift			35	150	pA/ $^\circ\text{C}$
Input Bias Current	$T_A = +125^\circ\text{C}$		20	100	nA
	$T_A = -55^\circ\text{C}$		80	200	nA
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $T_A = +125^\circ\text{C}$	1,000,000			V/V
	$R_L \geq 2$ k Ω , $T_A = -55^\circ\text{C}$	250,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	100			dB
Power Supply Rejection Ratio	$R_S \leq 10$ k Ω			20	$\mu\text{V/V}$
Output Voltage Swing	$R_L \geq 2$ k Ω	± 10			V

NOTES:

- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at 6.3 mW/ $^\circ\text{C}$.
- For supply voltages less than ± 22 V, the absolute maximum input voltage is equal to the supply voltage.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A725

725E

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25^\circ$ C unless otherwise specified)

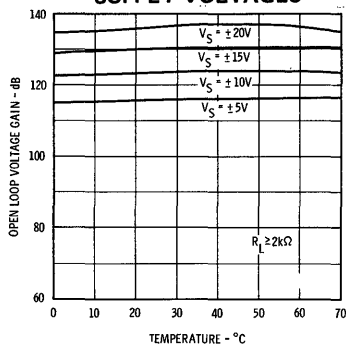
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ k Ω			0.5	mV
Input Offset Current				5.0	nA
Input Bias Current				75	nA
Input Noise Voltage	$f_o = 10$ Hz			15	nV/ $\sqrt{\text{Hz}}$
	$f_o = 100$ Hz			9.0	nV/ $\sqrt{\text{Hz}}$
	$f_o = 1$ kHz			7.5	nV/ $\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10$ Hz			1.2	pA/ $\sqrt{\text{Hz}}$
	$f_o = 100$ Hz			0.6	pA/ $\sqrt{\text{Hz}}$
	$f_o = 1$ kHz			0.25	pA/ $\sqrt{\text{Hz}}$
Input Resistance			1.5	M Ω	
Input Voltage Range		± 13.5	± 14		V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	1,000,000	3,000,000		V/V
	$R_L \geq 500$ Ω , $V_{OUT} = \pm 0.5$ V $V_S = \pm 3$ V	100,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	120			dB
Power Supply Rejection Ratio	$R_S \leq 10$ k Ω		2.0	5.0	μ V/V
Output Voltage Swing	$R_L \geq 10$ k Ω	± 12.5			V
	$R_L \geq 2$ k Ω	± 10			V
Output Resistance			150		Ω
Power Consumption			80	150	mW
	$V_S = \pm 3$ V			6.0	mW

The following specifications apply for 0° C $\leq T_A \leq +70^\circ$ C unless otherwise specified:

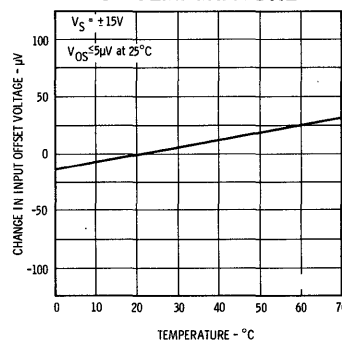
Input Offset Voltage (Without external trim)	$R_S \leq 10$ k Ω			0.75	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50$ Ω			2.0	μ V/ $^\circ$ C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50$ Ω			1.0	μ V/ $^\circ$ C
Input Offset Current	$T_A = +70^\circ$ C		1.2	4.0	nA
	$T_A = 0^\circ$ C		4.0	18	nA
Average Input Offset Current Drift			10	90	pA/ $^\circ$ C
Input Bias Current	$T_A = +70^\circ$ C			70	nA
	$T_A = 0^\circ$ C			180	nA
Large Signal Voltage	$R_L \geq 2$ k Ω , $T_A = +70^\circ$ C	1,000,000			V/V
	$R_L \geq 2$ k Ω , $T_A = 0^\circ$ C	500,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	110			dB
Power Supply Rejection Ratio	$R_S \leq 10$ k Ω			8.0	μ V/V
Output Voltage Swing	$R_L \geq 2$ k Ω	± 10			V

TYPICAL PERFORMANCE CURVES FOR 725E AND 725C

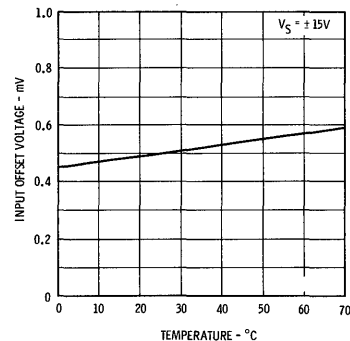
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A725

725C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25^\circ$ C unless otherwise specified)

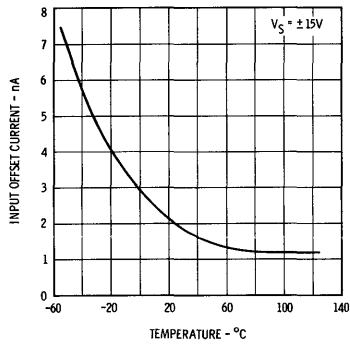
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ k Ω		0.5	2.5	mV
Input Offset Current			2.0	35	nA
Input Bias Current			42	125	nA
Input Noise Voltage	$f_o = 10$ Hz		15		nV/ $\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		9.0		nV/ $\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		8.0		nV/ $\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10$ Hz		1.0		pA/ $\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		0.3		pA/ $\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		0.15		pA/ $\sqrt{\text{Hz}}$
Input Resistance			1.5		M Ω
Input Voltage Range		± 13.5	± 14		V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	250,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	94	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ k Ω		2.0	35	μ V/V
Output Voltage Swing	$R_L \geq 10$ k Ω	± 12	± 13.5		V
	$R_L \geq 2$ k Ω	± 10	± 13.5		V
Output Resistance			150		Ω
Power Consumption			80	150	mW

The following specifications apply for 0° C $\leq T_A \leq +70^\circ$ C unless otherwise specified:

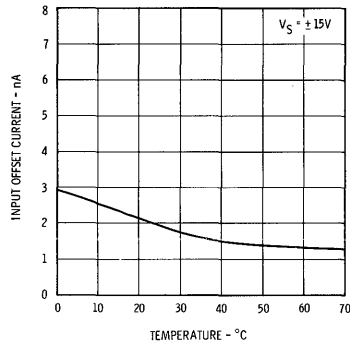
Input Offset Voltage (Without external trim)	$R_S \leq 10$ k Ω			3.5	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50$ Ω		2.0		μ V/ $^\circ$ C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50$ Ω		0.6		μ V/ $^\circ$ C
Input Offset Current	$T_A = +70^\circ$ C		1.2	35	nA
	$T_A = 0^\circ$ C		4.0	50	nA
Average Input Offset Current Drift			10		pA/ $^\circ$ C
Input Bias Current	$T_A = +70^\circ$ C			125	nA
	$T_A = 0^\circ$ C			250	nA
Large Signal Voltage	$R_L \geq 2$ k Ω , $T_A = +70^\circ$	125,000			V/V
	$R_L \geq 2$ k Ω , $T_A = 0^\circ$ C	125,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω		115		dB
Power Supply Rejection Ratio	$R_S \leq 10$ k Ω		20		μ V/V
Output Voltage Swing	$R_L \geq 2$ k Ω	± 10			V

TYPICAL PERFORMANCE CURVES FOR ALL TYPES (Unless Otherwise Specified)

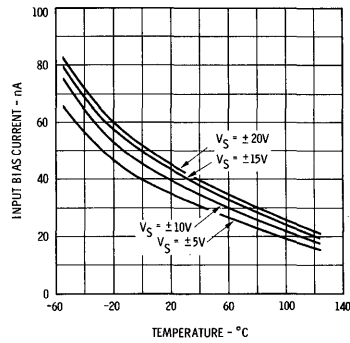
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE
725A AND 725



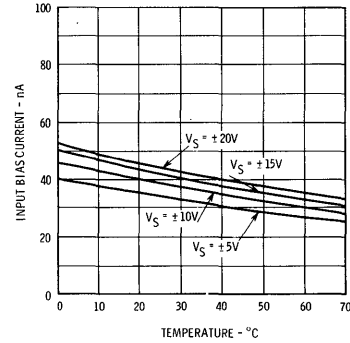
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE
725C AND 725E



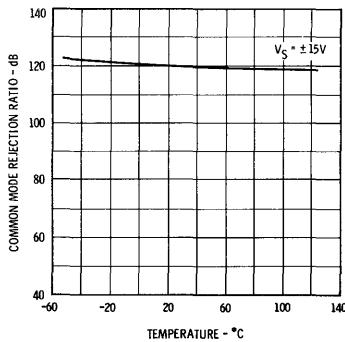
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE
725A AND 725



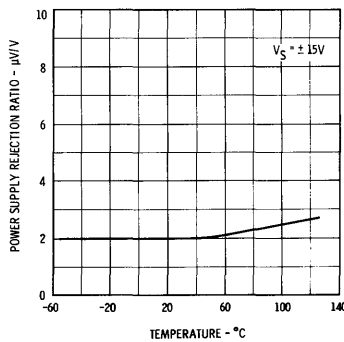
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE
725C AND 725E



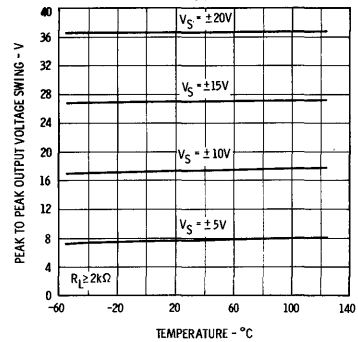
COMMON MODE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



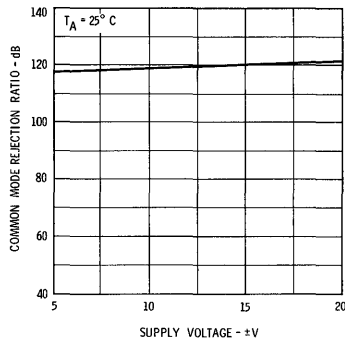
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



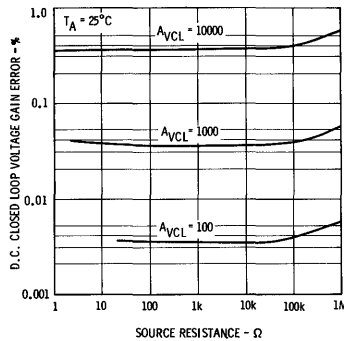
OUTPUT VOLTAGE SWING AS A FUNCTION OF TEMPERATURE



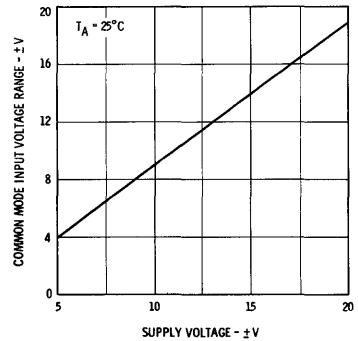
COMMON MODE REJECTION RATIO AS A FUNCTION OF SUPPLY VOLTAGE



D.C. CLOSED LOOP VOLTAGE GAIN ERROR AS A FUNCTION OF SOURCE RESISTANCE

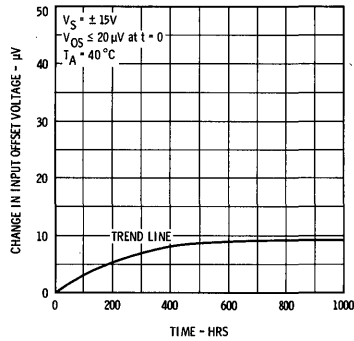


COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

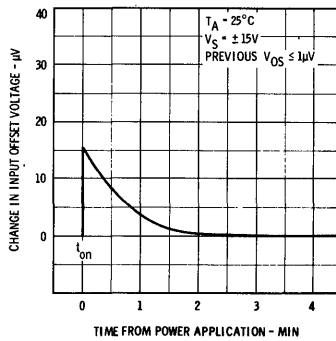


TYPICAL PERFORMANCE CURVES FOR ALL TYPES (Unless Otherwise Specified)

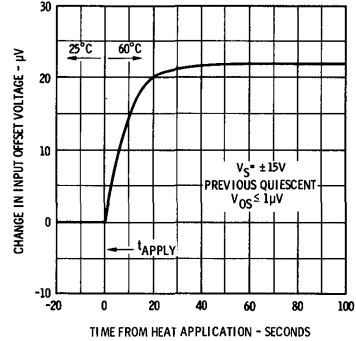
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



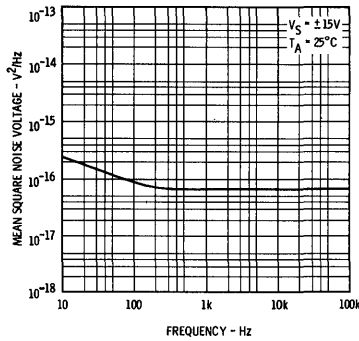
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



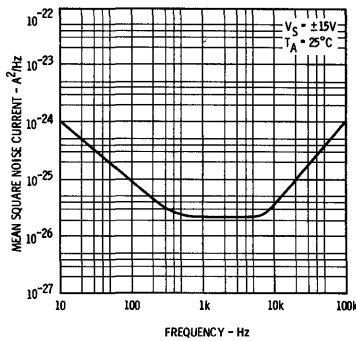
CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK AS A FUNCTION OF TIME



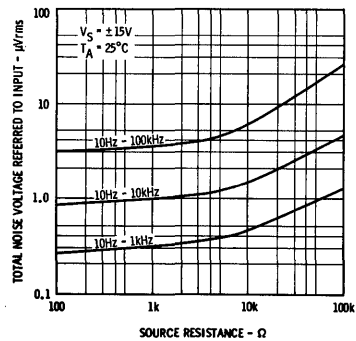
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



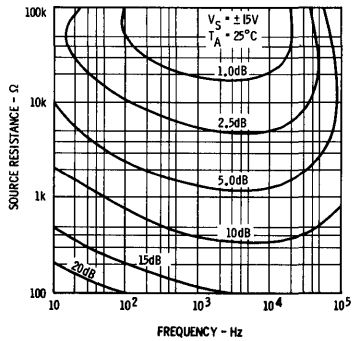
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



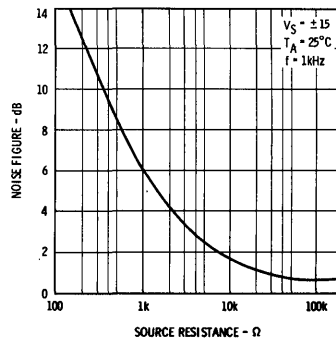
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



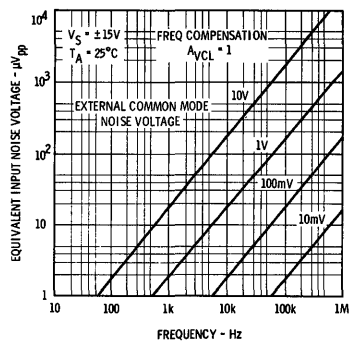
NARROW BAND SPOT NOISE FIGURE CONTOURS



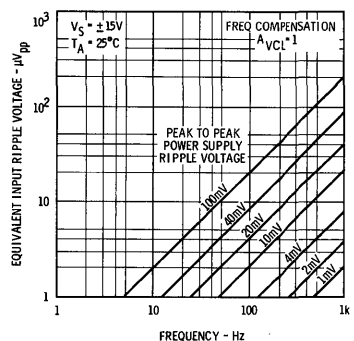
NOISE FIGURE AS A FUNCTION OF SOURCE RESISTANCE



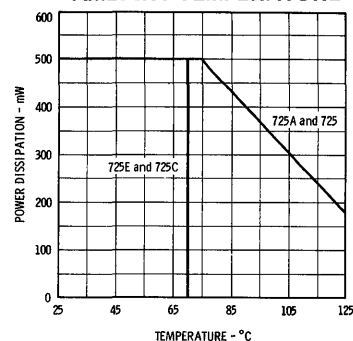
EQUIVALENT INPUT NOISE VOLTAGE DUE TO EXTERNAL COMMON MODE NOISE AS A FUNCTION OF FREQUENCY



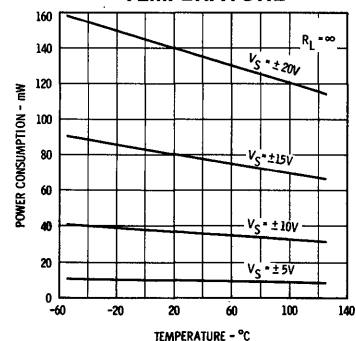
EQUIVALENT INPUT RIPPLE VOLTAGE DUE TO POWER SUPPLY RIPPLE AS A FUNCTION OF FREQUENCY



ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

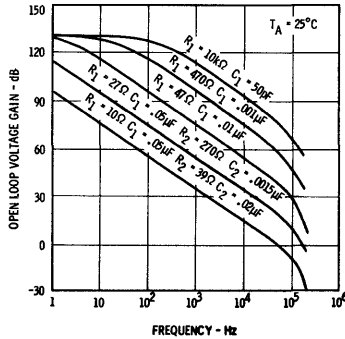


POWER CONSUMPTION AS A FUNCTION OF TEMPERATURE

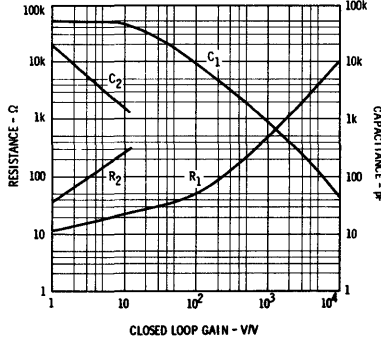


TYPICAL PERFORMANCE CURVES FOR ALL TYPES

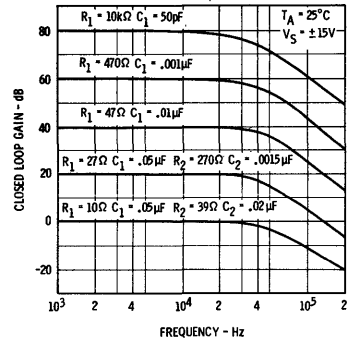
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY USING RECOMMENDED COMPENSATION NETWORKS



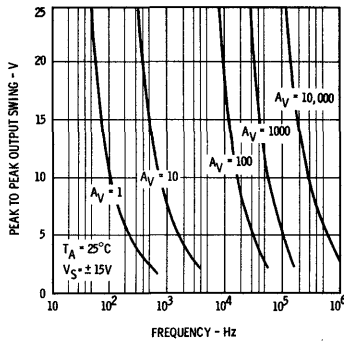
VALUES FOR SUGGESTED COMPENSATION NETWORKS FOR VARIOUS CLOSED LOOP VOLTAGE GAINS



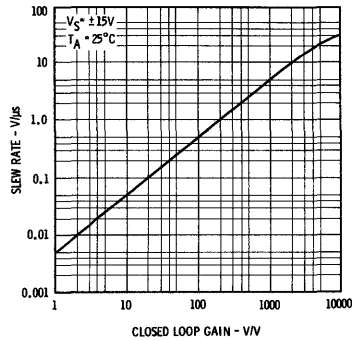
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS USING RECOMMENDED COMPENSATION NETWORKS



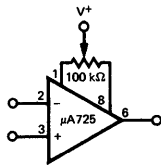
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR RECOMMENDED COMPENSATION NETWORKS



SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



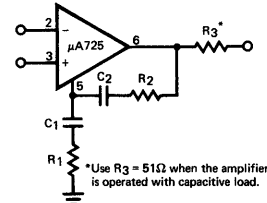
VOLTAGE OFFSET NULL CIRCUIT



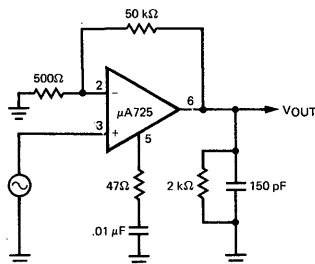
COMPENSATION COMPONENT VALUES

A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	—	—
1,000	470	.001	—	—
100	47	.01	—	—
10	27	.05	270	.0015
1	10	.05	39	.02

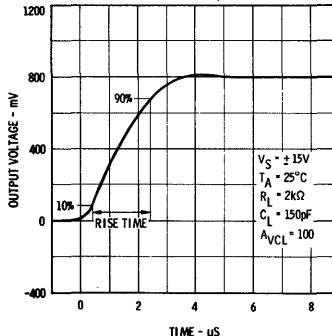
FREQUENCY COMPENSATION CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



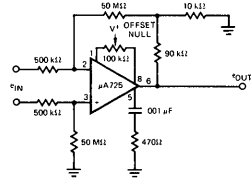
TRANSIENT RESPONSE



Pin numbers are shown for Metal Can only.

TYPICAL APPLICATIONS

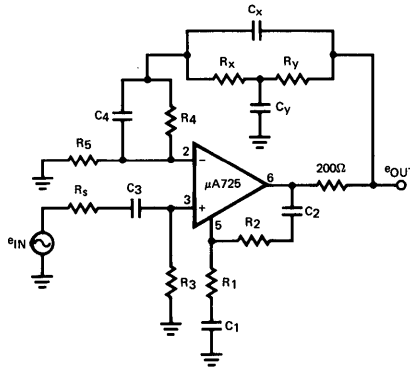
PRECISION AMPLIFIER - $A_{VCL} = 1000$



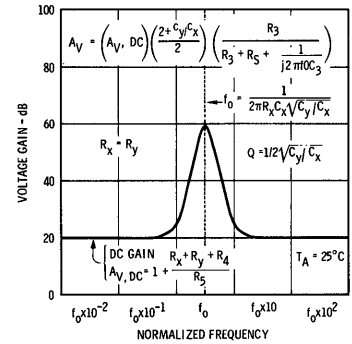
CHARACTERISTICS:

- $A_V = 1000 = 60 \text{ dB}$
- DC Gain Error = 0.05%
- Bandwidth = 1 kHz for -0.05% error
- Diff. Input Res. = 1 MΩ
- Typical amplifying capability
- $e_{IN} = 10 \mu\text{V}$ on $V_{CM1} = 1.0 \text{ V}$
- Caution: Minimize Stray Capacitance

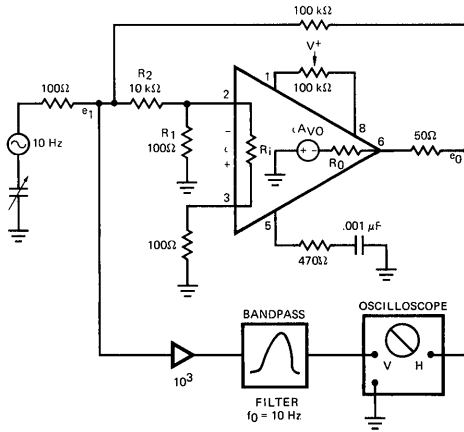
ACTIVE FILTER - BANDPASS WITH 60 dB GAIN



ACTIVE FILTER
FREQUENCY RESPONSE

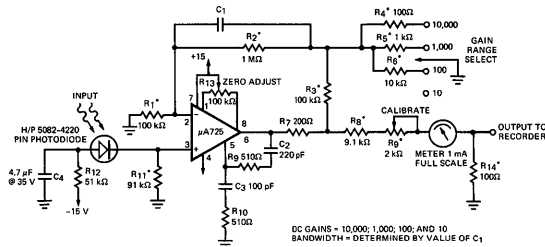


OPEN LOOP VOLTAGE GAIN TEST CIRCUIT



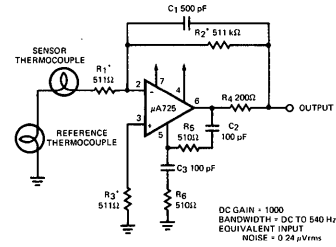
$$A_{VO} \approx \frac{e_0}{e_1} \left(\frac{R_2 R_i + R_1 R_i + R_1 R_2}{R_1 R_i} \right) = \frac{e_0}{e_1} 101$$

PIN PHOTODIODE AMPLIFIER



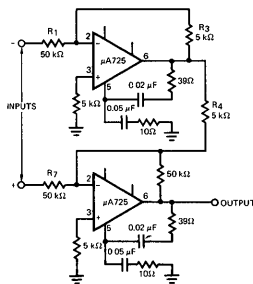
NOTE: * Indicates ±1% Metal film resistors recommended for temperature stability.

THERMOCOUPLE AMPLIFIER



NOTE: * Indicates ±1% metal film resistors recommended for temperature stability.

±100 V COMMON MODE RANGE
INSTRUMENTATION AMPLIFIER



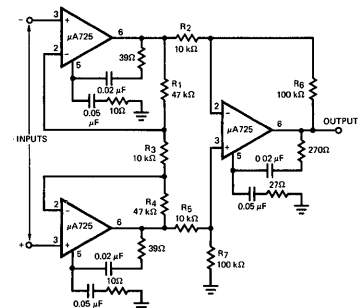
$$\frac{R_1}{R_7} = \frac{R_3}{R_4} \text{ for best CMRR}$$

$$R_3 = R_4$$

$$R_1 = R_6 = 10R_3$$

$$\text{Gain} = \frac{R_7}{R_6}$$

INSTRUMENTATION AMPLIFIER WITH
HIGH COMMON MODE REJECTION



$$\frac{R_2}{R_5} = \frac{R_6}{R_7} \text{ for best CMR}$$

$$R_1 = R_4$$

$$R_2 = R_5$$

$$\text{Gain} = \frac{R_6}{R_2} \left(1 + \frac{2R_1}{R_3} \right)$$

μA727

TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

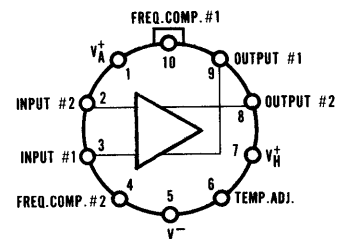
GENERAL DESCRIPTION — The μA727 is a monolithic, fixed gain, Differential-Input Differential-Output Amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gauge transducers, and A to D converters.

- VERY LOW OFFSET DRIFTS
- HIGH INPUT IMPEDANCE . . . 300 MΩ
- WIDE COMMON MODE RANGE . . . CMRR = 100 dB

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
Military (727)	-55°C to +125°C
Commercial (727C)	-20°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Internal Power Dissipation	500 mW
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

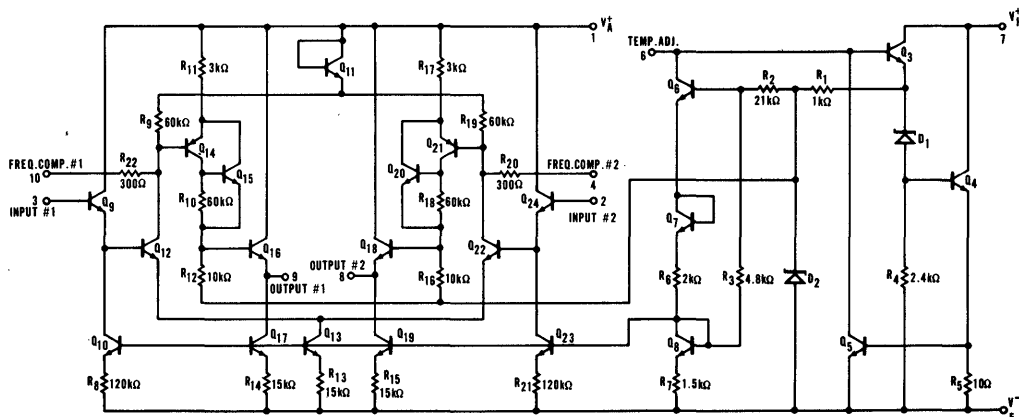
CONNECTION DIAGRAM
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5U



ORDER INFORMATION

TYPE	PART NO.
727	727HM
727C	727HC

EQUIVALENT CIRCUIT



* Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A727$

727

ELECTRICAL CHARACTERISTICS ($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $V_{H+} = V_{A+} = +15\text{ V}$, $V_- = -15\text{ V}$, $R_{ADJ} = 330\text{ k}\Omega$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\Omega$, $+25^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		0.6	1.5	$\mu\text{V}/^{\circ}\text{C}$
	$R_S \leq 50\Omega$, $-55^{\circ}\text{C} \leq T_A \leq +25^{\circ}\text{C}$		0.6	1.5	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current Drift	$+25^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		2.0		$\text{pA}/^{\circ}\text{C}$
	$-55^{\circ}\text{C} \leq T_A \leq +25^{\circ}\text{C}$		2.0		$\text{pA}/^{\circ}\text{C}$
Input Bias Current Drift	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		15		$\text{pA}/^{\circ}\text{C}$
Differential Input Resistance			300		$\text{M}\Omega$
Common Mode Input Resistance			1000		$\text{M}\Omega$
Input Voltage Range		± 12	± 13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\text{ k}\Omega$		80		$\mu\text{V}/\text{V}$
Common Mode Rejection Ratio	$R_S \leq 100\text{ k}\Omega$	80	100		dB
Output Resistance			1.0	4.0	$\text{k}\Omega$
Output Common Mode Voltage		-6.0	-5.0	-4.0	V
Differential Output Voltage Swing		± 5.0	± 7.0	± 10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	$\mu\text{V}/\mu\text{A}$
Differential Voltage Gain		60	100	250	
Low Frequency Noise	$\text{BW} = 10\text{ Hz to } 500\text{ Hz}$, $R_S \leq 50\Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\Omega$		5.0		$\mu\text{V}/\text{week}$
Amplifier Supply Current	$T_A = +25^{\circ}\text{C}$		1.0	2.0	mA
Heater Supply Current	$T_A = +25^{\circ}\text{C}$		10	15	mA

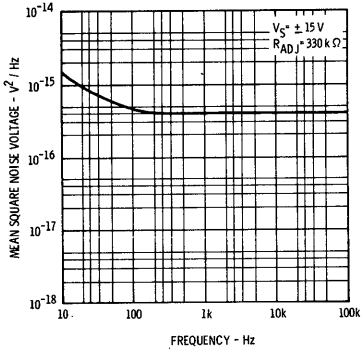
727C

ELECTRICAL CHARACTERISTICS ($-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $V_{H+} = V_{A+} = +15\text{ V}$, $V_- = -15\text{ V}$, $R_{ADJ} = 1\text{M}\Omega$, unless otherwise specified)

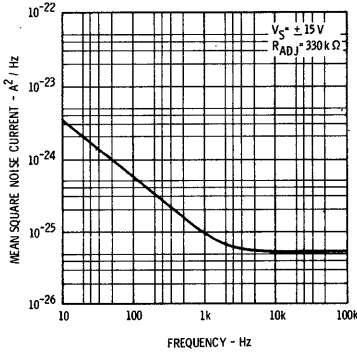
PARAMETER	CONDITONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	10	mV
Input Offset Current			2.5	25	nA
Input Bias Current			12	75	nA
Input Offset Voltage Drift	$R_S \leq 50\Omega$		0.6	3.0	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current Drift			2.0		$\text{pA}/^{\circ}\text{C}$
Input Bias Current Drift			15		$\text{pA}/^{\circ}\text{C}$
Differential Input Resistance			300		$\text{M}\Omega$
Common Mode Input Resistance			1000		$\text{M}\Omega$
Input Voltage Range		± 12	± 13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\text{ k}\Omega$		80		$\mu\text{V}/\text{V}$
Common Mode Rejection Ratio	$R_S \leq 100\text{ k}\Omega$	70	100		dB
Output Resistance			1.0	4.0	$\text{k}\Omega$
Output Common Mode Voltage		-7.0	-5.0	-4.0	V
Differential Output Voltage Swing		± 3.0	± 7.0	± 10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	15	$\mu\text{V}/\mu\text{A}$
Differential Voltage Gain		50	100	250	
Low Frequency Noise	$\text{BW} = 10\text{ Hz to } 500\text{ Hz}$, $R_S \leq 50\Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\Omega$		5.0		$\mu\text{V}/\text{week}$
Amplifier Supply Current	$T_A = +25^{\circ}\text{C}$		1.0	2.0	mA
Heater Supply Current	$T_A = +25^{\circ}\text{C}$		10	15	mA

TYPICAL PERFORMANCE CURVES FOR 727 AND 727C

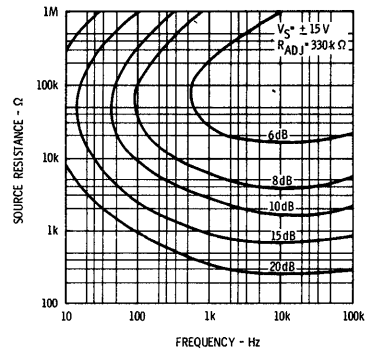
NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



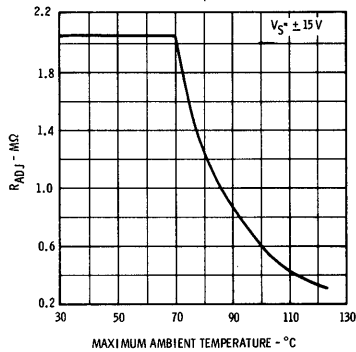
NOISE CURRENT AS A FUNCTION OF FREQUENCY



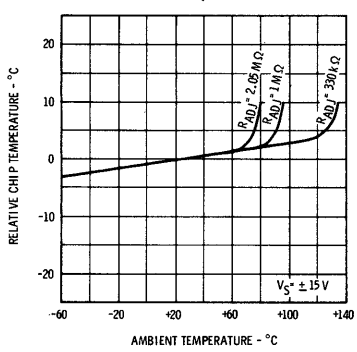
SPOT NOISE CONTOURS



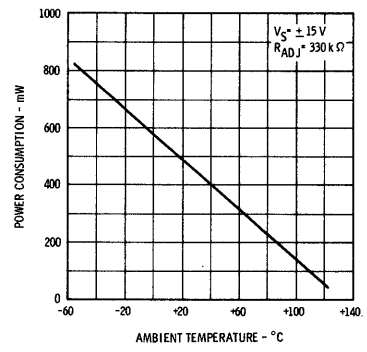
RECOMMENDED R_ADJ AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE



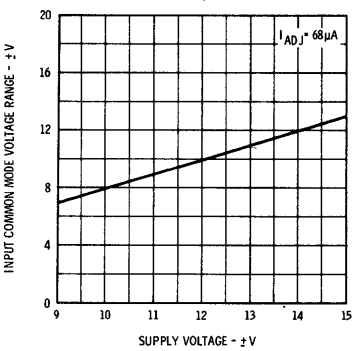
RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE



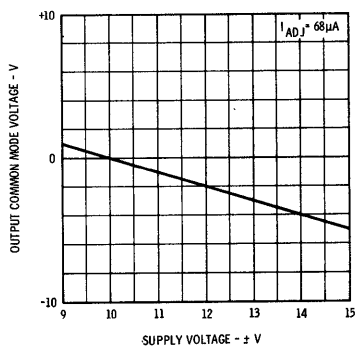
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



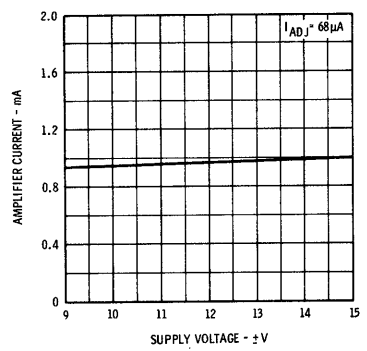
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



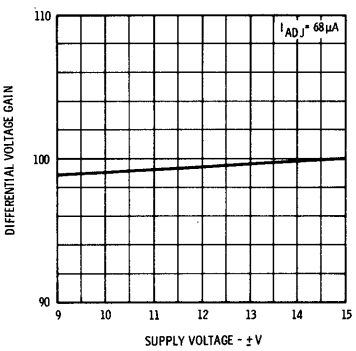
OUTPUT COMMON MODE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



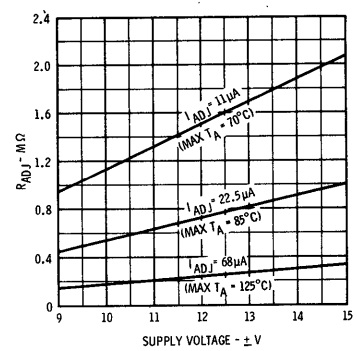
AMPLIFIER CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



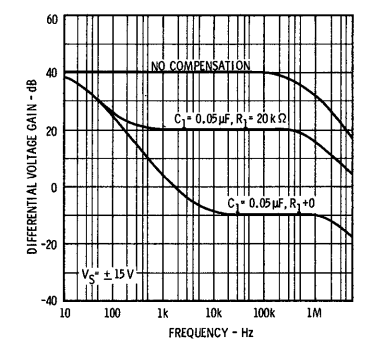
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



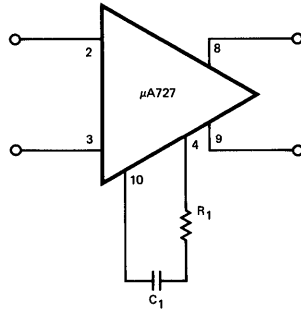
REQUIRED R_ADJ FOR CONSTANT I_ADJ AS A FUNCTION OF SUPPLY VOLTAGE



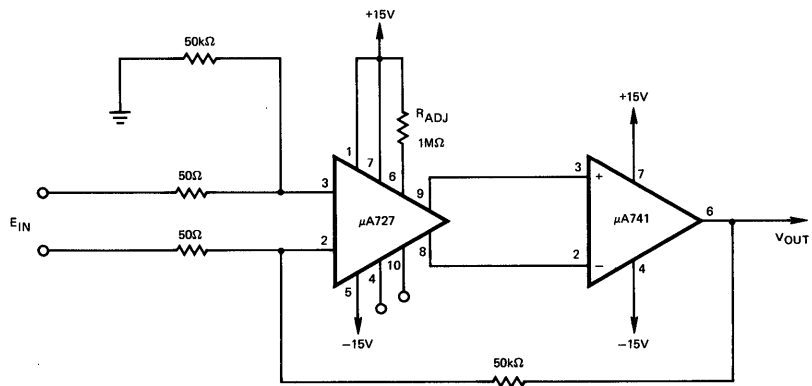
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY COMPENSATION CIRCUIT



TYPICAL X1000 CIRCUIT



μA730

DIFFERENTIAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA730 is a Differential Amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

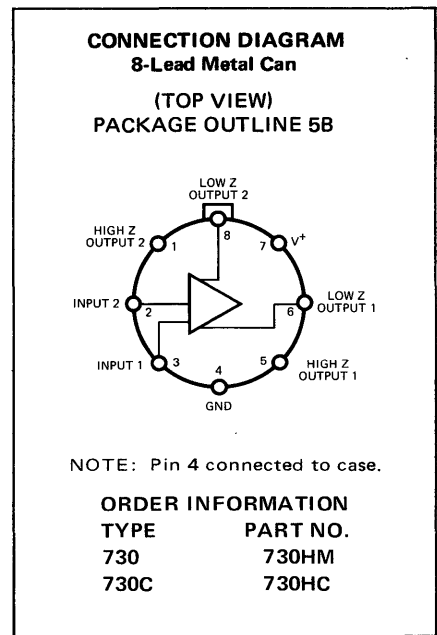
ABSOLUTE MAXIMUM RATINGS

- Supply Voltage
- Differential Input Voltage
- Common Mode Input Voltage
- Internal Power Dissipation (Note 1)
- Operating Temperature Range
 - Military (730)
 - Commercial (730C)
- Storage Temperature Range
- Lead Temperature (Soldering, 60 seconds)

- 15 V
- ±5 V
- 2.5 to 5.5 V
- 500 mW
- 55°C to +125°C
- 0°C to +70°C
- 65°C to +150°C
- +300°C

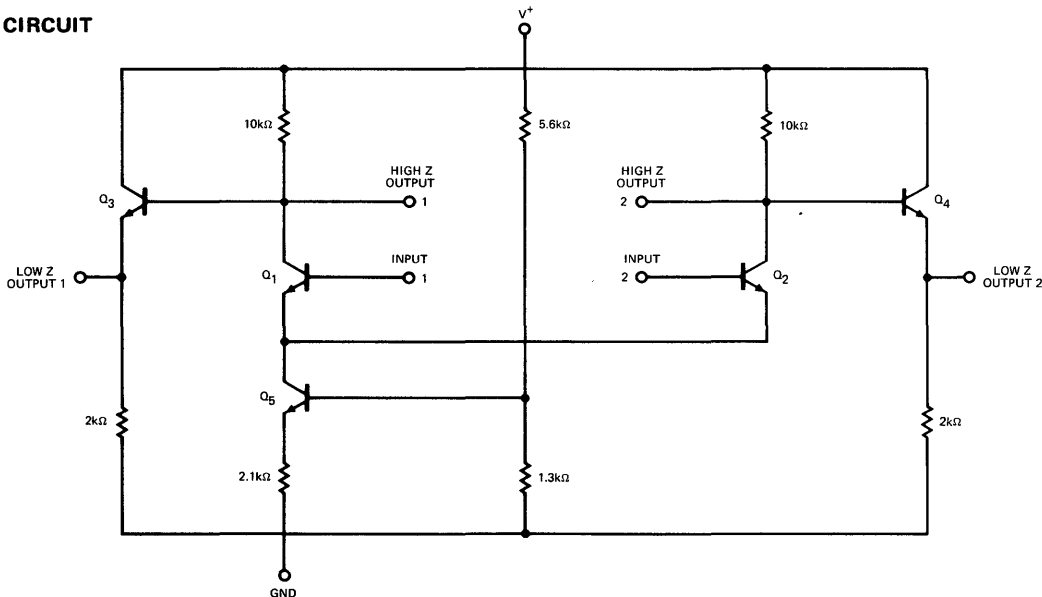
NOTE:

1. Rating applies for ambient temperature to +70°C; derate linearly at 6.3 mW/°C for ambient temperatures above +70°C.



3

EQUIVALENT CIRCUIT



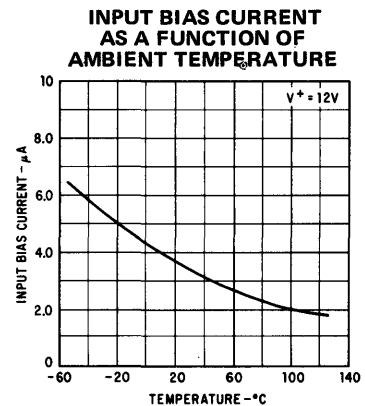
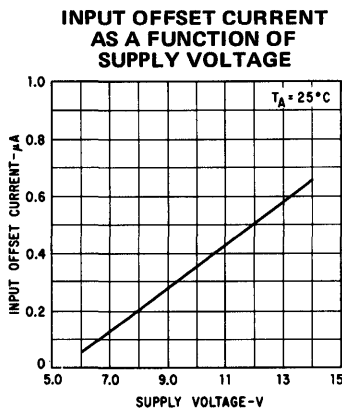
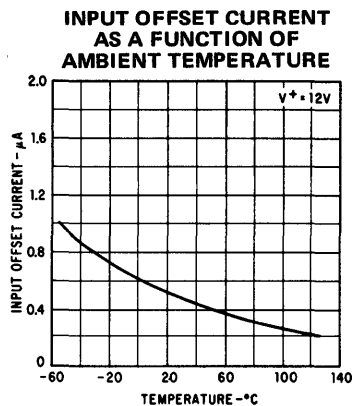
*Planar is a patented Fairchild process.

730

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V^+ = 12.0\text{ V}$, and $V_{CM} = 3.5\text{ V}$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current			0.5	1.5	μA
Input Bias Current			3.5	7.5	μA
Input Resistance		5.0	20		$\text{k}\Omega$
Differential Voltage Gain	$R_L \geq 100\text{ k}\Omega$	100	145	160	
Differential Distortion	$R_L \geq 100\text{ k}\Omega$		80	300	mVp-p
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100\text{ k}\Omega$	5.0	8.0		Vp-p
Supply Current	$R_L \geq 100\text{ k}\Omega$		9.5	13	mA
Power Consumption	$R_L \geq 100\text{ k}\Omega$		114	156	mW
The following specifications apply for $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$:					
Input Offset Voltage	$R_S \leq 50\Omega$			3.5	mV
Input Offset Current	$T_A = +125^\circ\text{C}$		0.2	1.5	μA
	$T_A = -55^\circ\text{C}$		1.0	3.0	μA
Input Bias Current	$T_A = -55^\circ\text{C}$		6.5	15	μA
Input Resistance		0.9			$\text{k}\Omega$
Input Voltage Range		3.5		5.2	V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$ $f \leq 1.0\text{ kHz}$, $+3.5\text{V} \leq V_{CM} \leq +5.2\text{V}$	70	85		dB
Differential Voltage Gain	$R_L \geq 100\text{ k}\Omega$	90		175	
Common Mode Output Voltage		5.5	7.0	7.75	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	6.8		Vp-p
Supply Current	$T_A = -55^\circ\text{C}$		10	15	mA
	$T_A = 125^\circ\text{C}$		8.0	11	mA
Power Consumption	$T_A = -55^\circ\text{C}$		120	180	mW
	$T_A = 125^\circ\text{C}$		96	121	mW

TYPICAL PERFORMANCE CURVES FOR 730

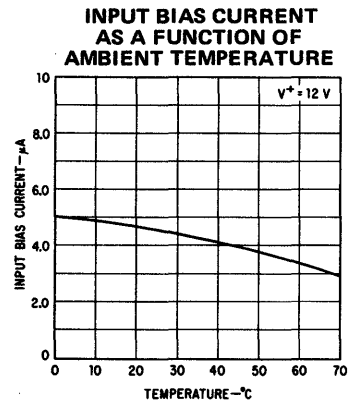
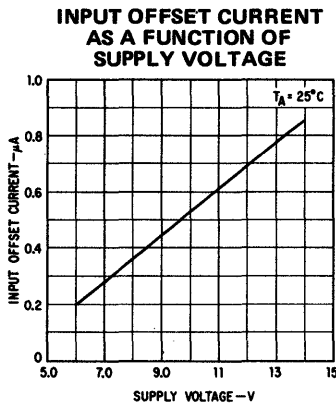
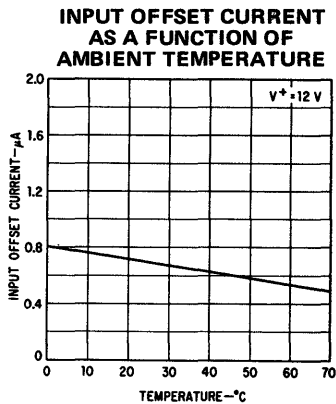


730C

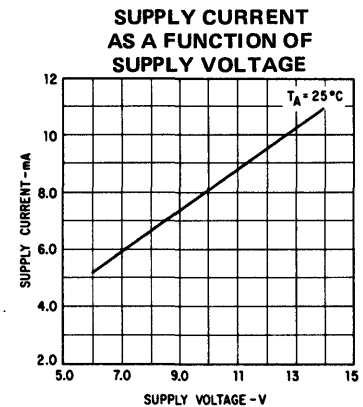
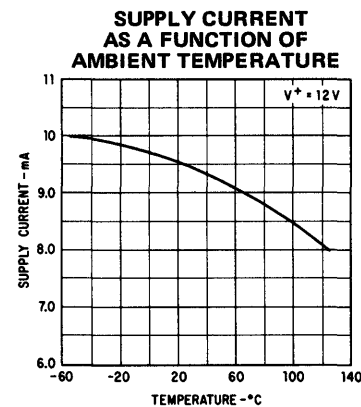
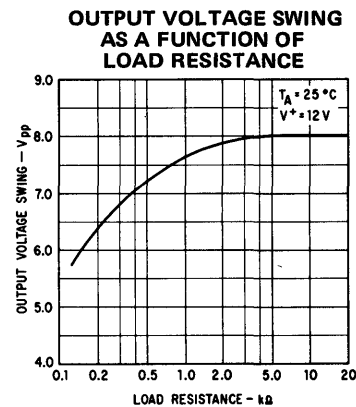
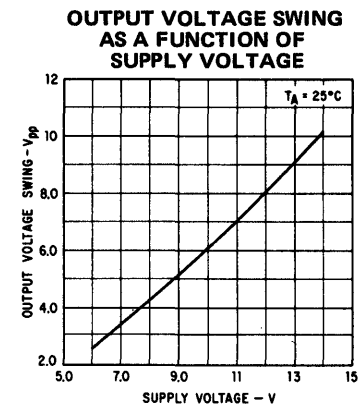
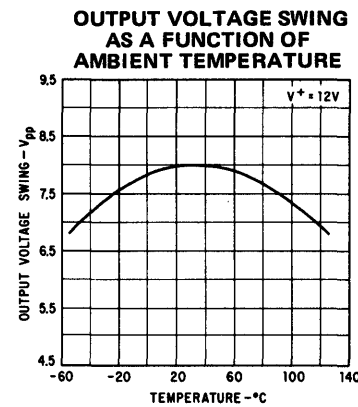
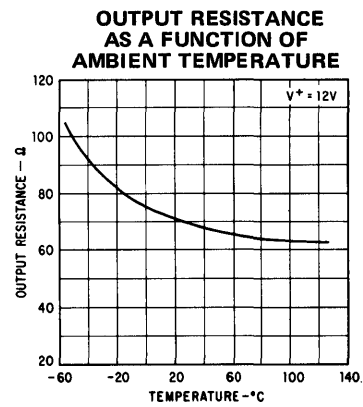
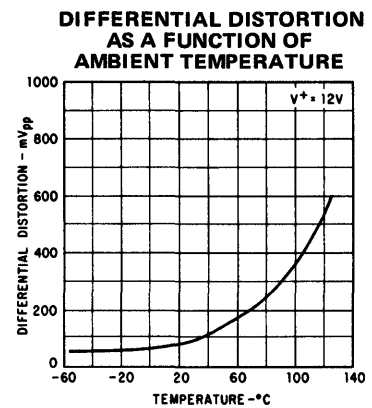
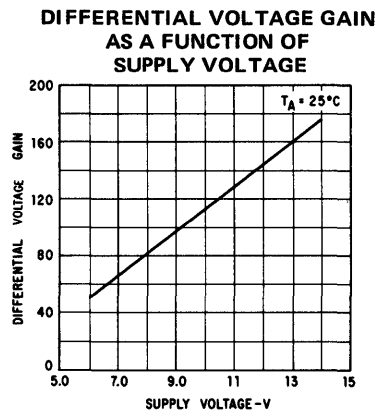
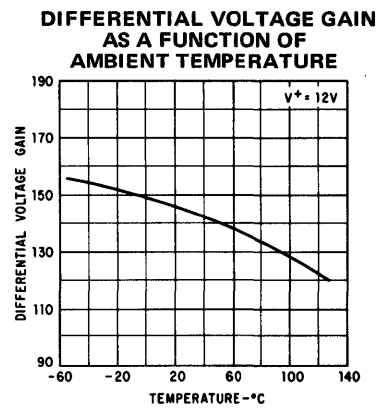
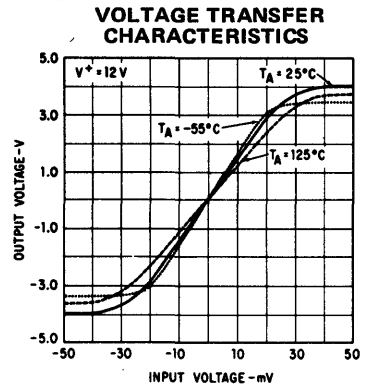
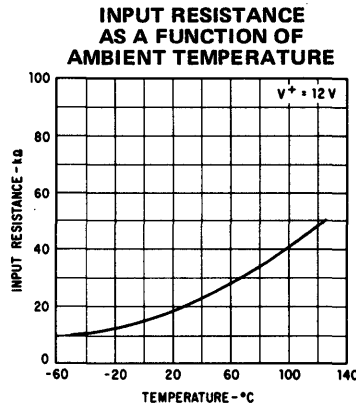
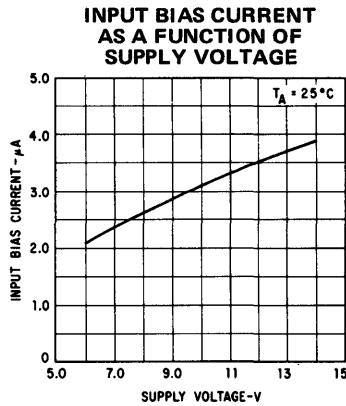
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$, $V^+ = 12.0 V$, and $V_{CM} = 3.5 V$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	5.0	mV
Input Offset Current			0.7	3.0	μA
Input Bias Current			4.5	16.0	μA
Input Resistance		2.5	15		$k\Omega$
Differential Voltage Gain	$R_L \geq 100 k\Omega$	100	135	160	
Differential Distortion	$R_L \geq 100 k\Omega$		85	300	mVp-p
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100 k\Omega$	5.0	8.0		Vp-p
Supply Current	$R_L \geq 100 k\Omega$		9.5	13	mA
Power Consumption	$R_L \geq 100 k\Omega$		114	156	mW
The following specifications apply for $0^\circ C \leq T_A \leq +70^\circ C$					
Input Offset Voltage	$R_S \leq 50\Omega$			7.5	mV
Input Offset Current	$T_A = +70^\circ C$		0.5	3.0	μA
	$T_A = 0^\circ C$		0.8	5.0	μA
Input Bias Current	$T_A = 0^\circ C$		5.0	20	μA
Input Resistance		1.8			$k\Omega$
Input Voltage Range		+3.5		+5.2	
Common Mode Rejection Ratio	$R_S \leq 50\Omega$ $f \leq 1.0 kHz$, $+3.5V \leq V_{CM} \leq +5.2V$	60	80		dB
Differential Voltage Gain	$R_L \geq 100 k\Omega$	80		190	
Common Mode Output Voltage		5.0	7.0	8.0	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	7.5		Vp-p
Supply Current	$T_A = 0^\circ C$		10	15	mA
	$T_A = +70^\circ C$		8.8	13	mA
Power Consumption	$T_A = 0^\circ C$		120	180	mW
	$T_A = +70^\circ C$		106	156	mW

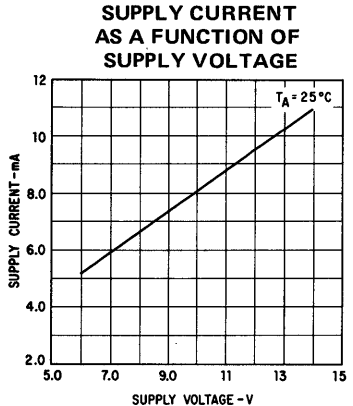
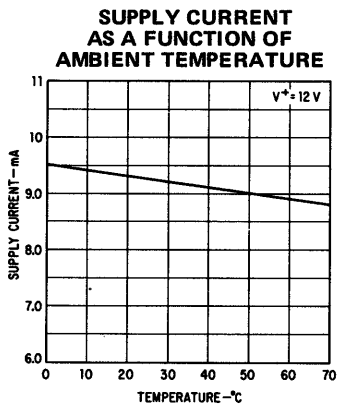
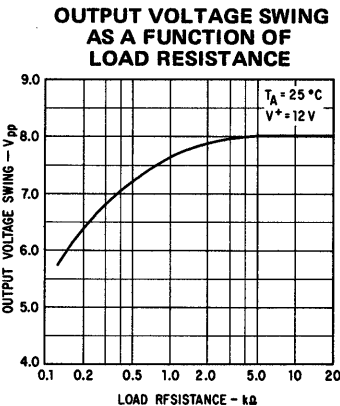
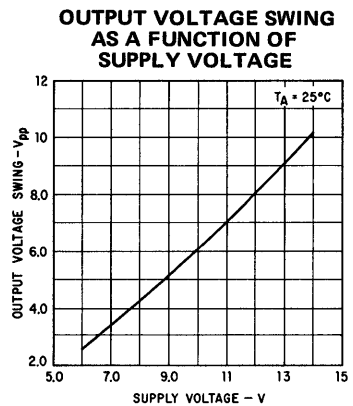
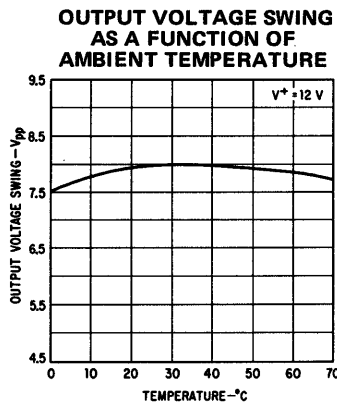
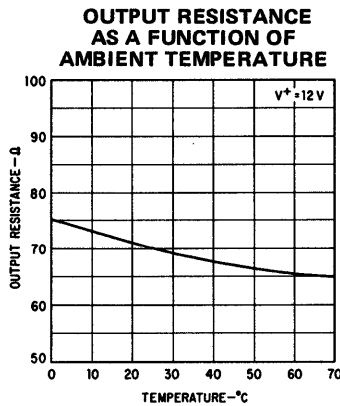
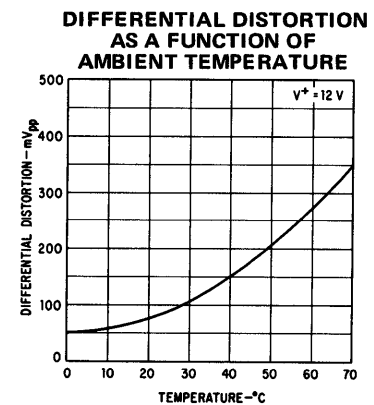
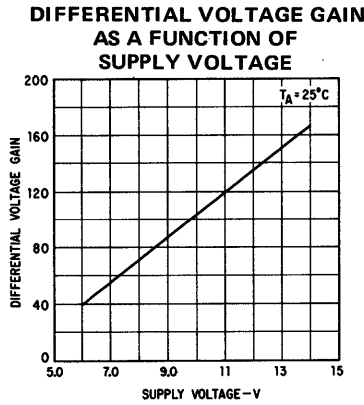
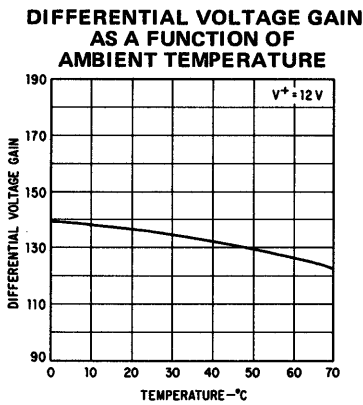
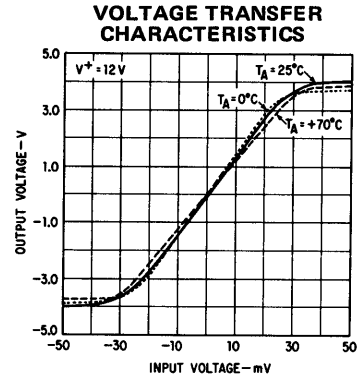
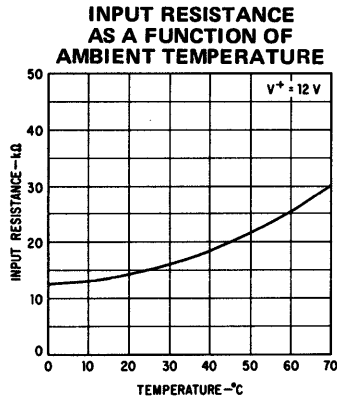
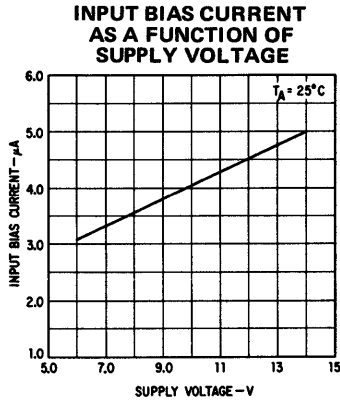
TYPICAL PERFORMANCE CURVES FOR 730C



TYPICAL PERFORMANCE CURVES FOR 730

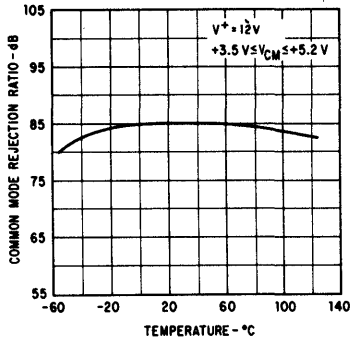


TYPICAL PERFORMANCE CURVES FOR 730C

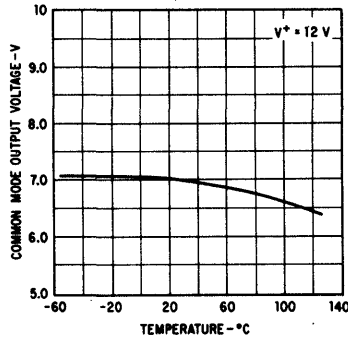


TYPICAL PERFORMANCE CURVES FOR 730 AND 730C

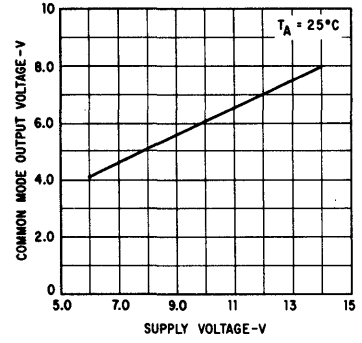
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



μA740

FET INPUT OPERATIONAL AMPLIFIER

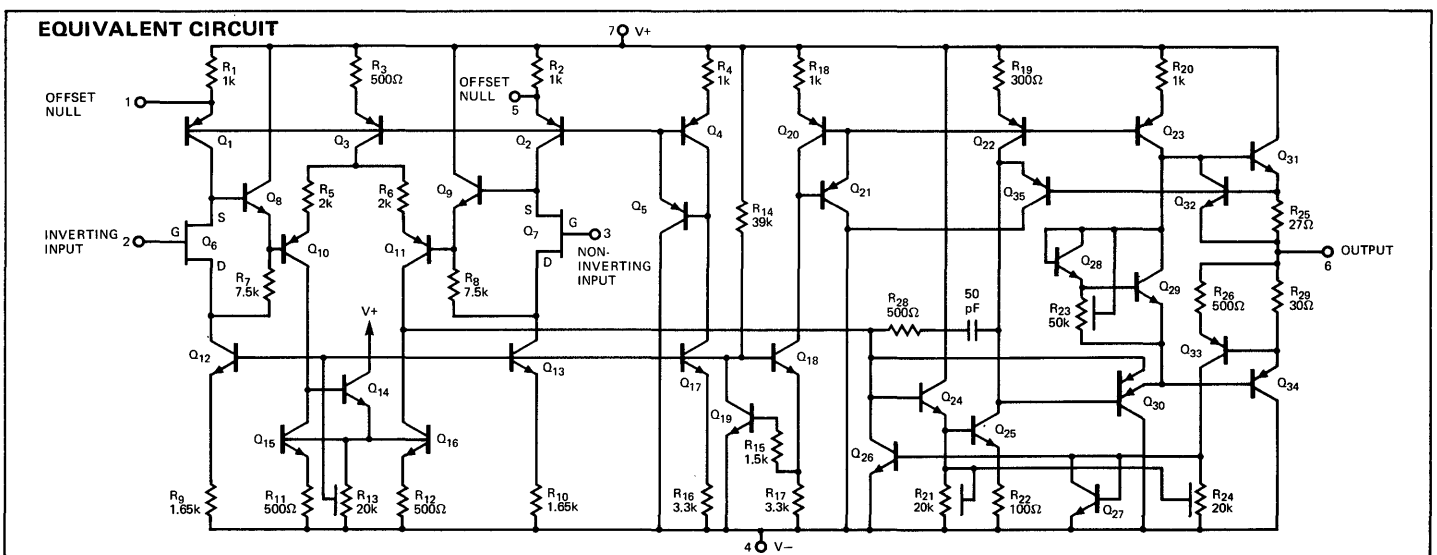
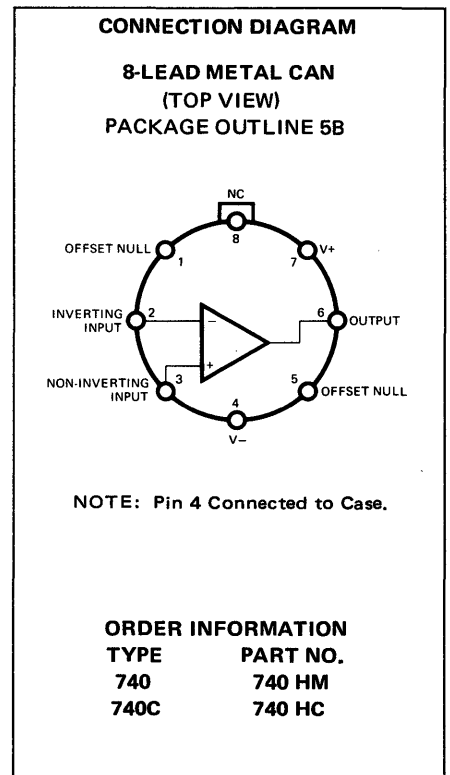
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA740 is a high performance monolithic FET-Input Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where very high input impedance is required and features very low input offset current and very low input bias current. High slew rate, high common mode voltage range and absence of "latch up" make the μA740 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in active filters, integrators, summing amplifiers, sample and holds, transducer amplifiers, and other general feedback applications. The μA740 is short circuit protected and has the same pin configuration as the popular μA741 operational amplifier. No external components for frequency compensation are required as the internal 6 dB/octave roll-off insures stability in closed loop applications.

- HIGH INPUT IMPEDANCE . . . 1,000,000 MΩ
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V+	±0.5V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (740)	-55°C to +125°C
Commercial (740C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite



Notes on following pages.

*Planar is a patented Fairchild process.

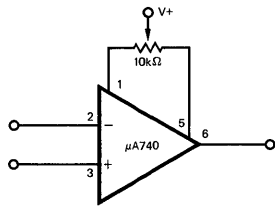
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_C = 25^\circ C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 100 k\Omega$		10	20	mV
Input Offset Current [Note 4]			40	150	pA
Input Current (either input) [Note 4]			100	200	pA
Input Resistance			1,000,000		$M\Omega$
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50,000	1,000,000		
Output Resistance			75		Ω
Output Short-Circuit Current			20		mA
Common Mode Rejection Ratio		64	80		dB
Supply Voltage Rejection Ratio			70	300	$\mu V/V$
Supply Current			4.2	5.2	mA
Power Consumption			126	156	mW
Slew Rate			6.0		V/ μs
Unity Gain Bandwidth			3.0		MHz
Transient Response (Unity Gain)	Risetime	$C_L \leq 100pF$, $R_L = 2k\Omega$, $V_{IN} = 100mV$	110		ns
	Overshoot		10	20	%

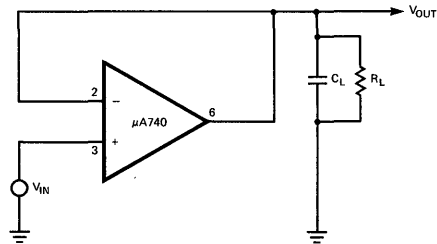
The following specifications apply for $T_C = -55^\circ C$ to $+85^\circ C$:

Input Voltage Range		± 10		± 12	V
Large Signal Voltage Gain		25,000			
Output Voltage Swing	$R_L \geq 10k\Omega$	± 12	± 14		V
	$R_L \geq 2k\Omega$	± 10	± 13		V
Input Offset Voltage	$R_S \leq 100k\Omega$		15	30	mV
Input Offset Current	$T_A = -55^\circ C$		30		pA
	$T_A = +85^\circ C$		185		pA
Input Current (either input)	$T_A = -55^\circ C$			200	pA
	$T_A = +85^\circ C$		2.5	4.0	nA

**VOLTAGE OFFSET
NULL CIRCUIT**



**TRANSIENT RESPONSE
TEST CIRCUIT**



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A740

740C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_C = 25^\circ C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Input Offset Voltage	$R_S \leq 100k\Omega$		30	110	mV	
Input Offset Current (Note 4)			60	300	pA	
Input Current (either input) [Note 4]			0.1	2.0	nA	
Input Resistance			1,000,000		M Ω	
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	20,000	1,000,000			
Output Resistance			75		Ω	
Output Short-Circuit Current			20		mA	
Supply Current			4.2	8.0	mA	
Power Consumption			126	240	mW	
Slew Rate			6.0		V/ μ s	
Unity Gain Bandwidth			1.0		MHz	
Transient Response (Unity Gain)	Risetime	$C_L \leq 100pF$, $R_L = 2k\Omega$, $V_{IN} = 100mV$		300		ns
	Overshoot			10		%

The following specifications apply for $0^\circ C \leq T_A \leq +70^\circ C$:

Input Voltage Range		± 10	± 12		V
Common Mode Rejection Ratio		55	80		dB
Supply Voltage Rejection Ratio			70	500	$\mu V/V$
Large Signal Voltage Gain			500,000		
Output Voltage Swing	$R_L \geq 10k\Omega$	± 12	± 14		V
	$R_L \geq 2k\Omega$	± 10	± 13		V
Input Offset Voltage			30		mV
Input Offset Current			60		pA
Input Current (either input)			1.1	10	nA

NOTES:

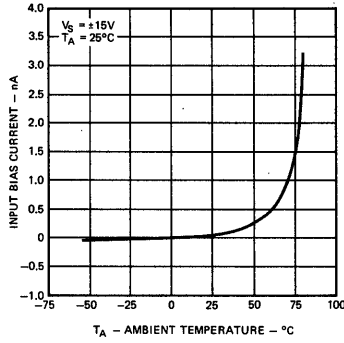
1. Rating applies for ambient temperature to $+70^\circ C$; derate linearly at 6.3mW/ $^\circ C$ for ambient temperatures above $+70^\circ C$.
2. For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to $+125^\circ C$ case temperature or $+75^\circ C$ ambient temperature.
4. Typically doubles for every $10^\circ C$ increase in ambient temperature.

3

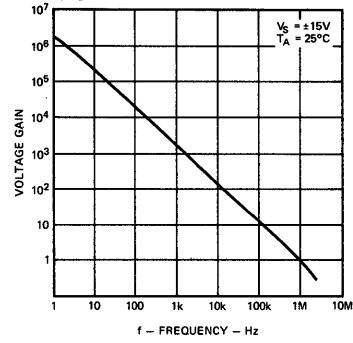
FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A740$

TYPICAL PERFORMANCE CURVES FOR 740 AND 740C

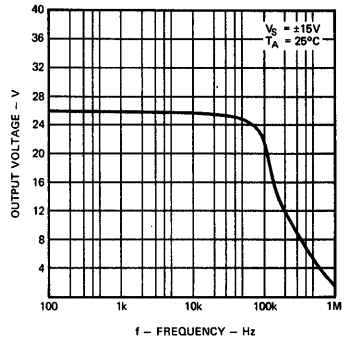
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



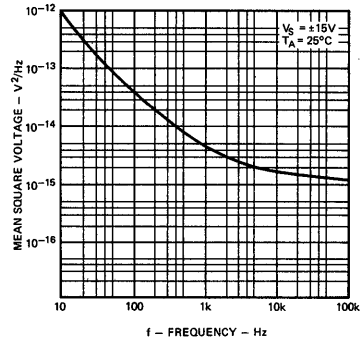
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



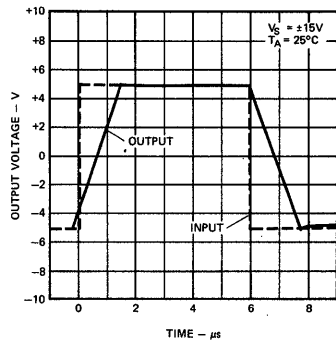
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



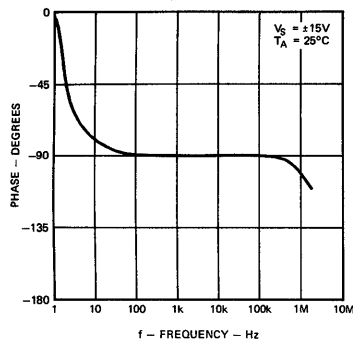
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

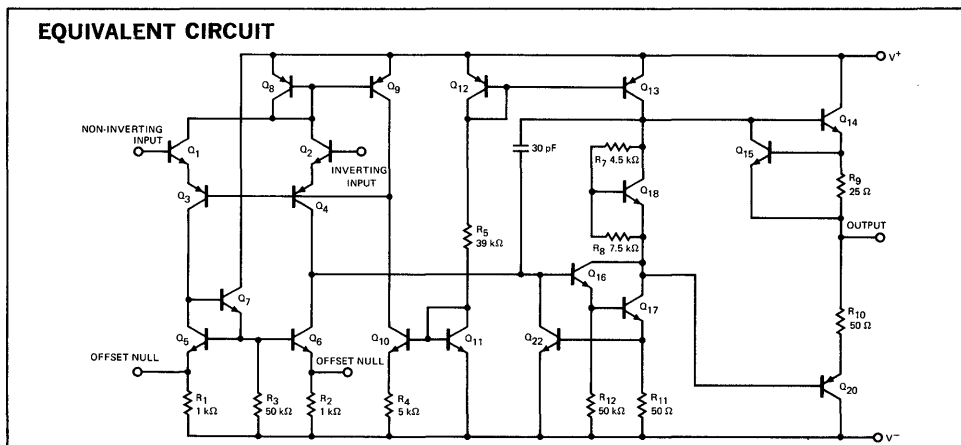
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

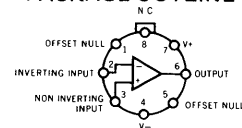
Supply Voltage	
Military (741)	±22 V
Commercial (741C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (741)	−55°C to +125°C
Commercial (741C)	0°C to +70°C
Lead Temperature (Soldering)	
Metal Can, DIP, and Flatpak (60 seconds)	300°C
Mini DIP (10 seconds)	260°C
Output Short Circuit Duration (Note 3)	Indefinite



Notes on following pages.

CONNECTION DIAGRAMS

8-LEAD METAL CAN (TOP VIEW) PACKAGE OUTLINE 5B

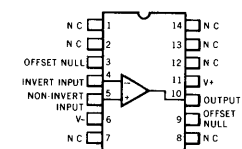


Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
741	741HM
741C	741HC

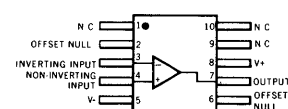
14-LEAD DIP (TOP VIEW) PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
741	741DM
741C	741DC

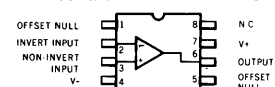
10-LEAD FLATPAK (TOP VIEW) PACKAGE OUTLINE 3F



ORDER INFORMATION

TYPE	PART NO.
741	741FM

8-LEAD MINIDIP (TOP VIEW) PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
741C	741TC

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A741

741

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25^\circ$ C unless otherwise specified)

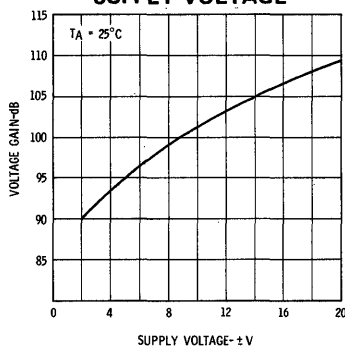
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ k Ω		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		M Ω
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			± 15		mV
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	50,000	200,000		
Output Resistance			75		Ω
Output Short Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (Unity Gain)	$V_{IN} = 20$ mV, $R_L = 2$ k Ω , $C_L \leq 100$ pF		0.3		μ s
		Risetime		5.0	
Slew Rate	$R_L \geq 2$ k Ω		0.5		V/ μ s

The following specifications apply for -55° C $\leq T_A \leq +125^\circ$ C:

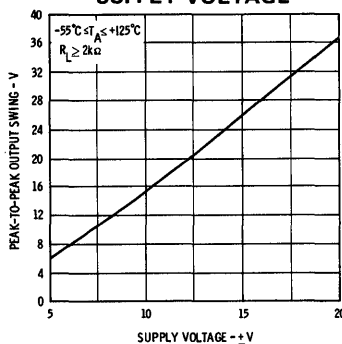
Input Offset Voltage	$R_S \leq 10$ k Ω		1.0	6.0	mV
Input Offset Current	$T_A = +125^\circ$ C		7.0	200	nA
	$T_A = -55^\circ$ C		85	500	nA
Input Bias Current	$T_A = +125^\circ$ C		0.03	0.5	μ A
	$T_A = -55^\circ$ C		0.3	1.5	μ A
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ k Ω		30	150	μ V/V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ k Ω	± 12	± 14		V
	$R_L \geq 2$ k Ω	± 10	± 13		V
Supply Current	$T_A = +125^\circ$ C		1.5	2.5	mA
	$T_A = -55^\circ$ C		2.0	3.3	mA
Power Consumption	$T_A = +125^\circ$ C		45	75	mW
	$T_A = -55^\circ$ C		60	100	mW

TYPICAL PERFORMANCE CURVES FOR 741

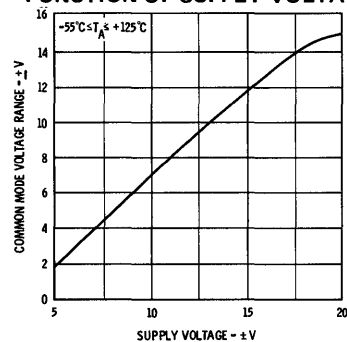
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



741C

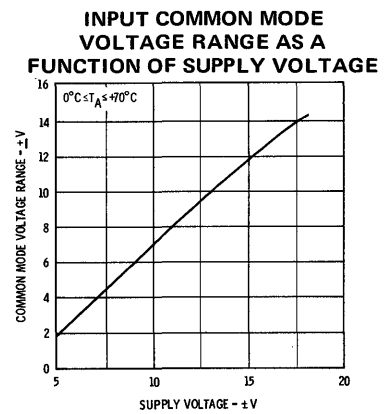
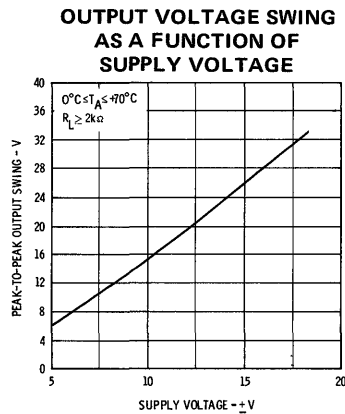
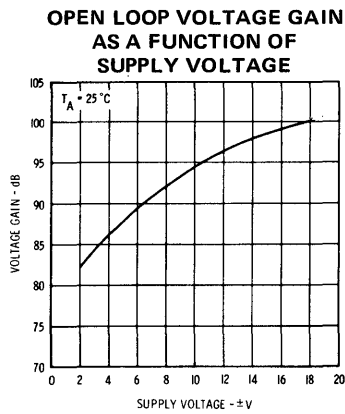
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 10\text{ k}\Omega$		2.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		M Ω
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				± 15		mV
Input Voltage Range			± 12	± 13		V
Common Mode Rejection Ratio		$R_S \leq 10\text{ k}\Omega$	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10\text{ k}\Omega$		30	150	$\mu\text{V/V}$
Large Signal Voltage Gain		$R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	20,000	200,000		
Output Voltage Swing		$R_L \geq 10\text{ k}\Omega$	± 12	± 14		V
		$R_L \geq 2\text{ k}\Omega$	± 10	± 13		V
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Risetime	$V_{IN} = 20\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2\text{ k}\Omega$		0.5		V/ μs

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$:

Input Offset Voltage					7.5	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Large Signal Voltage Gain		$R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	15,000			
Output Voltage Swing		$R_L \geq 2\text{ k}\Omega$	± 10	± 13		V

TYPICAL PERFORMANCE CURVES FOR 741C

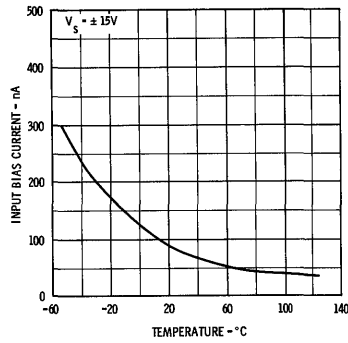


NOTES:

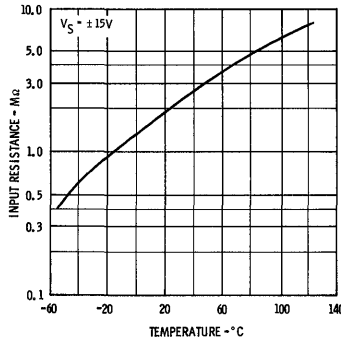
- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3\text{ mW}/^\circ\text{C}$ for the Metal Can, $8.3\text{ mW}/^\circ\text{C}$ for the DIP, $5.6\text{ mW}/^\circ\text{C}$ for the Mini DIP and $7.1\text{ mW}/^\circ\text{C}$ for the Flatpak.
- For supply voltages less than $\pm 15\text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply. Rating applies to $+125^\circ\text{C}$ case temperature or 75°C ambient temperature.

TYPICAL PERFORMANCE CURVES FOR 741

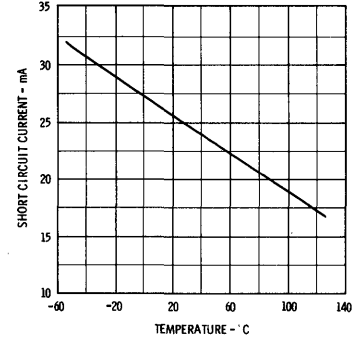
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



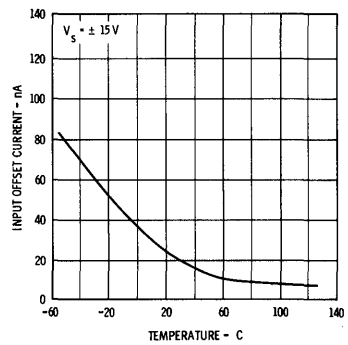
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



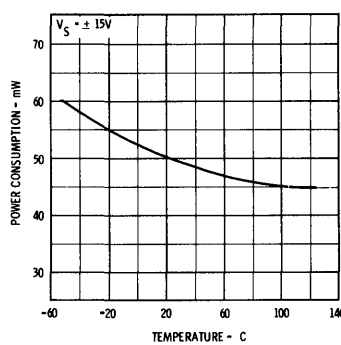
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



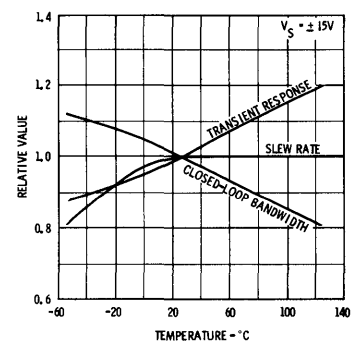
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

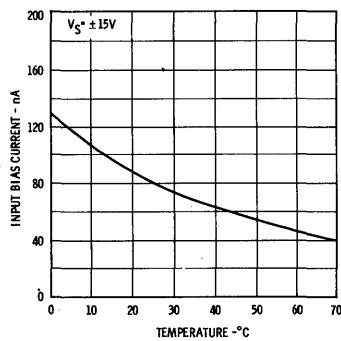


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

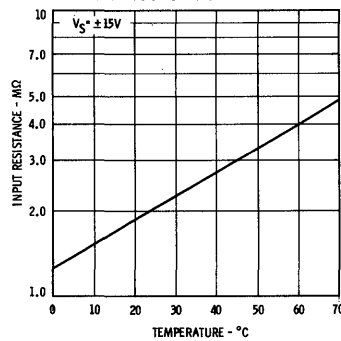


TYPICAL PERFORMANCE CURVES FOR 741C

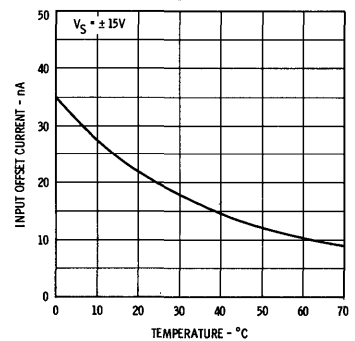
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



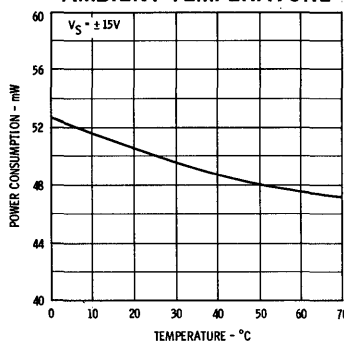
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



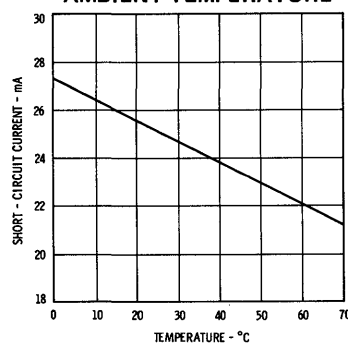
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



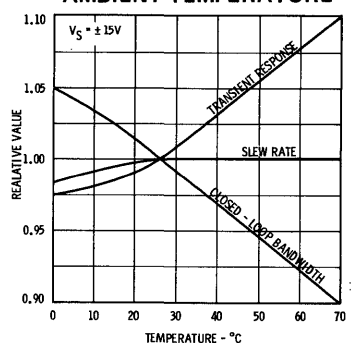
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

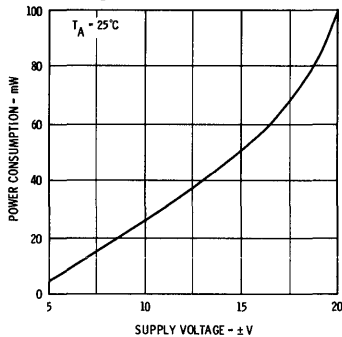


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

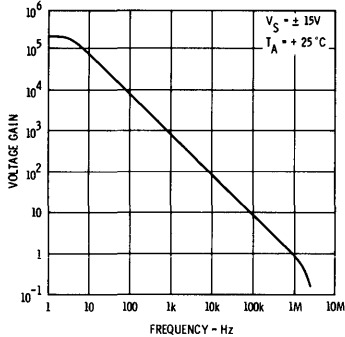


TYPICAL PERFORMANCE CURVES FOR 741 AND 741C (Cont'd)

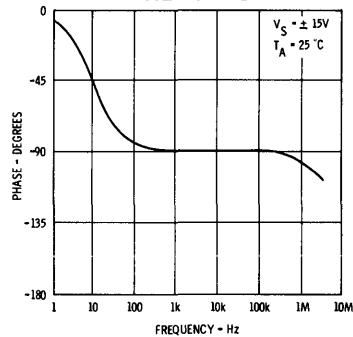
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



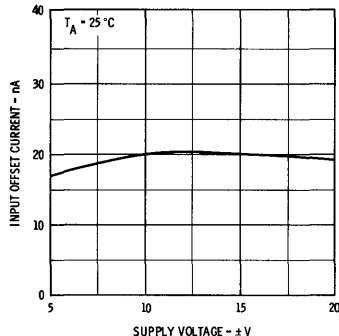
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



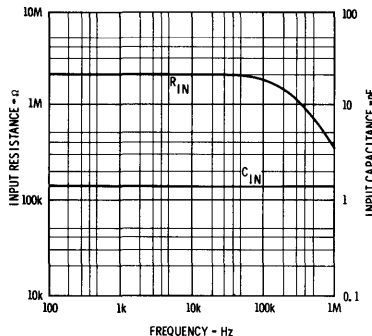
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



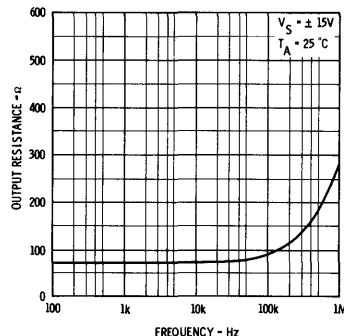
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



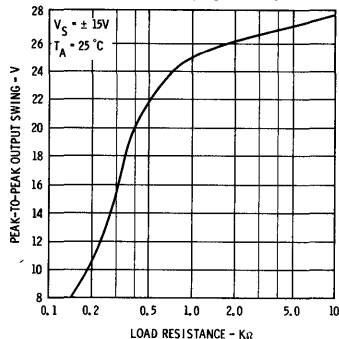
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



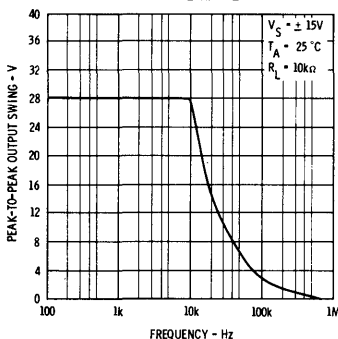
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



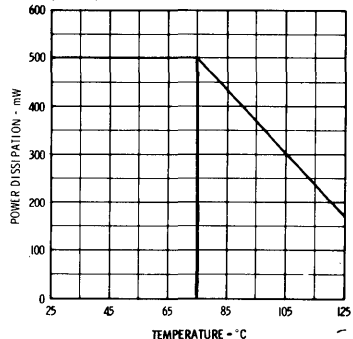
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



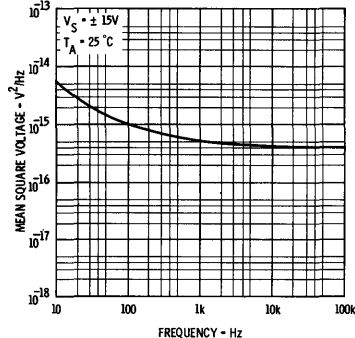
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



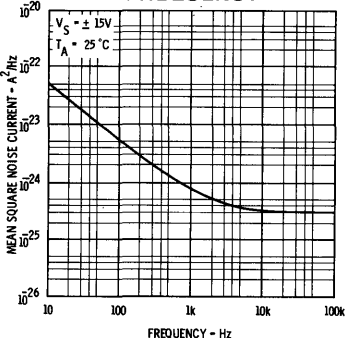
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



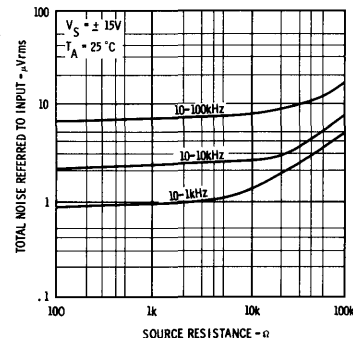
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



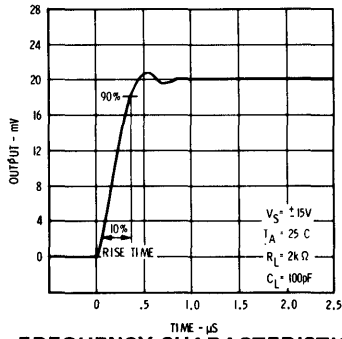
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



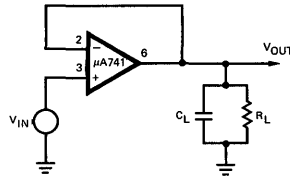
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



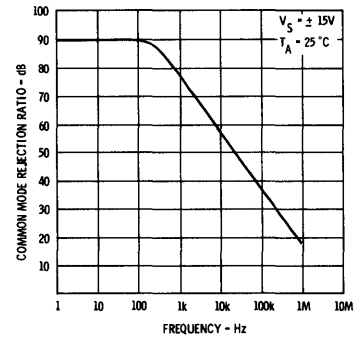
TRANSIENT RESPONSE



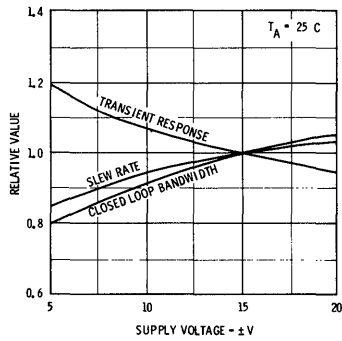
TRANSIENT RESPONSE TEST CIRCUIT



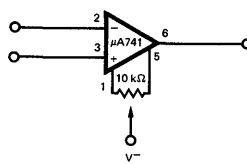
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



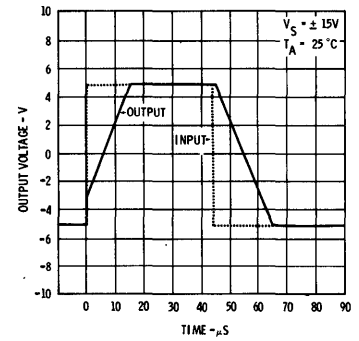
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

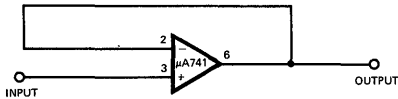


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



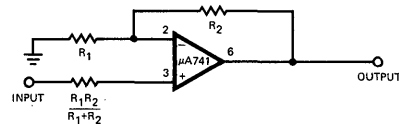
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



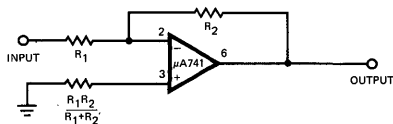
$R_{IN} = 400 \text{ M}\Omega$
 $C_{IN} = 1 \text{ pF}$
 $R_{OUT} \ll 1 \Omega$
 B.W. = 1 MHz

NON-INVERTING AMPLIFIER



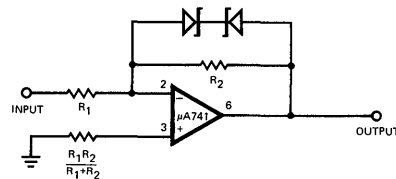
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 k Ω	9 k Ω	100 kHz	400 M Ω
100	100 Ω	9.9 k Ω	10 kHz	280 M Ω
1000	100 Ω	99.9 k Ω	1 kHz	80 M Ω

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 k Ω	10 k Ω	1 MHz	10 k Ω
10	1 k Ω	10 k Ω	100 kHz	1 k Ω
100	1 k Ω	100 k Ω	10 kHz	1 k Ω
1000	100 Ω	100 k Ω	1 kHz	100 Ω

CLIPPING AMPLIFIER

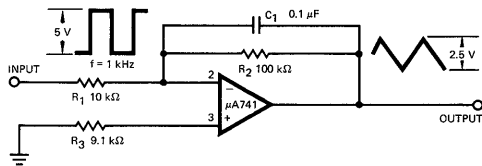


$$\frac{E_{OUT}}{E_{IN}} = \frac{R_2}{R_1} \text{ if } |E_{OUT}| \leq V_Z + 0.7 \text{ V}$$

where V_Z = Zener breakdown voltage

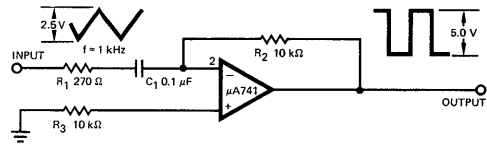
TYPICAL APPLICATIONS (Cont'd)

SIMPLE INTEGRATOR



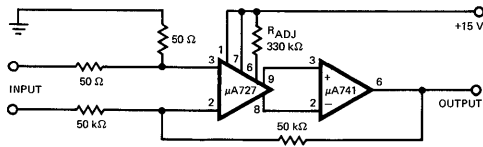
$$E_{OUT} = - \frac{1}{R_1 C_1} \int E_{IN} dt$$

SIMPLE DIFFERENTIATOR



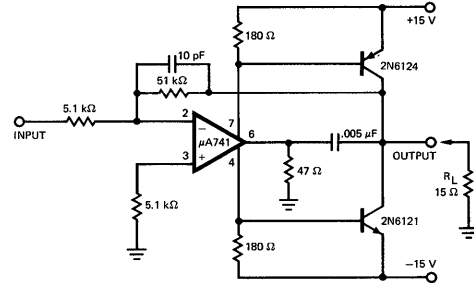
$$E_{OUT} = - R_2 C_1 \frac{dE_{IN}}{dt}$$

LOW DRIFT LOW NOISE AMPLIFIER

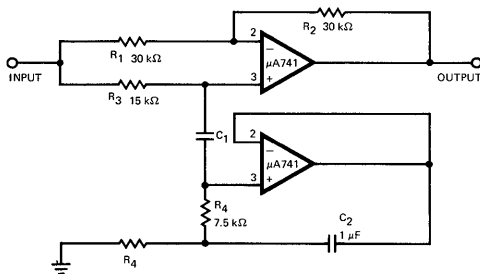


Voltage Gain = 10^3
 Input Offset Voltage Drift = $0.6 \mu V/^{\circ}C$
 Input Offset Current Drift = $2.0 pA/^{\circ}C$

HIGH SLEW RATE POWER AMPLIFIER

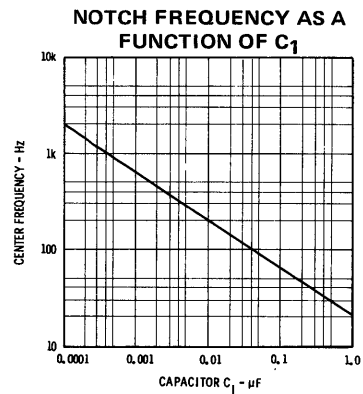


NOTCH FILTER USING THE $\mu A741$ AS A GYRATOR



Trim R_3 such that

$$\frac{R_1}{R_2} = \frac{R_3}{2 R_4}$$



μA741A • μA741E

FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER

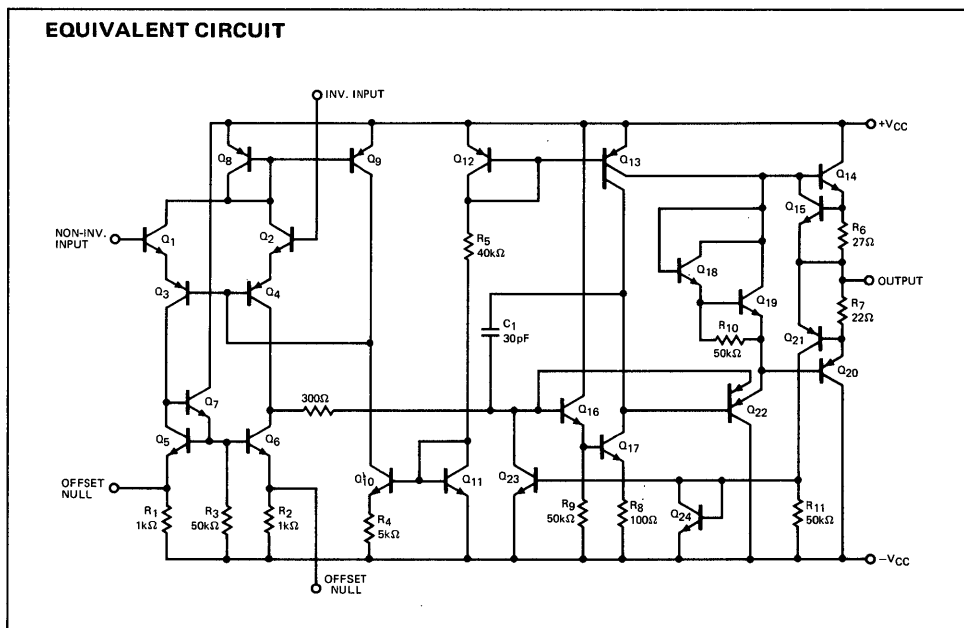
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA741A and E are high performance monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741A and E ideal for use as voltage followers. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. Electrical characteristics are identical to MIL-M-38510/10101.

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

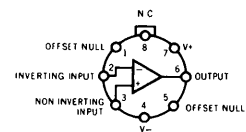
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	
Metal Can	500mW
DIP	670mW
Flatpak	570mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (741A)	-55°C to +125°C
Commercial (741E)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short Circuit Duration (Note 3)	Indefinite



Notes on following pages.

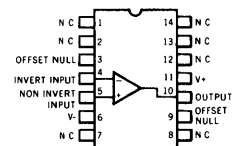
CONNECTION DIAGRAMS
8-LEAD METAL CAN
 (TOP VIEW)
 PACKAGE OUTLINE 5B



ORDER INFORMATION

TYPE	PART NO.
741A	741AHM
741EC	741EHC

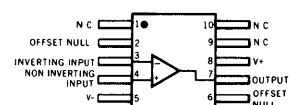
14-LEAD DIP
 (TOP VIEW)
 PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
741A	741ADM
741EC	741EDC

10-LEAD FLATPAK
 (TOP VIEW)
 PACKAGE OUTLINE 3F



ORDER INFORMATION

TYPE	PART NO.
741A	741AFM

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A741A • μ A741E

741A

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift				15	$\mu V/^\circ C$
Input Offset Current			3.0	30	nA
Average Input Offset Current Drift				0.5	nA/ $^\circ C$
Input Bias Current			30	80	nA
Power Supply Rejection Ratio	$V_S = +10, -20; V_S = +20, -10V, R_S = 50\Omega$		15	50	$\mu V/V$
Output Short Circuit Current		10	25	35	mA
Power Dissipation	$V_S = \pm 20V$		80	150	mW
Input Impedance	$V_S = \pm 20V$	1.0	6.0		M Ω
Large Signal Voltage Gain	$V_S = \pm 20V, R_L = 2k\Omega, V_{OUT} = \pm 15V$	50			V/mV
Transient Response (Unity Gain)	Rise Time		0.25	0.8	μs
	Overshoot		6.0	20	%
Bandwidth (Note 4)		.437	1.5		MHz
Slew Rate (Unity Gain)	$V_{IN} = \pm 10V$	0.3	0.7		V/ μs
The following specifications apply for $-55^\circ C \leq T_A \leq +125^\circ C$					
Input Offset Voltage				4.0	mV
Input Offset Current				70	nA
Input Bias Current				210	nA
Common Mode Rejection Ratio	$V_S = \pm 20V, V_{IN} = \pm 15V, R_S = 50\Omega$	80	95		dB
Adjustment For Input Offset Voltage	$V_S = \pm 20V$	10			mV
Output Short Circuit Current		10		40	mA
Power Dissipation	$V_S = \pm 20V$	$-55^\circ C$		165	mW
		$+125^\circ C$		135	mW
Input Impedance	$V_S = \pm 20V$	0.5			M Ω
Output Voltage Swing	$V_S = \pm 20V,$	$R_L = 10k\Omega$	± 16		V
		$R_L = 2k\Omega$	± 15		V
Large Signal Voltage Gain	$V_S = \pm 20V, R_L = 2k\Omega, V_{OUT} = \pm 15V$	32			V/mV
	$V_S = \pm 5V, R_L = 2k\Omega, V_{OUT} = \pm 2 V$	10			V/mV

NOTES

- Rating applies to ambient temperatures up to $70^\circ C$. Above $70^\circ C$ ambient derate linearly at $6.3mW/^\circ C$ for the Metal Can, $8.3mW/^\circ C$ for the DIP and $7.1mW/^\circ C$ for the Flatpak.
- For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply. Rating applies to $+125^\circ C$ case temperature or $75^\circ C$ ambient temperature.
- Calculated value from: $BW(MHz) = \frac{0.35}{\text{Rise Time } (\mu s)}$

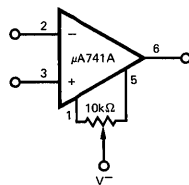
FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A741A • μ A741E

741E

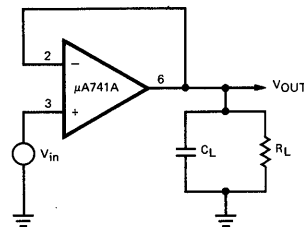
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift				15	$\mu V/^\circ C$
Input Offset Current			3.0	30	nA
Average Input Offset Current Drift				0.5	nA/°C
Input Bias Current			30	80	nA
Power Supply Rejection Ratio	$V_S = +10, -20; V_S = +20, -10V, R_S = 50\Omega$		15	50	$\mu V/V$
Output Short Circuit Current		10	25	35	mA
Power Dissipation	$V_S = \pm 20V$		80	150	mW
Input Impedance	$V_S = \pm 20V$	1.0	6.0		M Ω
Large Signal Voltage Gain	$V_S = \pm 20V, R_L = 2k\Omega, V_{OUT} = \pm 15V$	50			V/mV
Transient Response (Unity Gain)	Rise Time		0.25	0.8	μs
	Overshoot		6.0	20	%
Bandwidth (Note 4)		.437	1.5		MHz
Slew Rate (Unity Gain)	$V_{IN} = \pm 10V$	0.3	0.7		V/ μs
The following specifications apply for $0^\circ C \leq T_A \leq 70^\circ C$					
Input Offset Voltage				4.0	mV
Input Offset Current				70	nA
Input Bias Current				210	nA
Common Mode Rejection Ratio	$V_S = \pm 20V, V_{IN} = \pm 15V, R_S = 50\Omega$	80	95		dB
Adjustment For Input Offset Voltage	$V_S = \pm 20V$	10			mV
Output Short Circuit Current		10		40	mA
Power Dissipation	$V_S = \pm 20V$			150	mW
Input Impedance	$V_S = \pm 20V$	0.5			M Ω
Output Voltage Swing	$V_S = \pm 20V, R_L = 10k\Omega$ $R_L = 2k\Omega$	± 16			V
		± 15			V
Large Signal Voltage Gain	$V_S = \pm 20V, R_L = 2k\Omega, V_{OUT} = \pm 15V$	32			V/mV
	$V_S = \pm 5V, R_L = 2k\Omega, V_{OUT} = \pm 2V$	10			V/mV

**VOLTAGE OFFSET
NULL CIRCUIT**

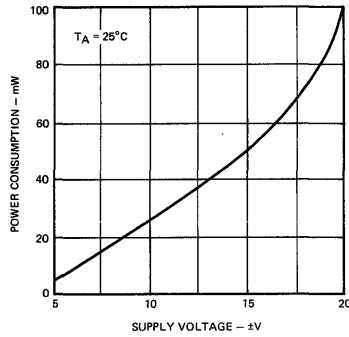


**TRANSIENT RESPONSE
TEST CIRCUIT**

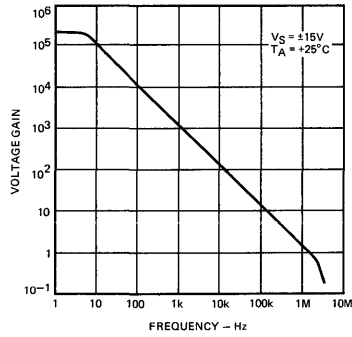


TYPICAL PERFORMANCE CURVES FOR 741A AND 741E

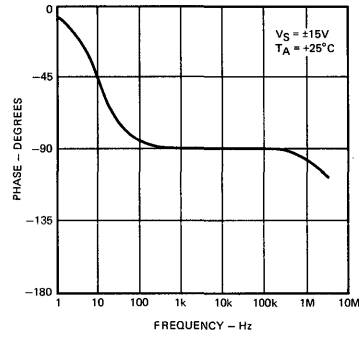
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



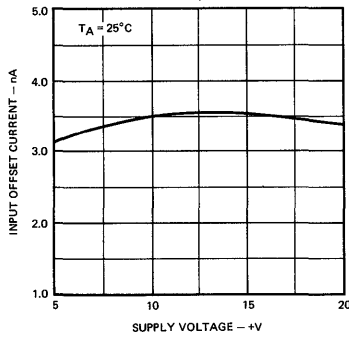
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



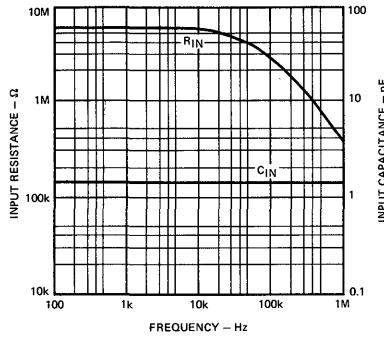
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



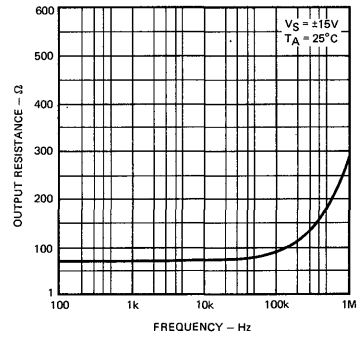
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



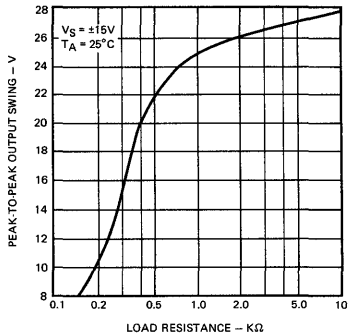
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



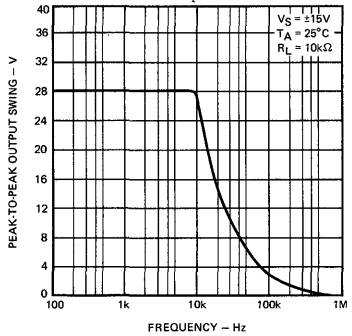
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



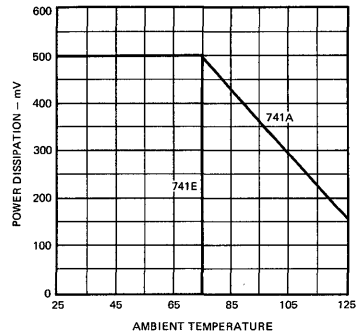
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



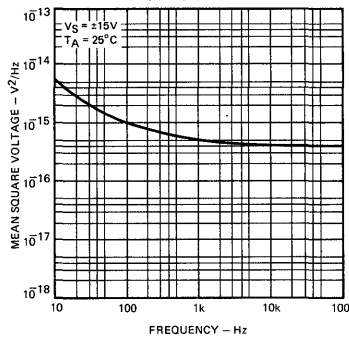
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



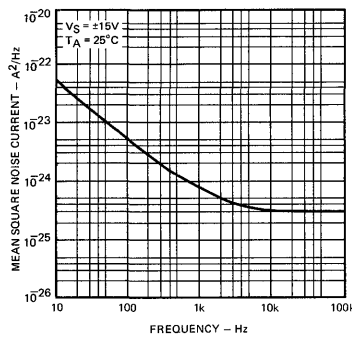
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



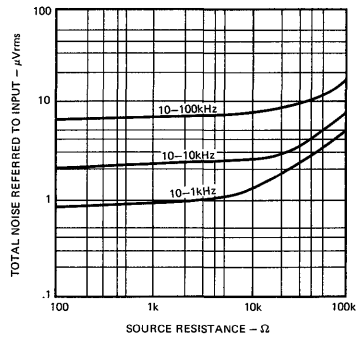
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



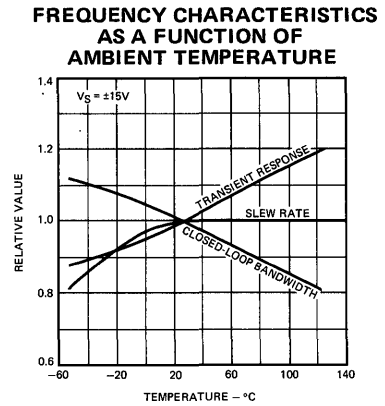
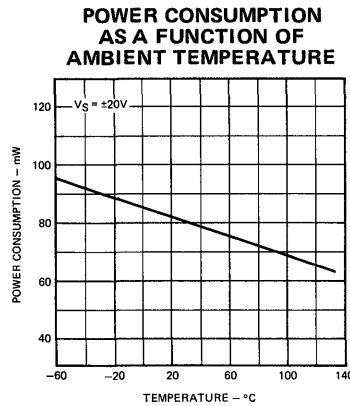
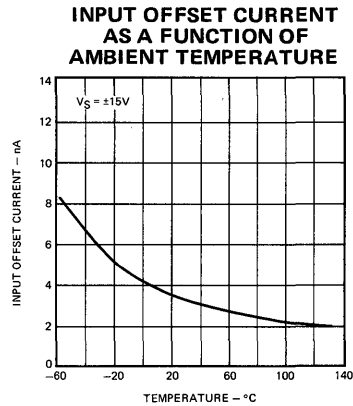
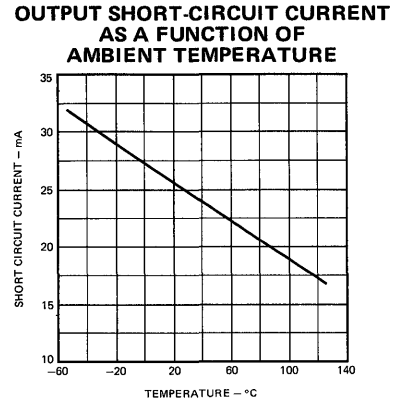
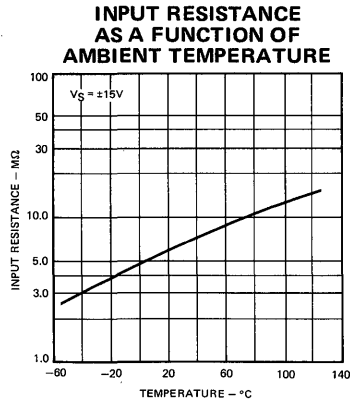
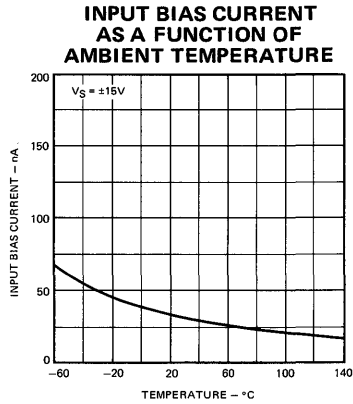
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



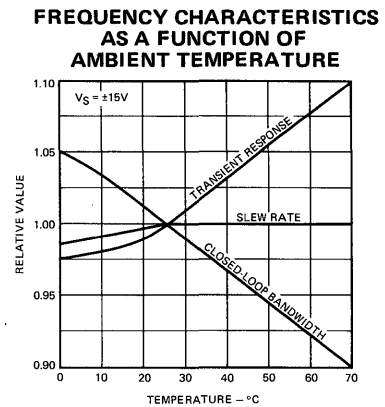
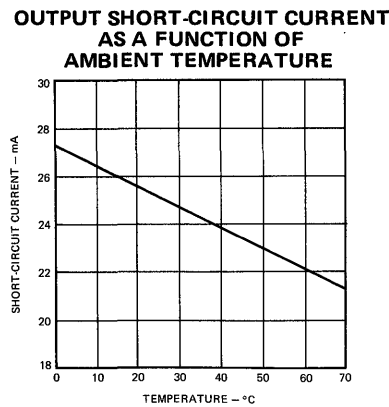
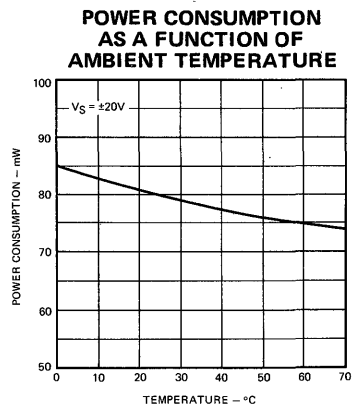
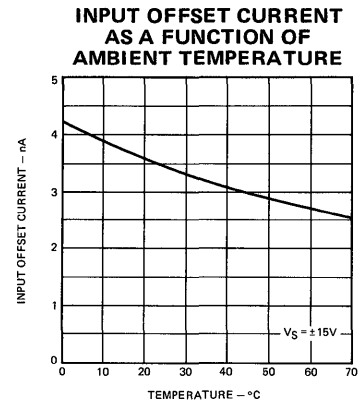
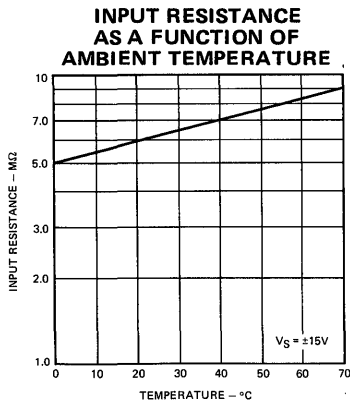
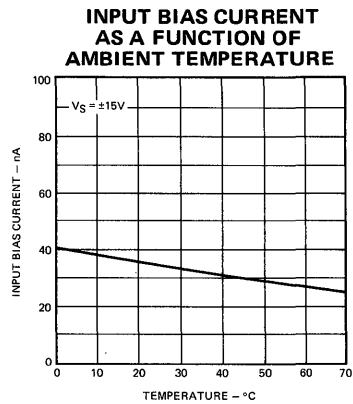
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



TYPICAL PERFORMANCE CURVES FOR 741A



TYPICAL PERFORMANCE CURVES FOR 741E



μA747

DUAL FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER FAIRCHILD LINEAR INTEGRATED CIRCUITS

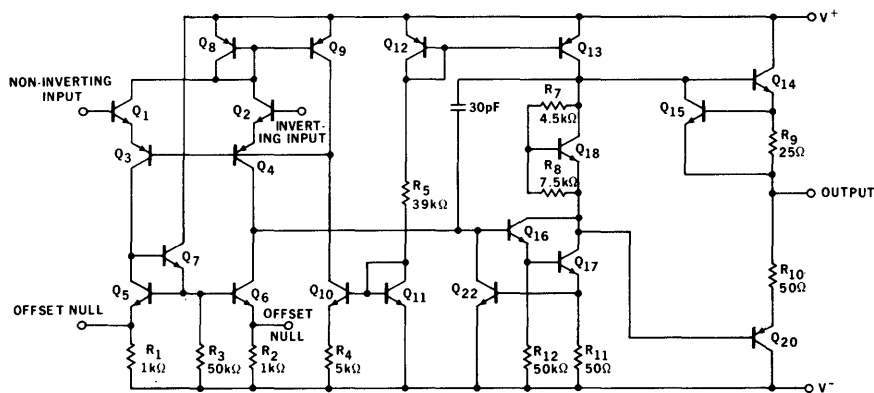
GENERAL DESCRIPTION — The μA747 is a pair of high performance monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short-circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

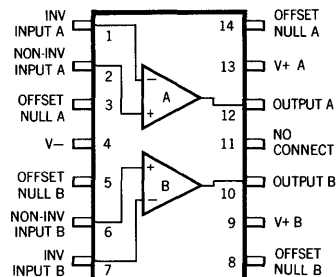
Supply Voltage	
Military (747)	±22 V
Commercial (747C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V ₋	±0.5 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (747)	-55°C to +125°C
Commercial (747C)	0°C to 70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT (Each Side)



Notes on following pages.

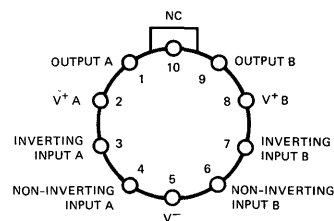
CONNECTION DIAGRAMS 14-LEAD DIP (TOP VIEW) PACKAGE OUTLINE 7A



ORDER INFORMATION

TYPE	PART NO.
747	747DM
747C	747DC

10-LEAD METAL CAN (TOP VIEW) PACKAGE OUTLINE 5F



ORDER INFORMATION

TYPE	PART NO.
747	747HM
747C	747HC

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A747

ELECTRICAL CHARACTERISTICS FOR 747 – Each Amplifier ($V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$ unless otherwise specified)

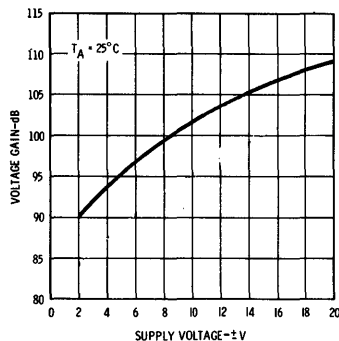
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		M Ω
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			± 15		mV
Large Signal Voltage Gain	$R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10$ V	50,000	200,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (Unity Gain)	Risetime	$V_{IN} = 20\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$		0.3	μs
	Overshoot			5.0	%
Slew Rate	$R_L \geq 2\text{ k}\Omega$		0.5		V/ μs
Channel Separation			120		dB

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$.

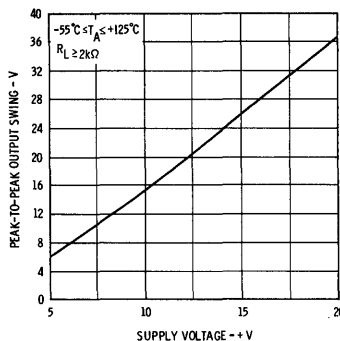
Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$		1.0	6.0	mV
Input Offset Current	$T_A = +125^\circ\text{C}$		7.0	200	nA
	$T_A = -55^\circ\text{C}$		85	500	nA
Input Bias Current	$T_A = +125^\circ\text{C}$		0.03	0.5	μA
	$T_A = -55^\circ\text{C}$		0.3	1.5	μA
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10\text{ k}\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{ k}\Omega$		30	150	$\mu\text{V/V}$
Large Signal Voltage Gain	$R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10$ V	25,000			V/V
Output Voltage Swing	$R_L \geq 10\text{ k}\Omega$	± 12	± 14		V
	$R_L \geq 2\text{ k}\Omega$	± 10	± 13		V
Supply Current	$T_A = +125^\circ\text{C}$		1.5	2.5	mA
	$T_A = -55^\circ\text{C}$		2.0	3.3	mA
Power Consumption	$T_A = +125^\circ\text{C}$		45	75	mW
	$T_A = -55^\circ\text{C}$		60	100	mW

TYPICAL PERFORMANCE CURVES (Each Amplifier) FOR 747 AND 747C

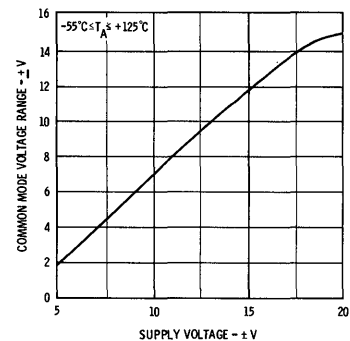
**OPEN LOOP VOLTAGE GAIN
AS A FUNCTION OF
SUPPLY VOLTAGE**



**OUTPUT VOLTAGE SWING
AS A FUNCTION OF
SUPPLY VOLTAGE**



**INPUT COMMON MODE
VOLTAGE RANGE AS A
FUNCTION OF SUPPLY VOLTAGE**



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A747

ELECTRICAL CHARACTERISTICS FOR 747C – Each Amplifier ($V_S = \pm 15$ V, $T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$		1.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		M Ω
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			± 15		mV
Large-Signal Voltage Gain	$R_L \geq 2 \text{ k}\Omega, V_{OUT} = \pm 10 \text{ V}$	25,000	200,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (Unity Gain)	Risetime	$V_{IN} = 20 \text{ mV}, R_L = 2 \text{ k}\Omega,$ $C_L \leq 100 \text{ pF}$	0.3		μs
	Overshoot		5.0		%
Slew Rate	$R_L \geq 2 \text{ k}\Omega$		0.5		V/ μs
Channel Separation			120		dB

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

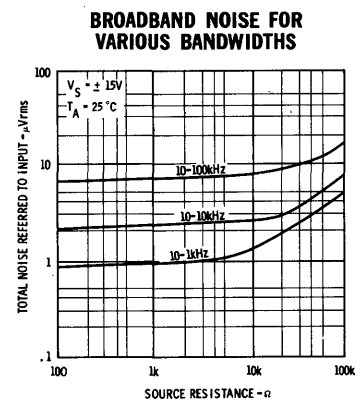
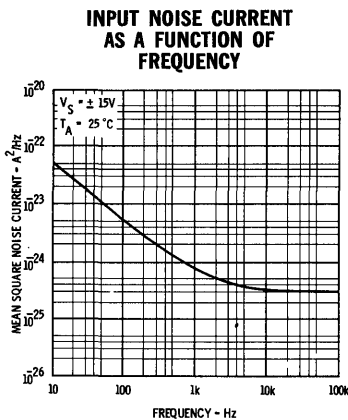
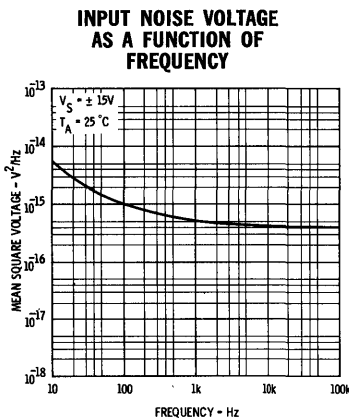
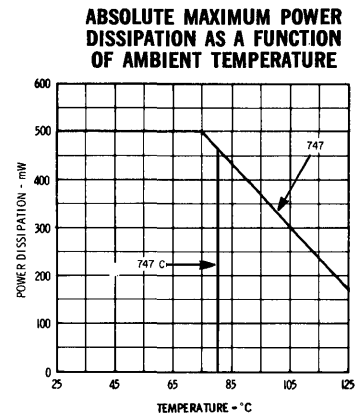
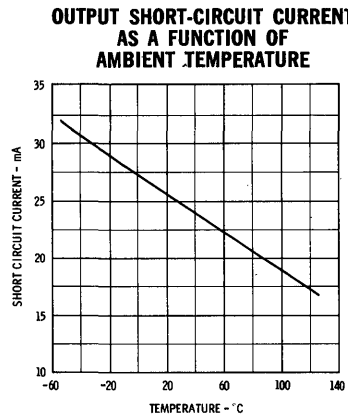
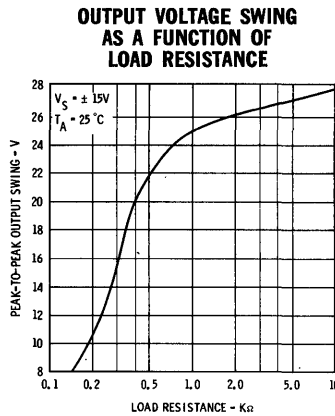
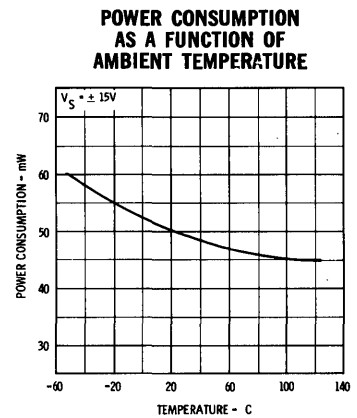
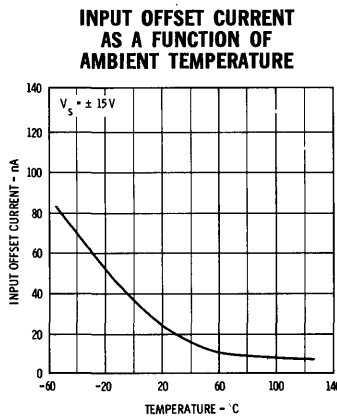
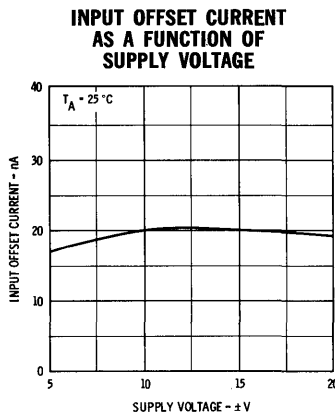
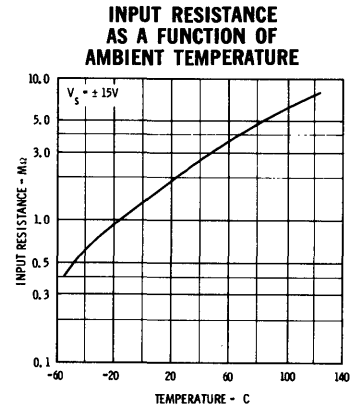
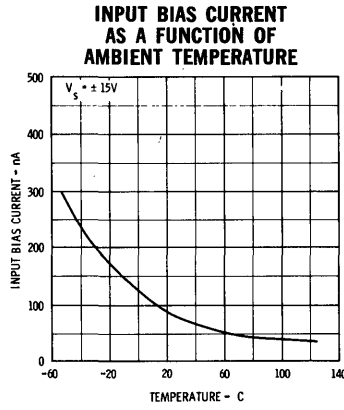
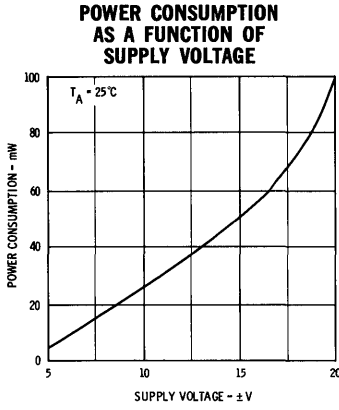
Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$		1.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			0.03	0.8	μA
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10 \text{ k}\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10 \text{ k}\Omega$		30	150	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	$R_L \geq 2 \text{ k}\Omega, V_{OUT} = \pm 10 \text{ V}$	15,000			V/V
	$R_L \geq 10 \text{ k}\Omega$	± 12	± 14		V
Output Voltage Swing	$R_L \geq 2 \text{ k}\Omega$	± 10	± 13		V
Supply Current			2.0	3.3	mA
Power Consumption			60	100	mW

NOTES

- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3 \text{ mW}/^\circ\text{C}$ for the Metal Can and $8.3 \text{ mW}/^\circ\text{C}$ for the DIP.
- For supply voltages less than $\pm 15 \text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply. Military rating applies to $+125^\circ\text{C}$ case temperature or $+60^\circ\text{C}$ ambient temperature for each side.

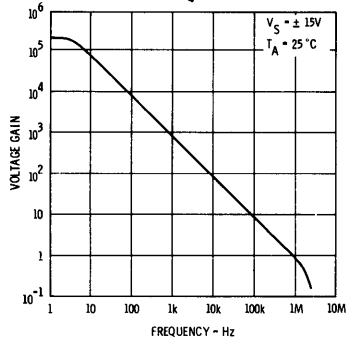
3

TYPICAL PERFORMANCE CURVES (Each Amplifier) FOR 747 AND 747C

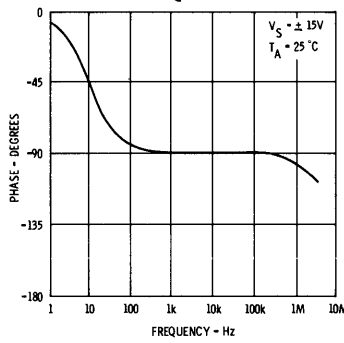


TYPICAL PERFORMANCE CURVES (Each Amplifier) FOR 747 AND 747C

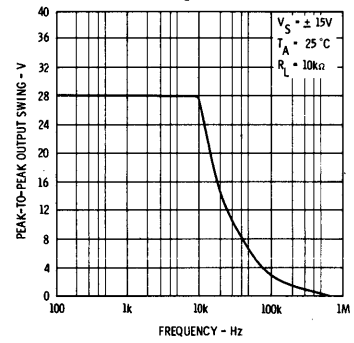
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



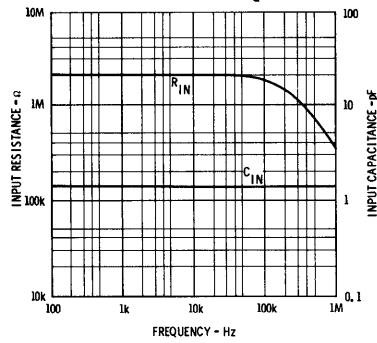
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



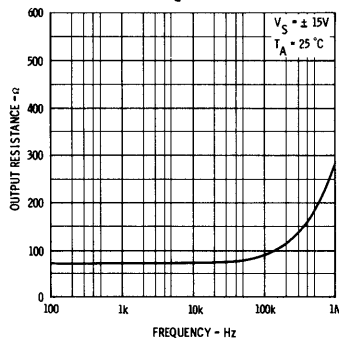
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



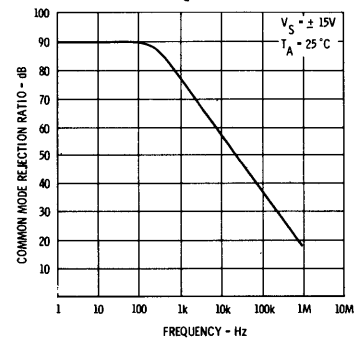
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



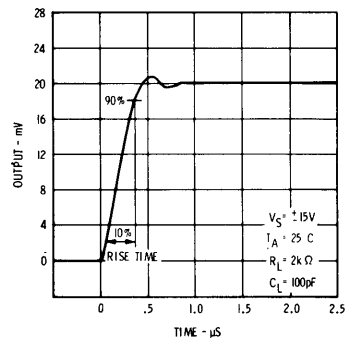
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



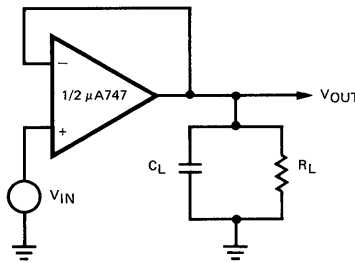
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



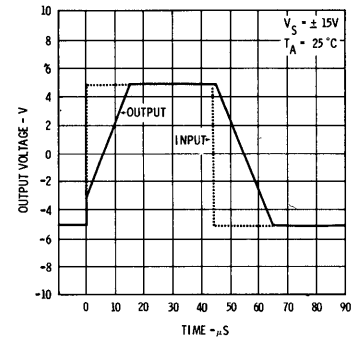
TRANSIENT RESPONSE



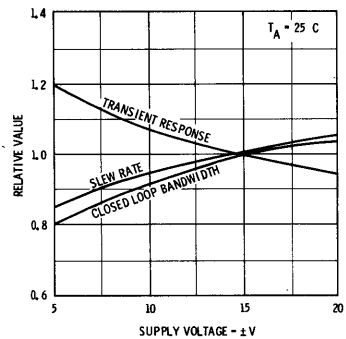
TRANSIENT RESPONSE TEST CIRCUIT



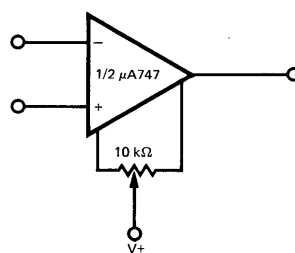
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



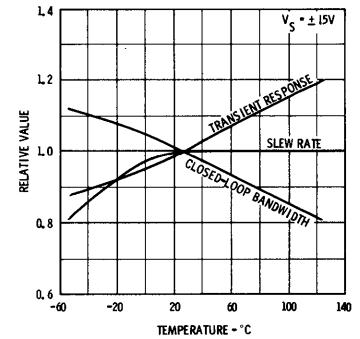
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

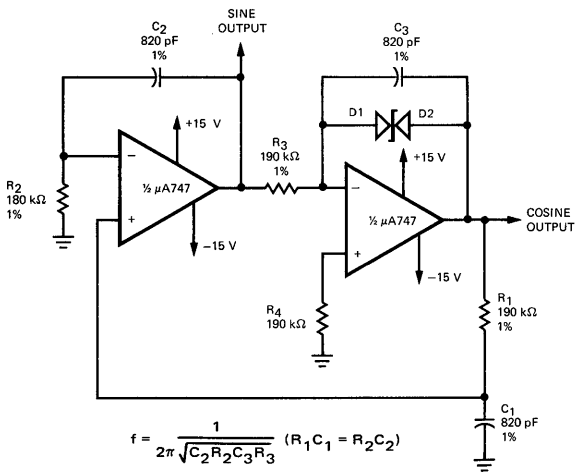


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

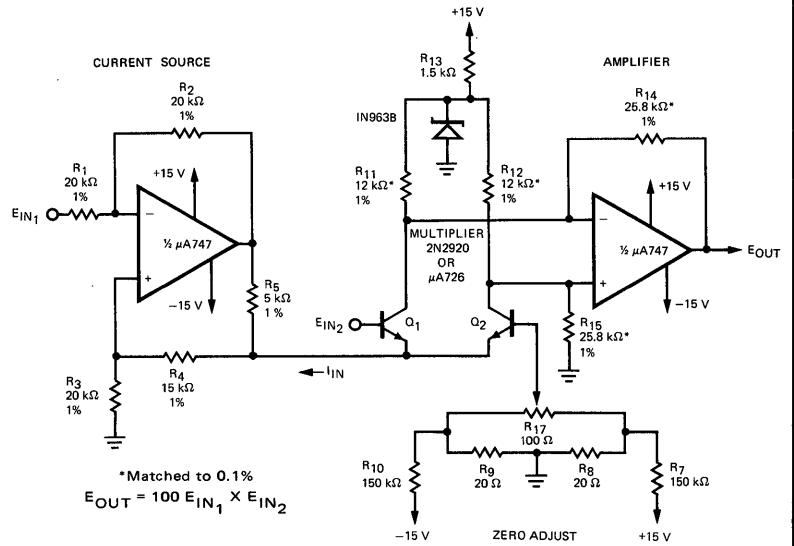


TYPICAL APPLICATIONS

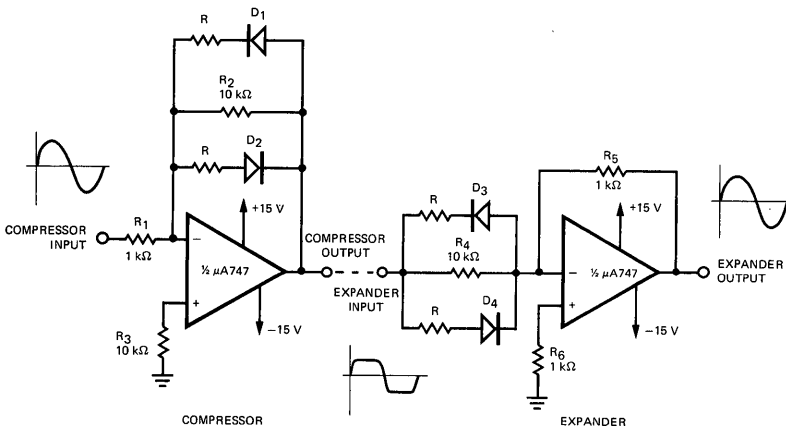
QUADRATURE OSCILLATOR



ANALOG MULTIPLIER

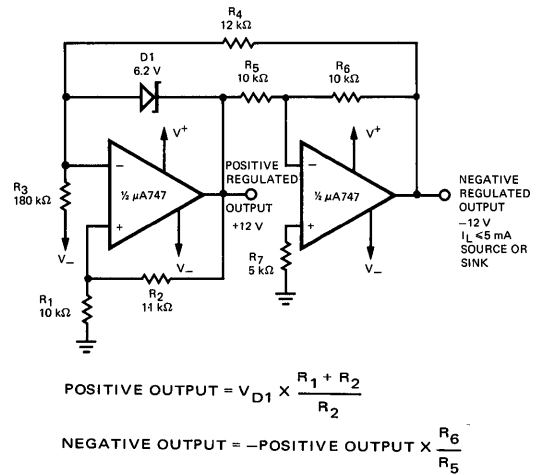


COMPRESSOR/EXPANDER AMPLIFIERS

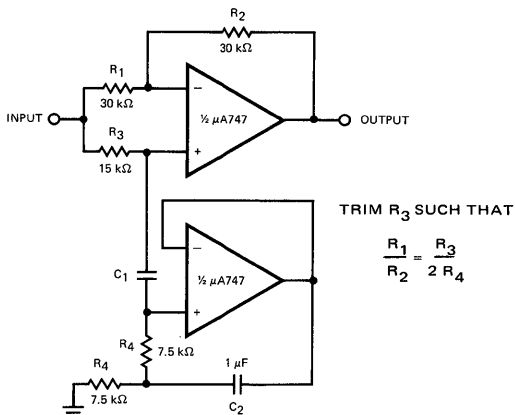


MAXIMUM COMPRESSION EXPANSION RATIO = R_1/R ($10 \text{ k}\Omega > R \geq 0$)
 NOTE: DIODES D_1 THROUGH D_4 ARE MATCHED FD6666 OR EQUIVALENT

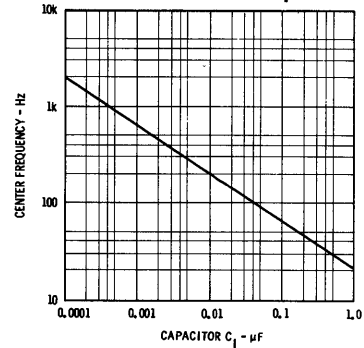
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES



NOTCH FILTER USING THE $\mu A747$ AS A GYRATOR

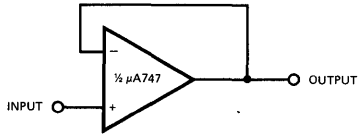


NOTCH FREQUENCY AS A FUNCTION OF C_1



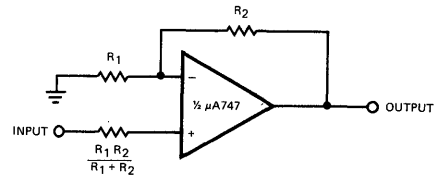
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



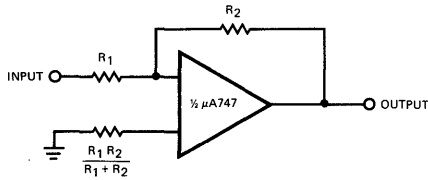
$R_{IN} = 400 \text{ M}\Omega$
 $C_{IN} = 1 \text{ pF}$
 $R_{OUT} \ll 1 \Omega$
 $BW = 1 \text{ MHz}$

NON-INVERTING AMPLIFIER



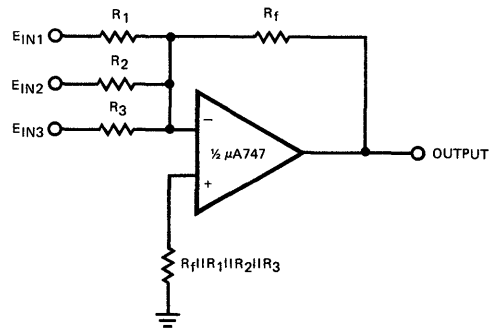
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 k Ω	9 k Ω	100 kHz	400 M Ω
100	100 Ω	9.9 k Ω	10 kHz	280 M Ω
1000	100 Ω	99.9 k Ω	1 kHz	80 M Ω

INVERTING AMPLIFIER



GAIN	R_1	R_2	BW	R_{IN}
1	10 k Ω	10 k Ω	1 MHz	10 k Ω
10	1 k Ω	10 k Ω	100 kHz	1 k Ω
100	1 k Ω	100 k Ω	10 kHz	1 k Ω
1000	100 Ω	100 k Ω	1 kHz	100 Ω

WEIGHTED AVERAGING AMPLIFIER



$$-E_{OUT} = E_{IN1} \left(\frac{R_f}{R_1} \right) + E_{IN2} \left(\frac{R_f}{R_2} \right) + E_{IN3} \left(\frac{R_f}{R_3} \right)$$

μA747A • μA747E

DUAL FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER

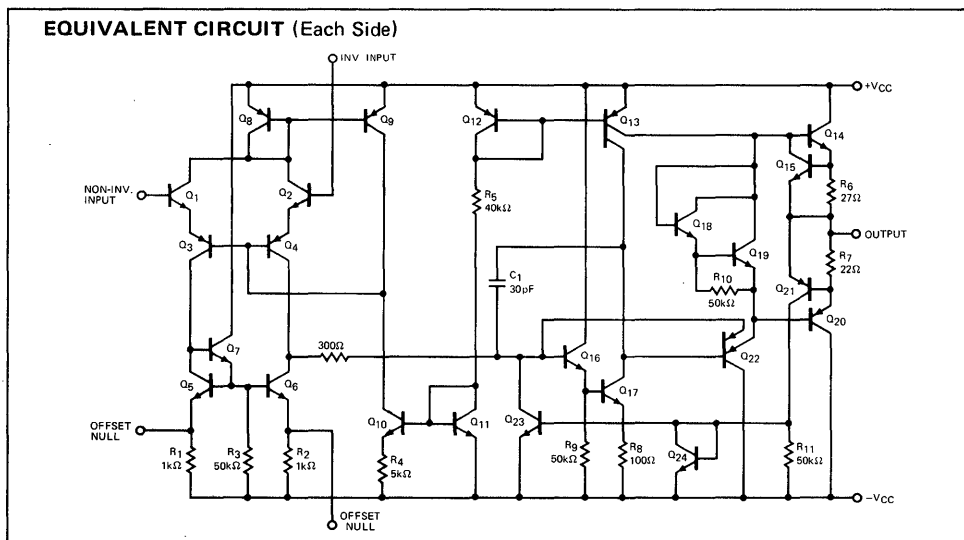
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA747A and E are pairs of high performance monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA747A and E ideal for use as voltage followers. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents. The μA747A and E are short-circuit protected and require no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. Electrical characteristics are identical to MIL-M-38510/10102.

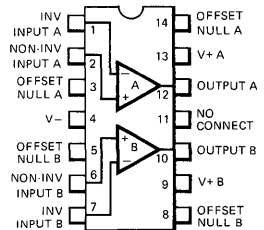
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **OFFSET VOLTAGE . . . 3.0 mV MAX**
- **OFFSET CURRENT . . . 30 nA MAX**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V ₋	±0.5 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (747A)	-55°C to +125°C
Commercial (747E)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

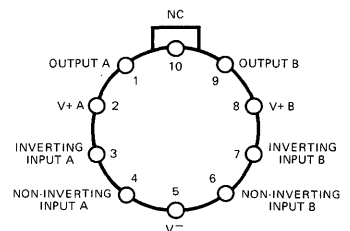


CONNECTION DIAGRAMS
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 7A



ORDER INFORMATION	
TYPE	PART NO.
747A	747ADM
747E	747EDC

10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F



ORDER INFORMATION	
TYPE	PART NO.
747A	747AHM
747E	747EHC

*Planar is a patented Fairchild Process.

747A

ELECTRICAL CHARACTERISTICS $\pm 5 \text{ V} \leq V_S \leq \pm 20 \text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50 \Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift				15	$\mu\text{V}/^\circ\text{C}$
Input Offset Current			3.0	30	nA
Average Input Offset Current Drift				0.5	$\text{nA}/^\circ\text{C}$
Input Bias Current			30	80	nA
Power Supply Rejection Ratio	$V_S = +10, -20; V_S = 20, -10 \text{ V}$ $R_S = 50 \Omega$		15	50	$\mu\text{V}/\text{V}$
Output Short Circuit Current		10	25	35	mA
Power Dissipation	$V_S = \pm 20 \text{ V}$		80	150	mW
Input Impedance	$V_S = \pm 20 \text{ V}$	1.0	6		$\text{M}\Omega$
Large Signal Voltage Gain	$V_S = \pm 20 \text{ V}$, $R_L = 2 \text{ k}\Omega$ $V_{\text{OUT}} = \pm 15 \text{ V}$	50			V/mV
Transient Response (Unity Gain)	Rise Time		0.25	0.8	μs
	Overshoot		6.0	20	%
Bandwidth (Note 4)		0.437	1.5		MHz
Slew Rate (Unity Gain)	$V_{\text{IN}} = \pm 10 \text{ V}$	0.3	0.7		$\text{V}/\mu\text{s}$

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

Input Offset Voltage				4.0	mV
Input Offset Current				70	nA
Input Bias Current				210	nA
Common Mode Rejection Ratio	$V_S = \pm 20 \text{ V}$, $V_{\text{IN}} = \pm 15 \text{ V}$ $R_S = 50 \Omega$	80	95		dB
Adjustment for Input Offset Voltage	$V_S = \pm 20 \text{ V}$	10			mV
Output Short Circuit Current		10		40	mA
Power Dissipation	$V_S = \pm 20 \text{ V}$	-55°C		165	mW
		$+125^\circ\text{C}$		135	mW
Input Impedance	$V_S = \pm 20 \text{ V}$	0.5			$\text{M}\Omega$
Output Voltage Swing	$V_S = \pm 20 \text{ V}$, $R_L = 10 \text{ k}\Omega$ $R_L = 2 \text{ k}\Omega$		± 16		V
			± 15		V
Large Signal Voltage Gain	$V_S = \pm 20 \text{ V}$, $R_L = 2 \text{ k}\Omega$, $V_{\text{OUT}} = \pm 15 \text{ V}$	32			V/mV
	$V_S = \pm 5 \text{ V}$, $R_L = 2 \text{ k}\Omega$, $V_{\text{OUT}} = \pm 2 \text{ V}$	10			V/mV
Channel Separation	$V_S = \pm 20 \text{ V}$	100			dB

NOTES:

- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3 \text{ mW}/^\circ\text{C}$ for the Metal Can, $8.3 \text{ mW}/^\circ\text{C}$ for the DIP.
- For supply voltages less than $\pm 15 \text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply. Rating applies to $+125^\circ\text{C}$ case temperature or 75°C ambient temperature.

4. Calculated value from: $\text{BW (MHz)} = \frac{0.35}{\text{RISETIME } (\mu\text{s})}$

747E

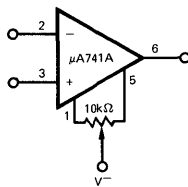
ELECTRICAL CHARACTERISTICS ($\pm 5\text{ V} \leq V_S \leq \pm 20\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ \Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift				15	$\mu\text{V}/^\circ\text{C}$
Input Offset Current			3	30	nA
Average Input Offset Current Drift				0.5	$\text{nA}/^\circ\text{C}$
Input Bias Current			30	80	nA
Power Supply Rejection Ratio	$V_S = +10, -20; V_S = 20, -10\text{ V}$ $R_S = 50\ \Omega$		15	50	$\mu\text{V}/\text{V}$
Output Short Circuit Current		10	25	35	mA
Power Dissipation	$V_S = \pm 20\text{ V}$		80	150	mW
Input Impedance	$V_S = \pm 20\text{ V}$	1.0	6		$\text{M}\Omega$
Large Signal Voltage Gain	$V_S = \pm 20\text{ V}, R_L = 2\ \text{k}\Omega, V_{\text{OUT}} = \pm 15\text{ V}$	50			V/mV
Transient Response (Unity Gain)	Rise Time		0.25	0.8	μs
	Overshoot		6	20	%
Bandwidth (Note 4)		0.45	1.5		MHz
Slew Rate (Unity Gain)	$V_{\text{IN}} = \pm 10\text{ V}$	0.3	0.7		$\text{V}/\mu\text{s}$

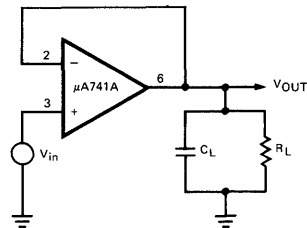
The following specifications apply for $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$

Input Offset Voltage				4.0	mV
Input Offset Current				70	nA
Input Bias Current				210	nA
Common Mode Rejection Ratio	$V_S = \pm 20\text{ V}, V_{\text{IN}} = \pm 15\text{ V}$ $R_S = 50\ \Omega$	80	95		dB
Adjustment for Input Offset Voltage	$V_S = \pm 20\text{ V}$	10			mV
Output Short Circuit Current		10		40	mA
Power Dissipation	$V_S = \pm 20\text{ V}$			165	mW
Input Impedance	$V_S = \pm 20\text{ V}$	0.5			$\text{M}\Omega$
Output Voltage Swing	$V_S = \pm 20\text{ V}, R_L = 10\ \text{k}\Omega$	± 16			V
	$R_L = 2\ \text{k}\Omega$	± 15			V
Large Signal Voltage Gain	$V_S = \pm 20\text{ V}, R_L = 2\ \text{k}\Omega, V_{\text{OUT}} = \pm 15\text{ V}$	32			V/mV
	$V_S = \pm 5\text{ V}, R_L = 2\ \text{k}\Omega, V_{\text{OUT}} = \pm 2\text{ V}$	10			V/mV
Channel Separation	$V_S = \pm 20\text{ V}$	100			dB

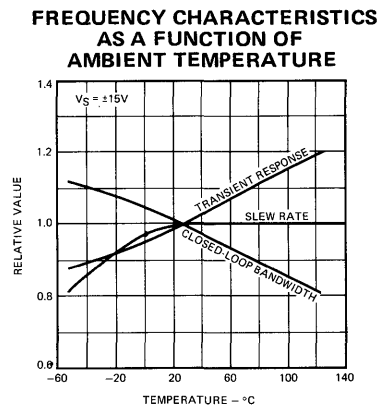
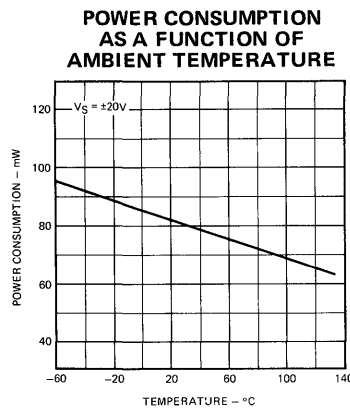
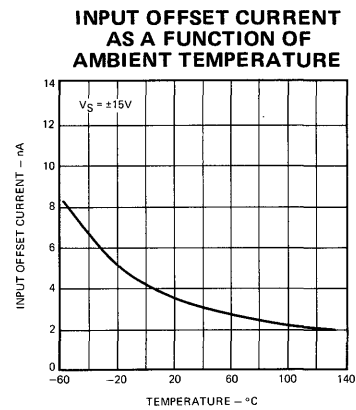
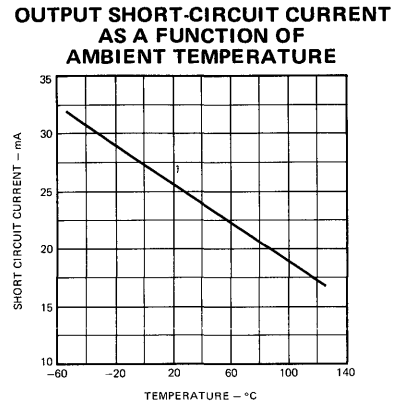
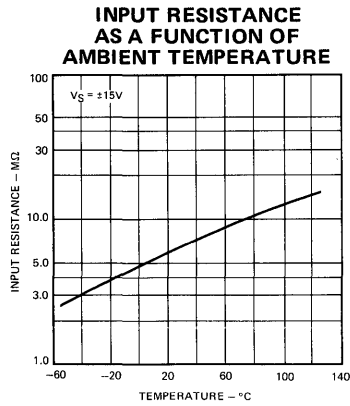
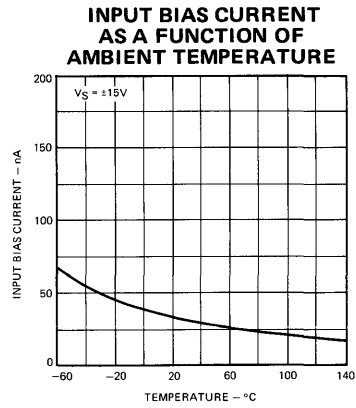
VOLTAGE OFFSET NULL CIRCUIT



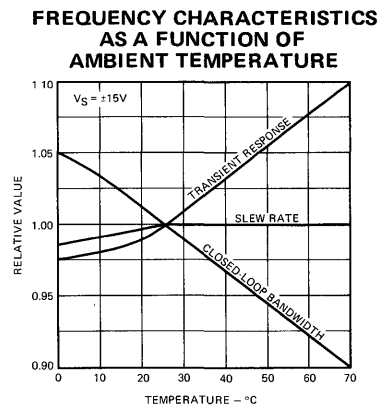
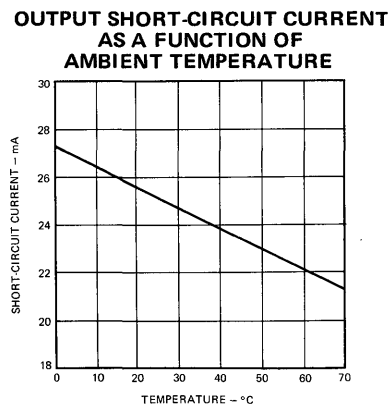
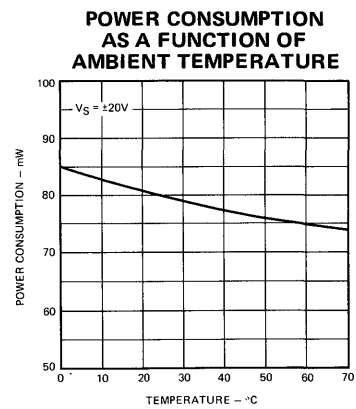
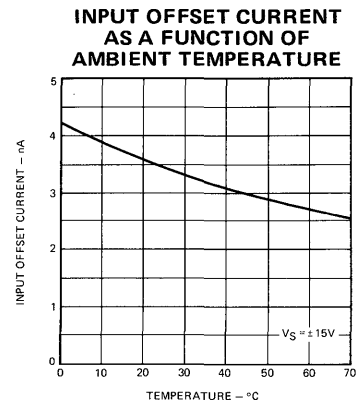
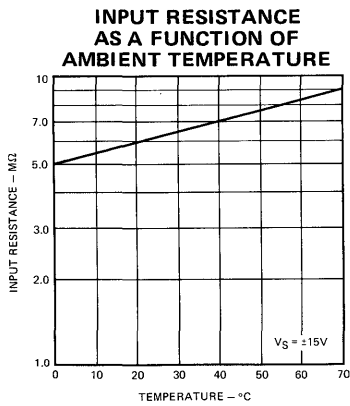
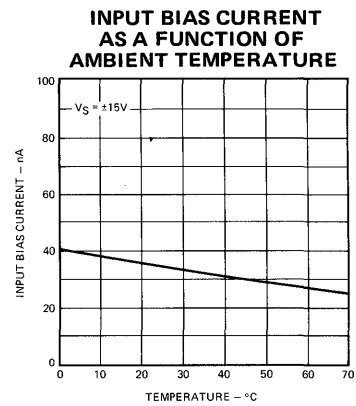
TRANSIENT RESPONSE TEST CIRCUIT



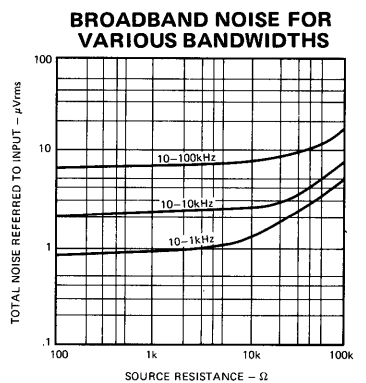
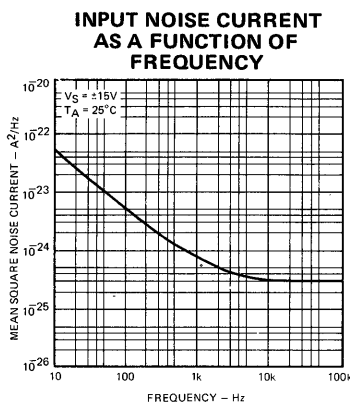
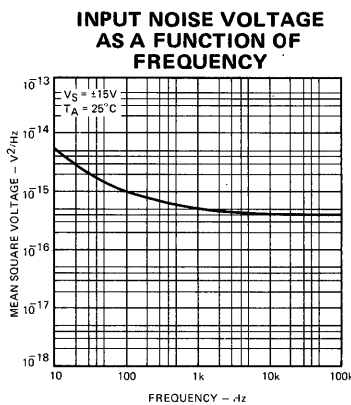
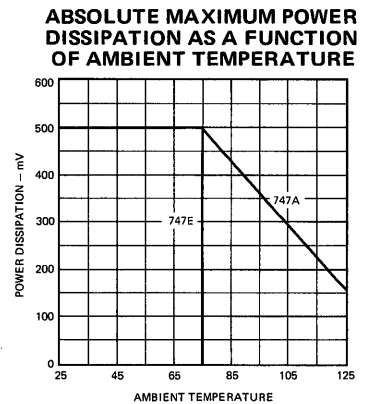
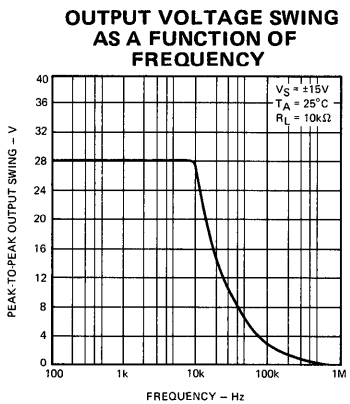
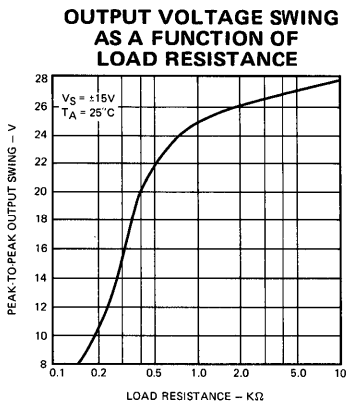
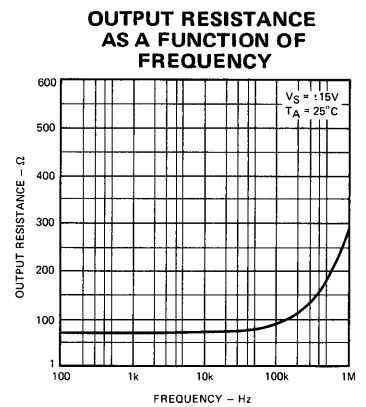
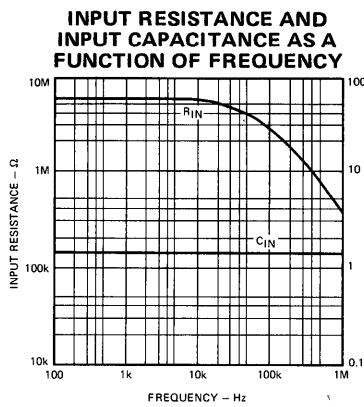
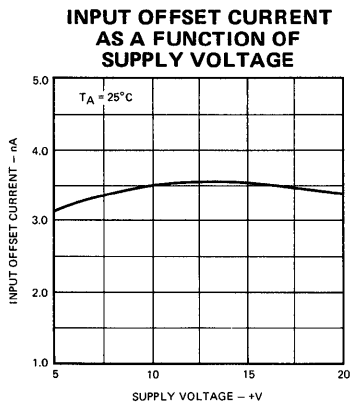
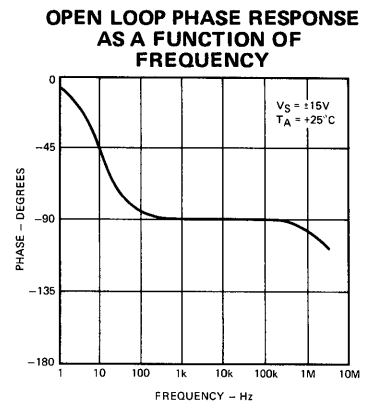
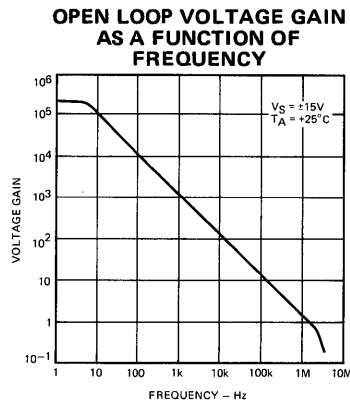
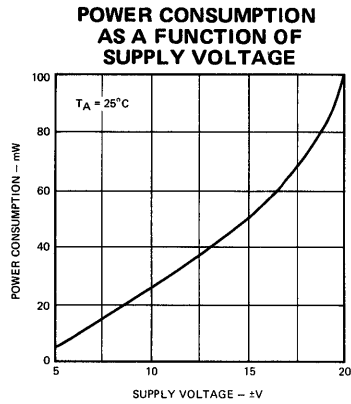
TYPICAL PERFORMANCE CURVES FOR 747A



TYPICAL PERFORMANCE CURVES FOR 747E



TYPICAL PERFORMANCE CURVES FOR 747A AND 747E



μA748

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

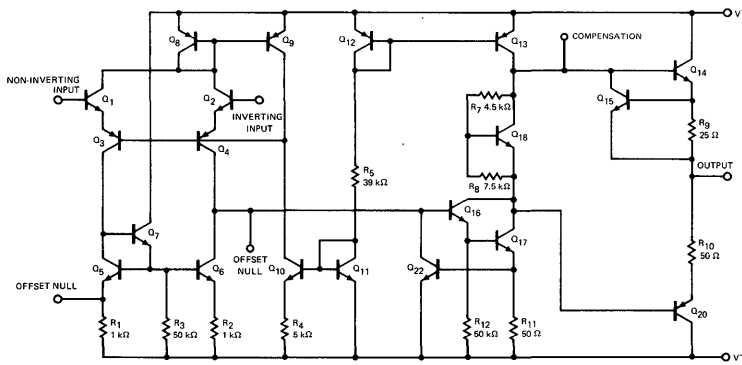
GENERAL DESCRIPTION — The μA748 is a High Performance Monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a high wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the μA748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA748 is short-circuit protected and has the same pin configuration as the popular μA741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. For superior performance, see μA777 data sheet.

- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

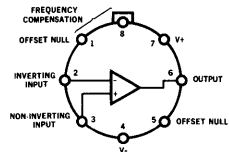
Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	-65°C to +150°C
Mini DIP	-55°C to +125°C
Operating Temperature Range	
Military (748)	-55°C to +125°C
Commercial (748C)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can, DIP and Flatpak	300°C
Mini DIP	260°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



Notes on following pages.

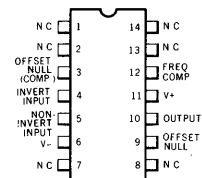
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B



NOTE: Pin 4 connected to case

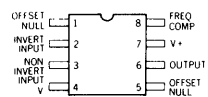
ORDER INFORMATION	
TYPE	PART NO.
748	748HM
748C	748HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



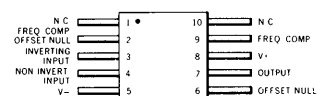
ORDER INFORMATION	
TYPE	PART NO.
748	748DM
748C	748DC

8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



ORDER INFORMATION	
TYPE	PART NO.
748C	748TC

10-LEAD FLATPAK ‡
(TOP VIEW)
PACKAGE OUTLINE 3F



‡ Available on special request

ORDER INFORMATION	
TYPE	PART NO.
748	748FM

*Planar is a patented Fairchild process.

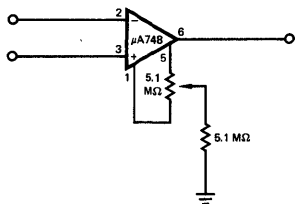
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25^\circ$ C, $C_C = 30$ pF unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ k Ω		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		M Ω
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			± 15		mV
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	50,000	150,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1)	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ k Ω , $C_L \leq 100$ pF	Risetime	0.3		μ s
		Overshoot	5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ k Ω		0.5		V/ μ s
Transient Response (Voltage Follower, Gain of 10)	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ k Ω , $C_L \leq 100$ pF	Risetime	0.2		μ s
		Overshoot	5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ k Ω , $C_C = 3.5$ pF		5.5		V/ μ s

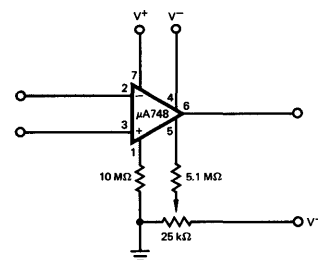
The following specifications apply for -55° C $\leq T_A \leq +125^\circ$ C:

Input Offset Voltage	$R_S \leq 10$ k Ω		1.0	6.0	mV
Input Offset Current	$T_A = +125^\circ$ C		10	200	nA
	$T_A = -55^\circ$ C		50	500	nA
Input Bias Current	$T_A = +125^\circ$ C		0.03	0.5	μ A
	$T_A = -55^\circ$ C		0.3	1.5	μ A
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ k Ω		30	150	μ V/V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	25,000			V/V
Output Voltage Swing	$R_L \geq 10$ k Ω	± 12	± 14		V
	$R_L \geq 2$ k Ω	± 10	± 13		V
Supply Current	$T_A = +125^\circ$ C		1.5	2.5	mA
	$T_A = -55^\circ$ C		2.0	3.3	mA
Power Consumption	$T_A = +125^\circ$ C		45	75	mW
	$T_A = -55^\circ$ C		60	100	mW

**VOLTAGE OFFSET
NULL CIRCUIT**



SUGGESTED



ALTERNATE

748C

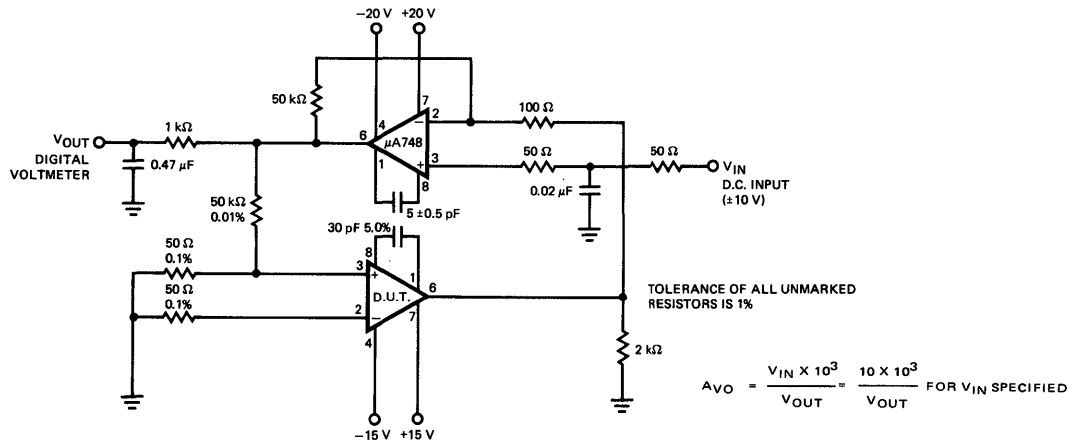
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25^\circ$ C, $C_C = 30$ pF unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ k Ω		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		M Ω
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			± 15		mV
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	20,000	150,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1)	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ k Ω , $C_L \leq 100$ pF	Risetime	0.3		μ s
		Overshoot	5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ k Ω		0.5		V/ μ s
Transient Response (Voltage Follower, Gain of 10)	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ k Ω , $C_L \leq 100$ pF	Risetime	0.2		μ s
		Overshoot	5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ k Ω		5.5		V/ μ s

The following specifications apply for 0° C $\leq T_A \leq +70^\circ$ C:

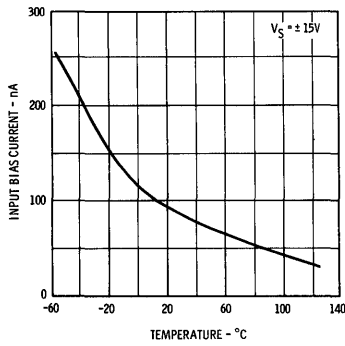
Input Offset Voltage	$R_S \leq 10$ k Ω			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ k Ω		30	150	μ V/V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	15,000			V/V
Output Voltage Swing	$R_L \geq 10$ k Ω	± 12	± 14		V
	$R_L \geq 2$ k Ω	± 10	± 13		V
Power Consumption			60	100	mW

GAIN TEST CIRCUIT

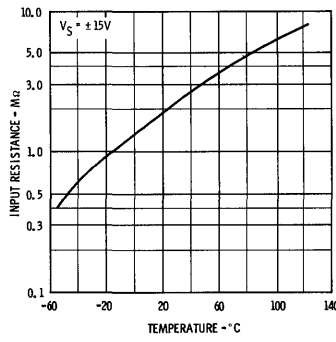


TYPICAL PERFORMANCE CURVES FOR 748

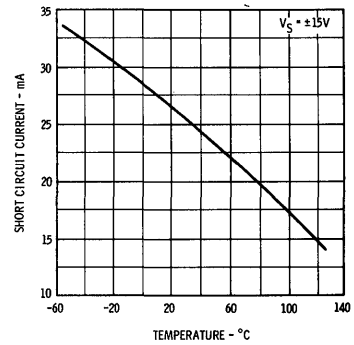
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



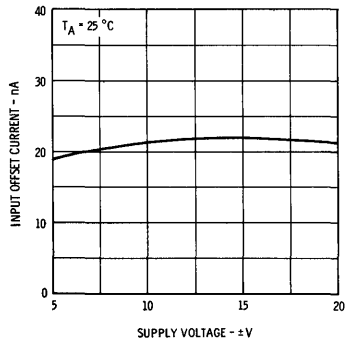
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



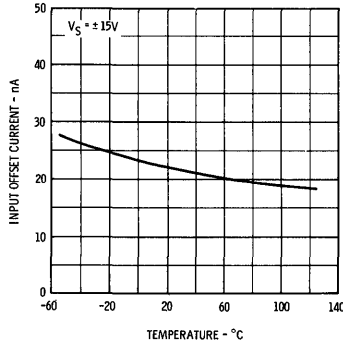
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



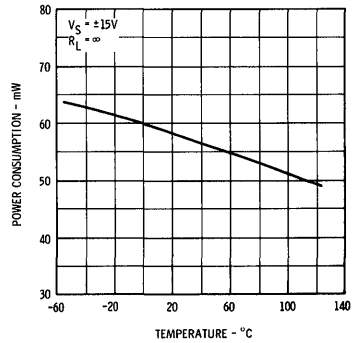
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

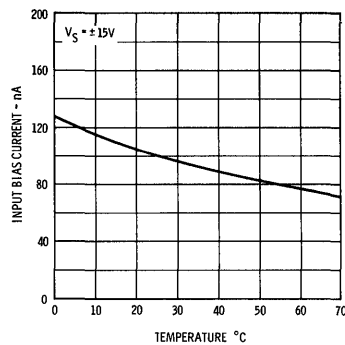


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

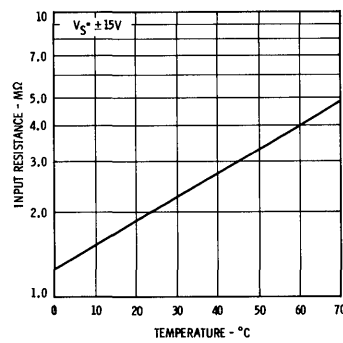


TYPICAL PERFORMANCE CURVES FOR 748C

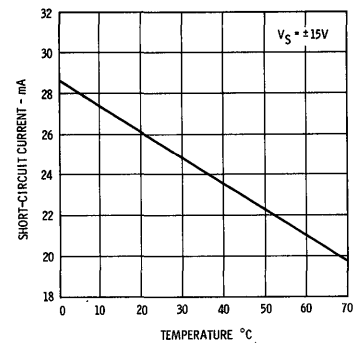
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



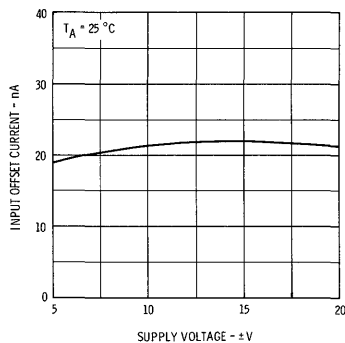
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



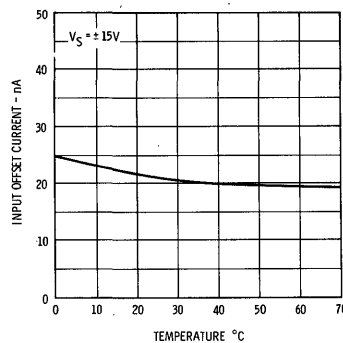
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



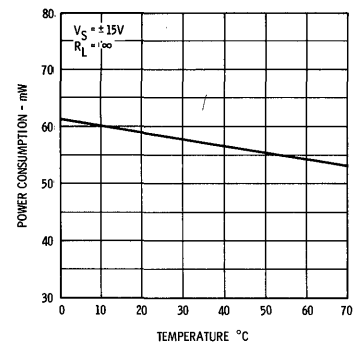
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

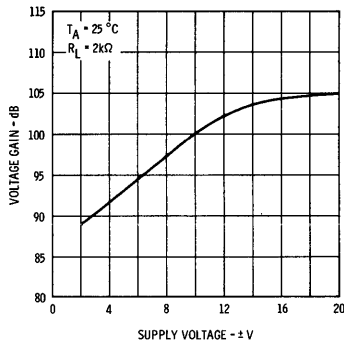


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

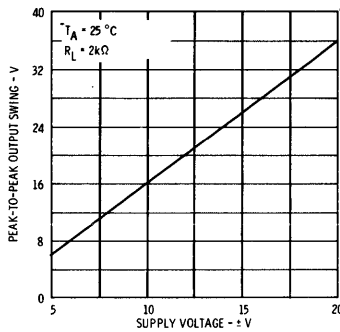


TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

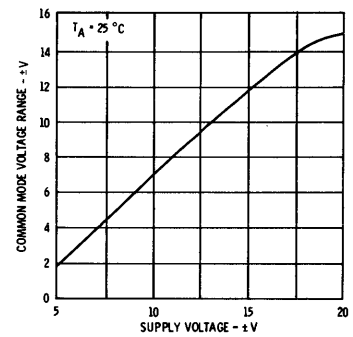
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



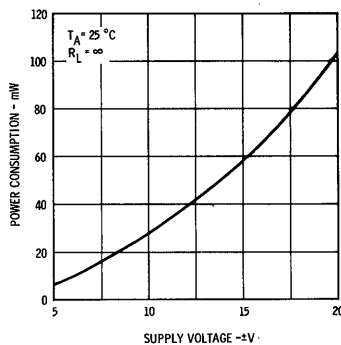
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



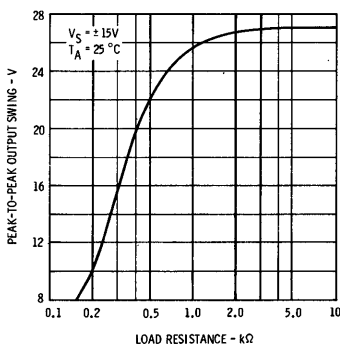
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



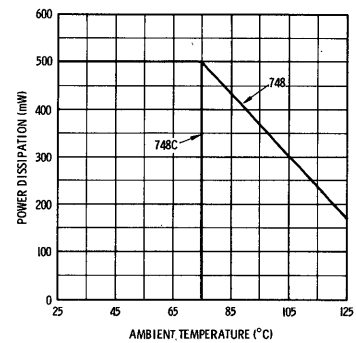
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



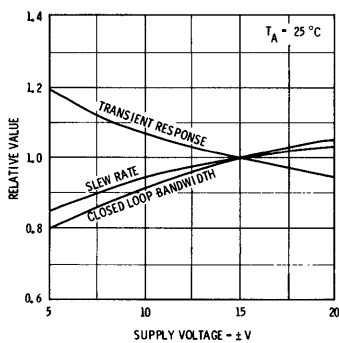
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



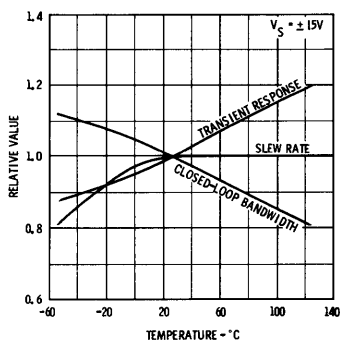
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



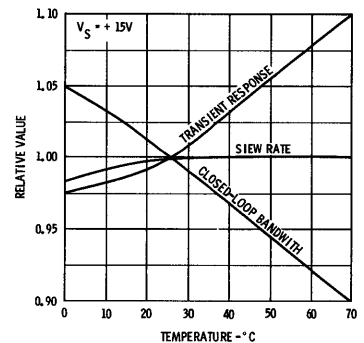
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



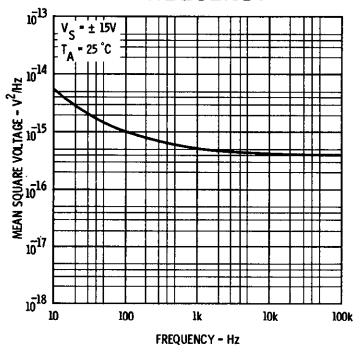
748 FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



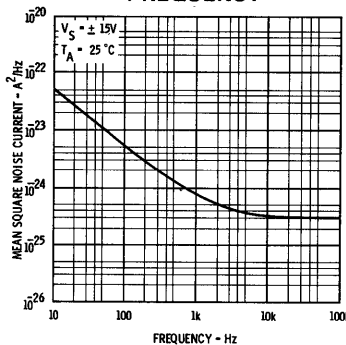
748C FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



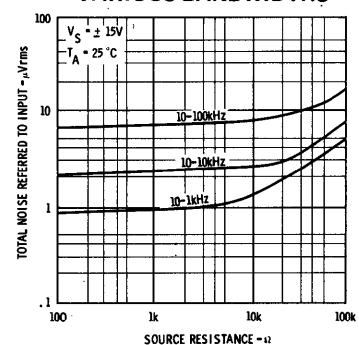
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

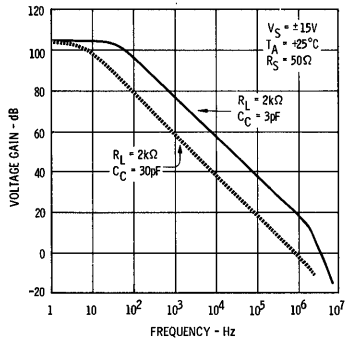


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

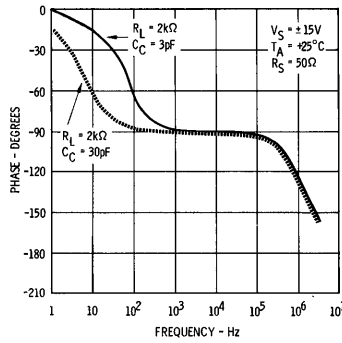


TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

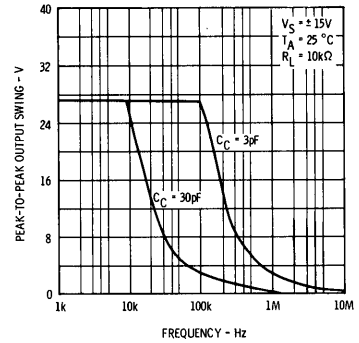
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



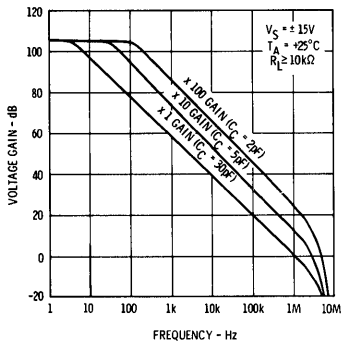
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



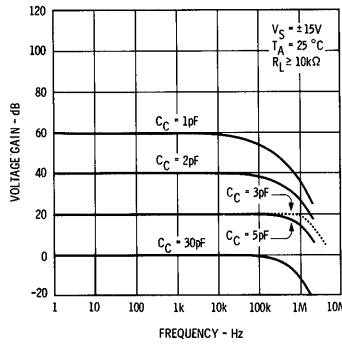
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



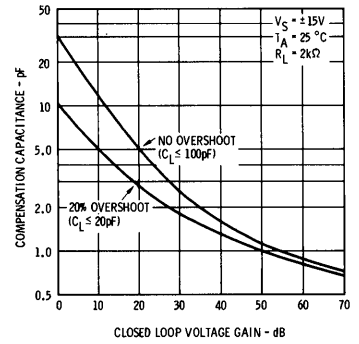
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



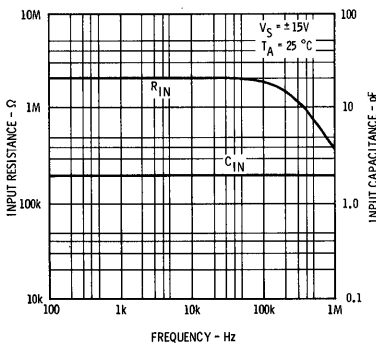
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



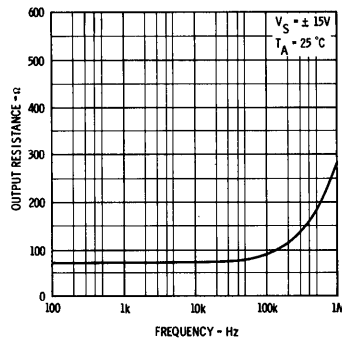
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



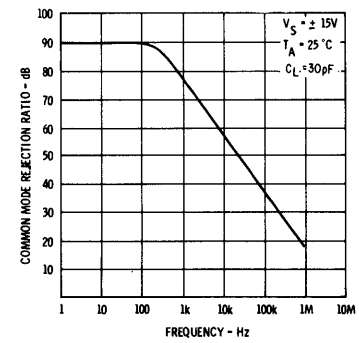
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



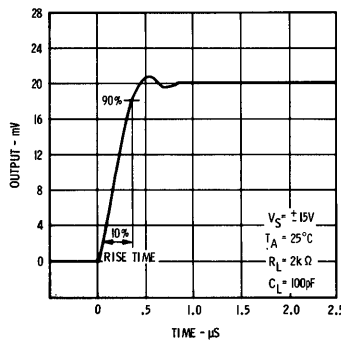
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



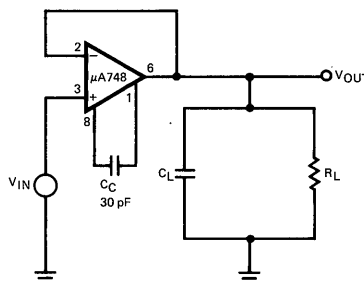
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



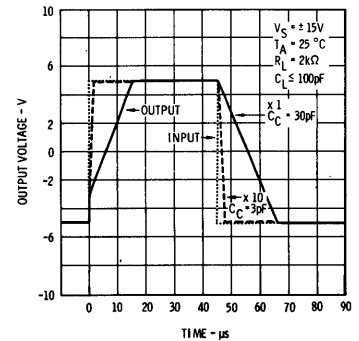
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

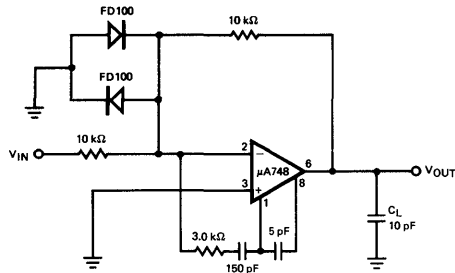


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

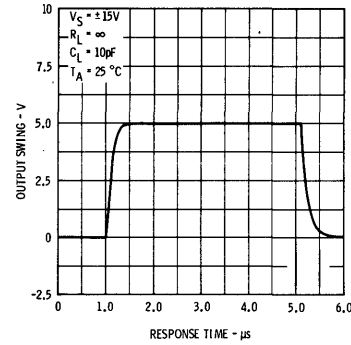


TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

FEED-FORWARD COMPENSATION

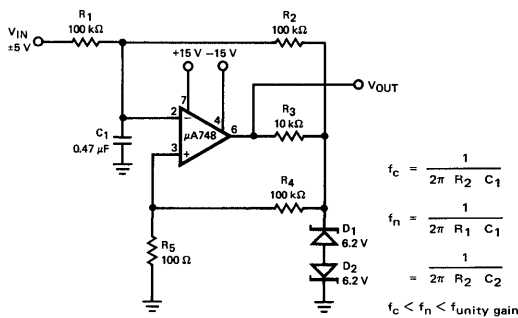


LARGE SIGNAL FEED-FORWARD TRANSIENT RESPONSE

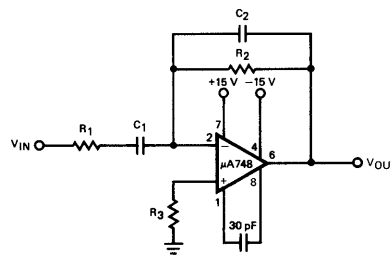


TYPICAL APPLICATIONS

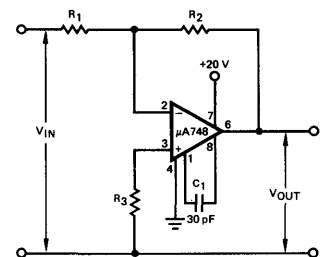
PULSE WIDTH MODULATOR



PRACTICAL DIFFERENTIATOR



CIRCUIT FOR OPERATING THE $\mu A748$ WITHOUT A NEGATIVE SUPPLY



NOTES

1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP, 5.6 mW/°C for the Mini DIP and 7.1 mW/°C for the Flatpak.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C case temperature or +75°C ambient temperature.

μA776

MULTI-PURPOSE PROGRAMMABLE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

DESCRIPTION — The μA776 Programmable Operational Amplifier is constructed using the Fairchild Planar* epitaxial process. High input impedance, low supply currents, and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano-watt power consumption or for characteristics similar to the μA741. Internal frequency compensation, absence of latch up, high slew rate and short circuit current protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

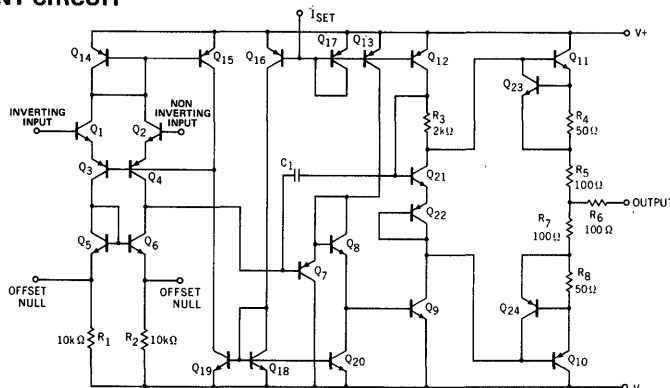
- **MICROPOWER CONSUMPTION**
- **±1.2V to ±18V OPERATION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **LOW INPUT BIAS CURRENTS**
- **WIDE PROGRAMMING RANGE**

- **HIGH SLEW RATE**
- **LOW NOISE**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET NULL CAPABILITY**
- **NO LATCH UP**

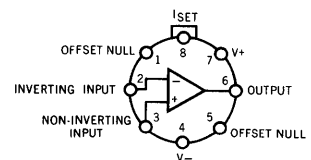
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage Between Offset Null and V-	±0.5 V
I _{SET} (Maximum Current at I _{SET})	500 μA
V _{SET} (Maximum Voltage to Ground at I _{SET})	(V ₊ - 2.0 V) ≤ V _{SET} ≤ V ₊
Storage Temperature Range	
Metal Can, DIP	-65°C to +150°C
Mini DIP	-55°C to +125°C
Operating Temperature Range	
Military (776)	-55°C to +125°C
Commercial (776C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	
Metal Can, DIP	300°C
Mini DIP	260°C
Output Short-Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



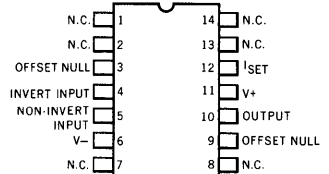
CONNECTION DIAGRAMS 8-LEAD METAL CAN (TOP VIEW) PACKAGE OUTLINE 5B



ORDER INFORMATION

TYPE	PART NO.
776	776HM
776C	776HC

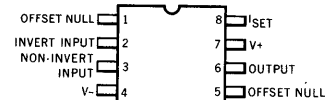
14-LEAD DIP (TOP VIEW) PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
776	776DM
776C	776DC

8-LEAD MINI DIP (TOP VIEW) PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
776C	776TC

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A776

± 15 VOLT OPERATION FOR 776

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Unless Otherwise Specified)

PARAMETERS	CONDITIONS	$I_{SET} = 1.5\mu\text{A}$			$I_{SET} = 15\mu\text{A}$			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 10\text{k}\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current	$R_S \leq 10\text{k}\Omega$		0.7	3.0		2.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		M Ω
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75\text{k}\Omega, V_{OUT} = \pm 10\text{V}$	200k	400k					V/V
	$R_L \geq 5\text{k}\Omega, V_{OUT} = \pm 10\text{V}$				100k	400k		V/V
Output Resistance			5.0k			1.0k		Ω
Output Short-Circuit Current			3.0			12		mA
Supply Current			20	25		160	180	μA
Power Consumption				0.75			5.4	mW
Transient Response (unity gain)	$V_{IN} = 20\text{mV}, R_L \geq 5\text{k}\Omega,$ $C_L = 100\text{pF}$	Risetime		1.6		0.35		μs
		Overshoot		0		10		%
Slew Rate	$R_L \geq 5\text{k}\Omega$		0.1			0.8		V/ μs
Output Voltage Swing	$R_L \geq 75\text{k}\Omega$	± 12	± 14					V
	$R_L \geq 5\text{k}\Omega$				± 10	± 13		V

The following specifications apply $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

Input Offset Voltage	$R_S \leq 10\text{k}\Omega$			6.0			6.0	mV
Input Offset Current	$T_A = +125^\circ\text{C}$			5.0			15	nA
	$T_A = -55^\circ\text{C}$			10			40	nA
Input Bias Current	$T_A = +125^\circ\text{C}$			7.5			50	nA
	$T_A = -55^\circ\text{C}$			20			120	nA
Input Voltage Range		± 10				± 10		V
Common Mode Rejection Ratio	$R_S \leq 10\text{k}\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{k}\Omega$		25	150		25	150	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	$R_L \geq 75\text{k}\Omega, V_{OUT} = \pm 10\text{V}$	100k			75k			V/V
Output Voltage Swing	$R_L \geq 75\text{k}\Omega$	± 10			± 10			V
Supply Current				30			200	μA
Power Consumption				0.9			6.0	mW

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A776

± 3 VOLT OPERATION FOR 776

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Unless Otherwise Specified)

PARAMETERS	CONDITIONS	$I_{SET} = 1.5\mu\text{A}$			$I_{SET} = 15\mu\text{A}$			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current			0.7	3.0		2.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		M Ω
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega, V_{OUT} = \pm 1V$	50k	200k					V/V
	$R_L \geq 5k\Omega, V_{OUT} = \pm 1V$				50k	200k		V/V
Output Resistance			5k			1k		Ω
Output Short-Circuit Current			3.0			5.0		mA
Supply Current			13	20		130	160	μA
Power Consumption			78	120		780	960	μW
Transient Response (unity gain)	$V_{IN} = 20\text{mV}, R_L \geq 5k\Omega,$ $C_L \leq 100\text{pF}$	Risetime		3.0		0.6		μs
		Overshoot		0		5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/ μs

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current	$T_A = +125^\circ\text{C}$			5.0			15	nA
	$T_A = -55^\circ\text{C}$			10			40	nA
Input Bias Current	$T_A = +125^\circ\text{C}$			7.5			50	nA
	$T_A = -55^\circ\text{C}$			20			120	nA
Input Voltage Range		± 1.0				± 1.0		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	150		25	150	$\mu\text{V/V}$
Large Signal Voltage Gain	$R_L \geq 75k\Omega, V_{OUT} = \pm 1V$	25k						V/V
	$R_L \geq 5k\Omega, V_{OUT} = \pm 1V$				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	± 2.0	± 2.4					V
	$R_L \geq 5k\Omega$				± 1.9	± 2.1		V
Supply Current				25			180	μA
Power Consumption				150			1080	μW

NOTES

1. Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3 \text{ mW}/^\circ\text{C}$ for Metal Can, $8.3 \text{ mW}/^\circ\text{C}$ for the DIP, and $5.6 \text{ mW}/^\circ\text{C}$ for the Mini DIP.
2. For supply voltages less than $\pm 15 \text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
3. Short Circuit may be to ground or either supply. Rating applies to $+125^\circ\text{C}$ case temperature or $+75^\circ\text{C}$ ambient temperature for $I_{SET} \leq 30 \mu\text{A}$.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A776

± 15 VOLT OPERATION FOR 776C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Unless Otherwise Specified)

PARAMETERS	CONDITIONS	$I_{SET} = 1.5\mu\text{A}$			$I_{SET} = 15\mu\text{A}$			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 10\text{k}\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		2.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		M Ω
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75\text{k}\Omega, V_{OUT} = \pm 10\text{V}$	50k	400k					V/V
	$R_L \geq 5\text{k}\Omega, V_{OUT} = \pm 10\text{V}$				50k	400k		V/V
Output Resistance			5.0			1.0		k Ω
Output Short-Circuit Current			3.0			12		mA
Supply Current			20	30		160	190	μA
Power Consumption				0.9			5.7	mW
Transient Response (unity gain)	$V_{IN} = 20\text{mV}, R_L \geq 5\text{k}\Omega,$ $C_L \leq 100\text{pF}$	Risetime		1.6		0.35		μs
		Overshoot		0		10		%
Slew Rate	$R_L \geq 5\text{k}\Omega$		0.1			0.8		V/ μs
Output Voltage Swing	$R_L \geq 75\text{k}\Omega$	± 12	± 14					V
	$R_L \geq 5\text{k}\Omega$				± 10	± 13		V

The following specifications apply to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$

Input Offset Voltage	$R_S \leq 10\text{k}\Omega$		7.5			7.5		mV
Input Offset Current	$T_A = +70^\circ\text{C}$		6.0			25		nA
	$T_A = 0^\circ\text{C}$		10			40		nA
Input Bias Current	$T_A = +70^\circ\text{C}$		10			50		nA
	$T_A = 0^\circ\text{C}$		20			100		nA
Input Voltage Range		± 10			± 10			V
Common Mode Rejection Ratio	$R_S \leq 10\text{k}\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{k}\Omega$		25	200		25	200	$\mu\text{V/V}$
Large Signal Voltage Gain	$R_L \geq 75\text{k}\Omega, V_{OUT} = \pm 10\text{V}$	50k			50k			V/V
Output Voltage Swing	$R_L \geq 75\text{k}\Omega$	± 10			± 10			V
Supply Current			35			200		μA
Power Consumption			1.05			6.0		mW

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A776

± 3 VOLT OPERATION FOR 776C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Unless Otherwise Specified)

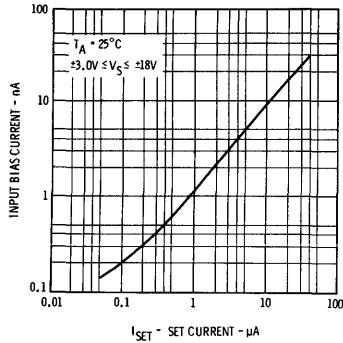
PARAMETERS	CONDITIONS	$I_{SET} = 1.5\mu\text{A}$			$I_{SET} = 15\mu\text{A}$			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 10\text{k}\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		2.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		M Ω
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75\text{k}\Omega, V_{OUT} = \pm 1\text{V}$	25k	200k					V/V
	$R_L \geq 5\text{k}\Omega, V_{OUT} = \pm 1\text{V}$				25 k	200k		V/V
Output Resistance			5.0			1.0		k Ω
Output Short-Circuit Current			3.0			5.0		mA
Supply Current			13	20		130	170	μA
Power Consumption			78	120		780	1020	μW
Transient Response (unity gain)	$V_{IN} = 20\text{mV}, R_L \geq 5\text{k}\Omega,$ $C_L = 100\text{pF}$	Risetime		3.0		0.6		μs
		Overshoot		0		5		%
Slew Rate	$R_L \geq 5\text{k}\Omega$		0.03			0.35		V/ μs

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$

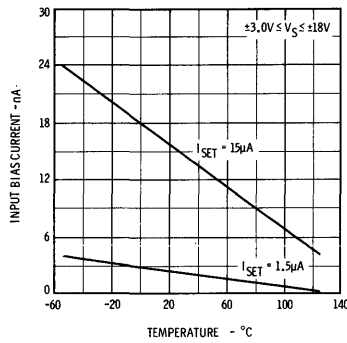
Input Offset Voltage	$R_S \leq 10\text{k}\Omega$			7.5			7.5	mV
Input Offset Current	$T_A = +70^\circ\text{C}$			6.0			25	nA
	$T_A = 0^\circ\text{C}$			10			40	nA
Input Bias Current	$T_A = +70^\circ\text{C}$			10			50	nA
	$T_A = 0^\circ\text{C}$			20			100	nA
Input Voltage Range		± 1.0				± 1.0		V
Common Mode Rejection Ratio	$R_S \leq 10\text{k}\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{k}\Omega$		25	200		25	200	$\mu\text{V/V}$
Large Signal Voltage Gain	$R_L \geq 75\text{k}\Omega, V_{OUT} = \pm 1\text{V}$	25k						V/V
	$R_L \geq 5\text{k}\Omega, V_{OUT} = \pm 1\text{V}$				25k			V/V
Output Voltage Swing	$R_L \geq 75\text{k}\Omega$	± 2.0	± 2.4					V
	$R_L \geq 5\text{k}\Omega$				± 2.0	± 2.1		V
Supply Current			25				180	μA
Power Consumption				150			1080	μW

TYPICAL PERFORMANCE CURVES FOR 776 AND 776C

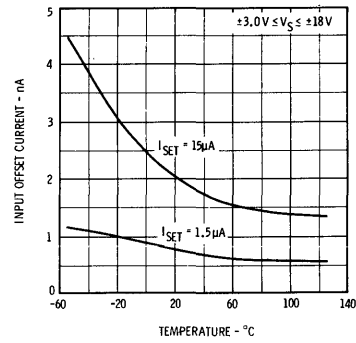
INPUT BIAS CURRENT AS A FUNCTION OF SET CURRENT



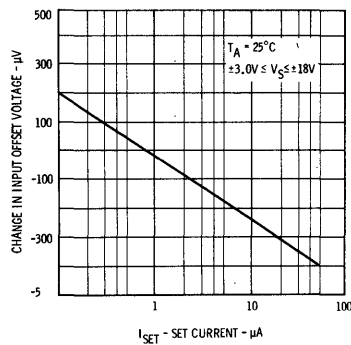
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



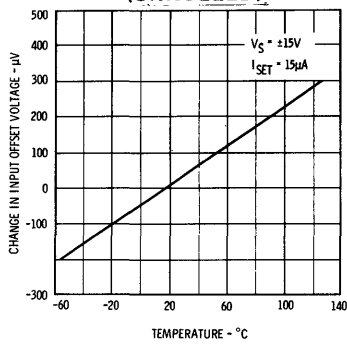
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



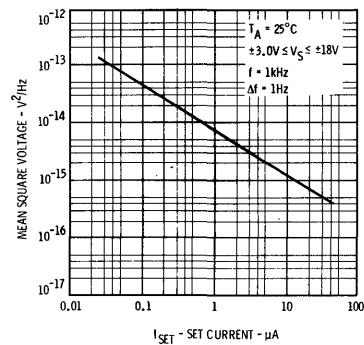
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF SET CURRENT



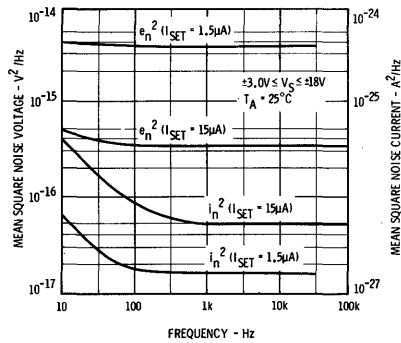
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE (UNNULLED)



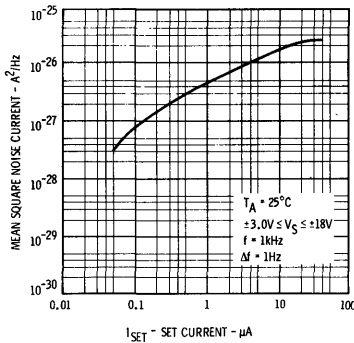
INPUT NOISE VOLTAGE AS A FUNCTION OF SET CURRENT



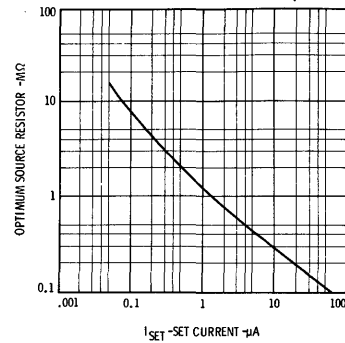
INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY



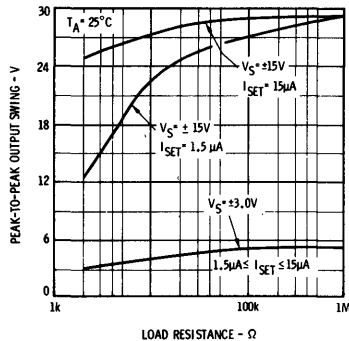
INPUT NOISE CURRENT AS A FUNCTION OF SET CURRENT



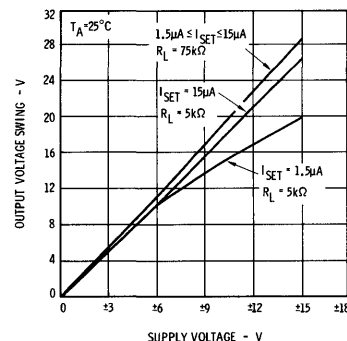
OPTIMUM SOURCE RESISTOR FOR MINIMUM NOISE AS A FUNCTION OF SET CURRENT



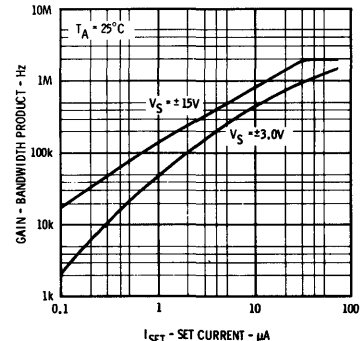
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

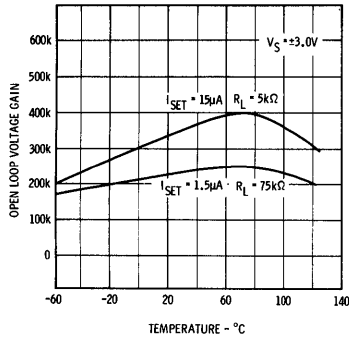


GAIN-BANDWIDTH PRODUCT AS A FUNCTION OF SET CURRENT

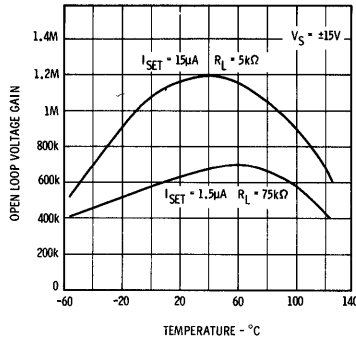


TYPICAL PERFORMANCE CURVES FOR 776 AND 776C

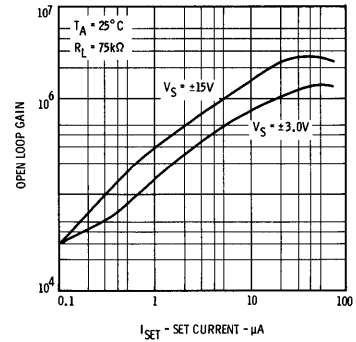
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



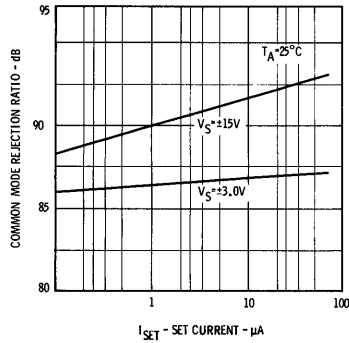
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



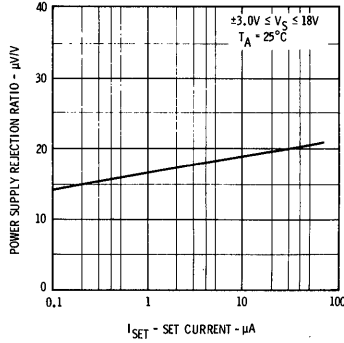
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SET CURRENT



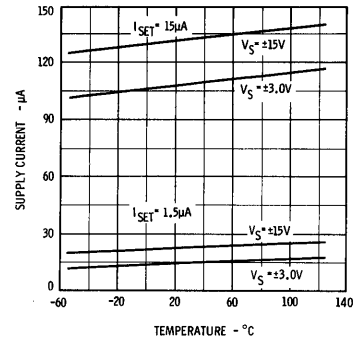
COMMON MODE REJECTION RATIO AS A FUNCTION OF SET CURRENT



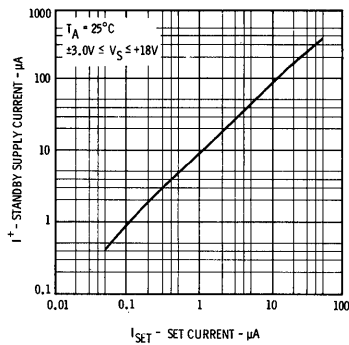
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF SET CURRENT



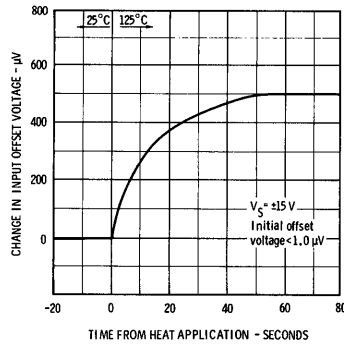
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



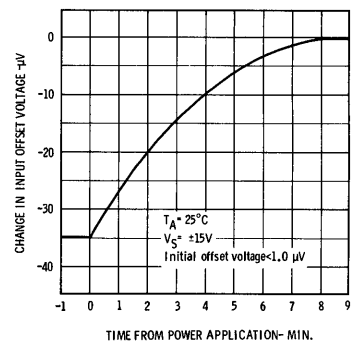
STANDBY SUPPLY CURRENT AS A FUNCTION OF SET CURRENT



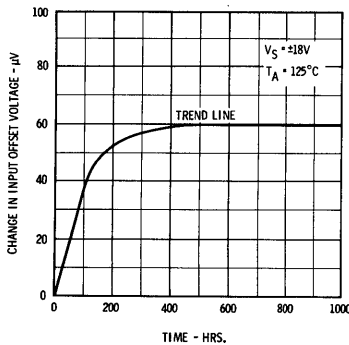
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



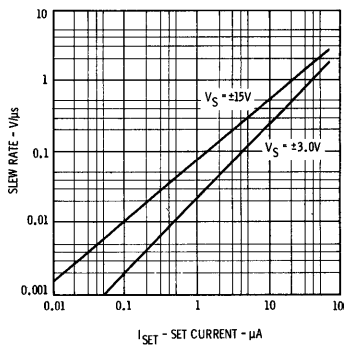
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER ON



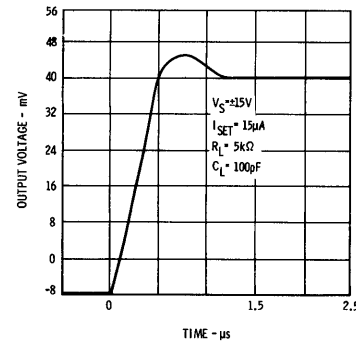
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



SLEW RATE AS A FUNCTION OF SET CURRENT

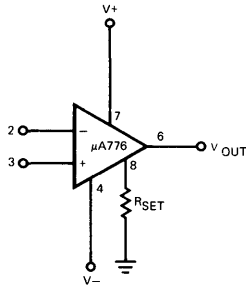


VOLTAGE FOLLOWER TRANSIENT RESPONSE (UNITY GAIN)

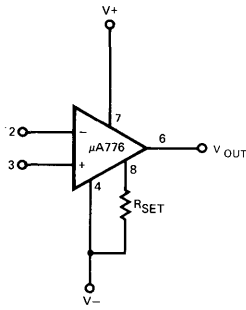


BIASING CIRCUITS

RESISTOR BIASING



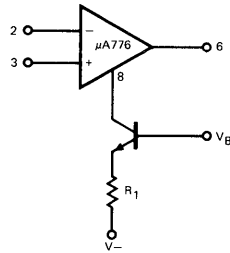
R_{SET} CONNECTED TO GROUND



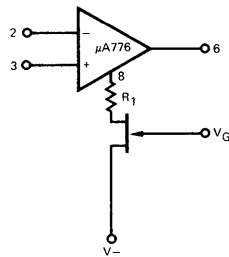
R_{SET} CONNECTED TO V^-

* Recommended for supply voltages less than $\pm 6V$.

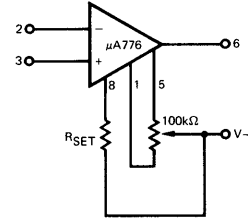
TRANSISTOR CURRENT SOURCE BIASING



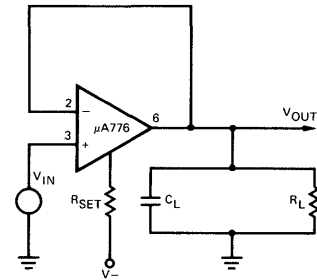
FET CURRENT SOURCE BIASING



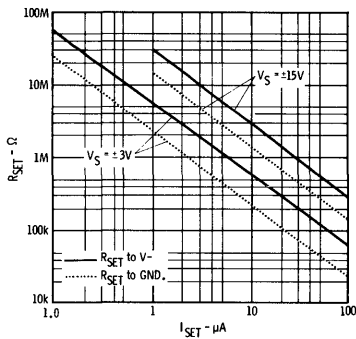
VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



SET CURRENT AS A FUNCTION OF SET RESISTOR



QUIESCENT CURRENT SETTING RESISTOR (I_{SET} TO V^-)

V_S	I_{SET}	
	$1.5\mu A$	$15\mu A$
$\pm 1.5 V$	$1.7M\Omega$	$170k\Omega$
$\pm 3.0 V$	$3.6M\Omega$	$360k\Omega$
$\pm 6.0 V$	$7.5M\Omega$	$750k\Omega$
$\pm 15 V$	$20M\Omega$	$2.0M\Omega$

Note: The $\mu A776$ may be operated with R_{SET} connected to ground or V^- .

I_{SET} EQUATIONS:

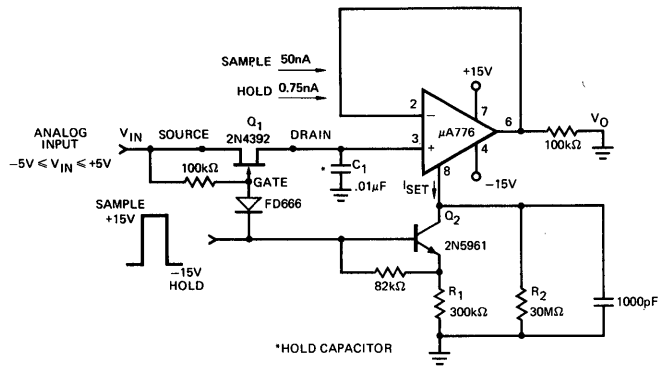
$$I_{SET} = \frac{V^+ - 0.7 - V^-}{R_{SET}}$$

where R_{SET} is connected to V^-

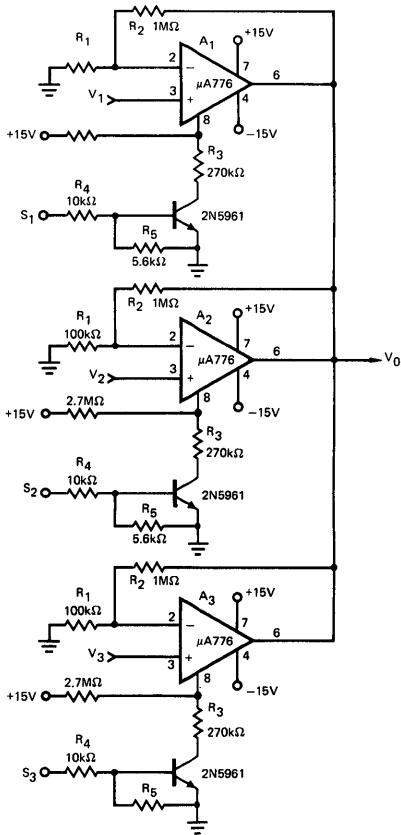
$$I_{SET} = \frac{V^+ - 0.7}{R_{SET}}$$

where R_{SET} is connected to ground.

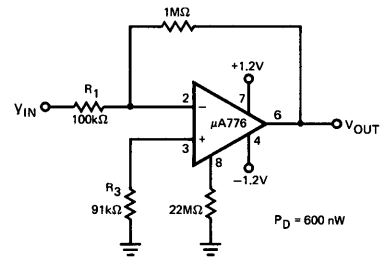
TYPICAL APPLICATIONS
HIGH ACCURACY SAMPLE AND HOLD



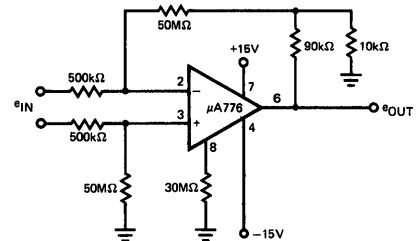
MULTIPLEXING AND SIGNAL CONDITIONING
WITHOUT FET'S



NANO-WATT AMPLIFIER



HIGH INPUT IMPEDANCE
AMPLIFIER



μA777

PRECISION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

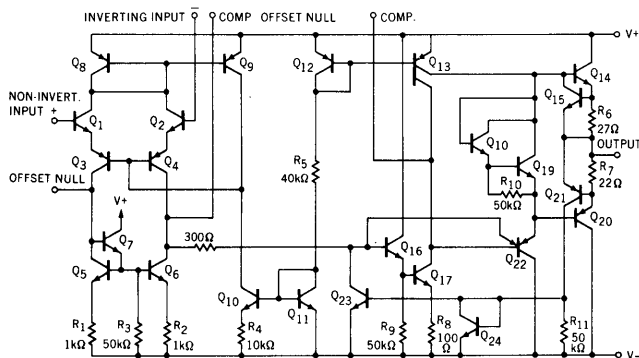
GENERAL DESCRIPTION — The μA777 is a monolithic Precision Operational Amplifier constructed using a low noise Fairchild Planar* epitaxial process. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifiers and low cost general purpose operational amplifiers. Low offset and bias currents improve system accuracy when used in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the μA777 maintains full ±30 V differential voltage range. The internal construction utilizes isothermal layout and special electrical design to maintain system performance despite variations in temperature or output load. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and easily used.

- **LOW OFFSET VOLTAGE AND OFFSET CURRENT**
- **LOW OFFSET VOLTAGE AND CURRENT DRIFT**
- **LOW INPUT BIAS CURRENT**
- **LOW INPUT NOISE VOLTAGE**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	-65° C to +150° C
Mini DIP	-55° C to +125° C
Operating Temperature Range	
Military (777)	-55° C to +125° C
Commercial (777C)	0° C to 70° C
Lead Temperature	
Metal Can, DIP and Flatpak (Soldering, 60 seconds)	300° C
Mini DIP (Soldering, 10 seconds)	260° C
Output Short-Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



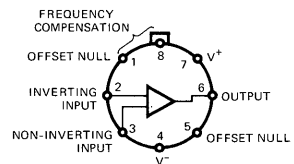
Notes on following pages.

CONNECTION DIAGRAMS

8-LEAD METAL CAN

(TOP VIEW)

PACKAGE OUTLINE 5B



NOTE: Pin 4 connected to case

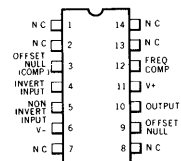
ORDER INFORMATION

TYPE	PART NO.
777	777 HM
777C	777 HC

14-LEAD DIP

(TOP VIEW)

PACKAGE OUTLINE 6A



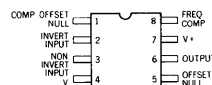
ORDER INFORMATION

TYPE	PART NO.
777	777DM
777C	777DC

8-LEAD MINI DIP

(TOP VIEW)

PACKAGE OUTLINE 9T



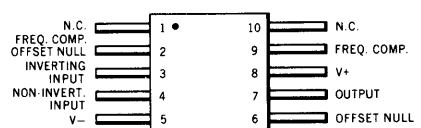
ORDER INFORMATION

TYPE	PART NO.
777C	777TC

10-LEAD FLATPAK ‡

(TOP VIEW)

PACKAGE OUTLINE 3F



‡ Available on special request

ORDER INFORMATION

TYPE	PART NO.
777	777FM

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A777

ELECTRICAL CHARACTERISTICS FOR 777 ($V_S = \pm 15$ V, $T_A = 25^\circ$ C, $C_C = 30$ pF unless otherwise specified)

PARAMETERS		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 50$ k Ω		0.5	2.0	mV
Input Offset Current				0.25	3.0	nA
Input Bias Current				8.0	25	nA
Input Resistance			2.0	10.0		M Ω
Input Capacitance				3.0		pF
Offset Voltage Adjustment Range				± 25		mV
Large Signal Voltage Gain		$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	50,000	250,000		V/V
Output Resistance				100		Ω
Output Short-Circuit Current				± 25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Risetime	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ k Ω , $C_L \leq 100$ pF		0.3		μ s
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2$ k Ω		0.5		V/ μ s
Transient Response (Voltage Follower, Gain of 10)	Risetime	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ k Ω , $C_L \leq 100$ pF		0.2		μ s
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2$ k Ω , $C_C = 3.5$ pF		5.5		V/ μ s
The following specifications apply for -55° C $\leq T_A \leq +125^\circ$ C:						
Input Offset Voltage		$R_S \leq 50$ k Ω		0.5	3.0	mV
Average Input Offset Voltage Drift		$R_S \leq 50$ k Ω		2.5	15	μ V/ $^\circ$ C
Input Offset Current					10	nA
Average Input Offset Current Drift		25° C $\leq T_A \leq +125^\circ$ C		2.5	30	pA/ $^\circ$ C
		-55° C $\leq T_A \leq 25^\circ$ C		6.5	150	pA/ $^\circ$ C
Input Bias Current					75	nA
Input Voltage Range			± 12	± 13		V
Common Mode Rejection Ratio		$R_S \leq 50$ k Ω	80	95		dB
Supply Voltage Rejection Ratio		$R_S \leq 50$ k Ω		13	100	μ V/V
Large Signal Voltage Gain		$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	25,000			V/V
Output Voltage Swing		$R_L \geq 10$ k Ω	± 12	± 14		V
		$R_L \geq 2$ k Ω	± 10	± 13		V
Supply Current		$T_A = +125^\circ$ C		1.5	2.5	mA
		$T_A = -55^\circ$ C		2.0	3.3	mA
Power Consumption		$T_A = +125^\circ$ C		40	75	mW
		$T_A = -55^\circ$ C		60	100	mW

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A777

ELECTRICAL CHARACTERISTICS FOR 777C ($V_S = \pm 15$ V, $T_A = 25^\circ$ C, $C_C = 30$ pF unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50$ k Ω		0.7	5.0	mV
Input Offset Current			0.7	20.0	nA
Input Bias Current			25	100	nA
Input Resistance		1.0	2.0		M Ω
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			± 25		mV
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	25,000	250,000		V/V
Output Resistance			100		Ω
Output Short-Circuit Current			± 25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1)	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ k Ω , $C_L \leq 100$ pF	Risetime		0.3	μ s
		Overshoot		5.0	%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ k Ω		0.5		V/ μ s
Transient Response (Voltage Follower, Gain of 10)	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ k Ω , $C_L \leq 100$ pF	Risetime		0.2	μ s
		Overshoot		5.0	%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ k Ω		5.5		V/ μ s
The following specifications apply for 0° C $\leq T_A \leq +70^\circ$ C					
Input Offset Voltage	$R_S \leq 50$ k Ω		0.8	5.0	mV
Average Input Offset Voltage Drift	$R_S \leq 50$ k Ω		4.0	30	μ V/ $^\circ$ C
Input Offset Current				40	nA
Average Input Offset Current Drift	25° C $\leq T_A \leq +70^\circ$ C		0.01	0.3	nA/ $^\circ$ C
	0° C $\leq T_A \leq +25^\circ$ C		0.02	0.6	nA/ $^\circ$ C
Input Bias Current				200	nA
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 50$ k Ω	70	95		dB
Supply Voltage Rejection Ratio	$R_S \leq 50$ k Ω		15	150	μ V/V
Large Signal Voltage Gain	$R_L \geq 2$ k Ω , $V_{OUT} = \pm 10$ V	15,000			V/V
Output Voltage Swing	$R_L \geq 10$ k Ω	± 12	± 14		V
	$R_L \geq 2$ k Ω	± 10	± 13		V
Power Consumption			60	100	mW

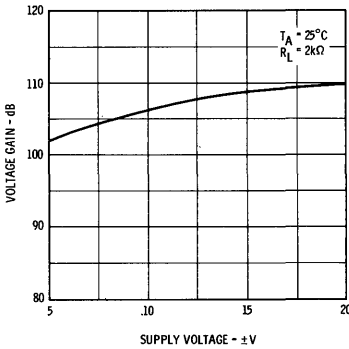
NOTES

1. Rating applies to ambient temperatures up to 70° C. Above 70° C ambient derate linearly at 6.3 mW/ $^\circ$ C for Metal Can, 8.3 mW/ $^\circ$ C for the DIP 5.6 mW/ $^\circ$ C for the Mini DIP and 7.1 mW/ $^\circ$ C for the Flatpak.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to $+125^\circ$ C case temperature or $+75^\circ$ C ambient temperature.

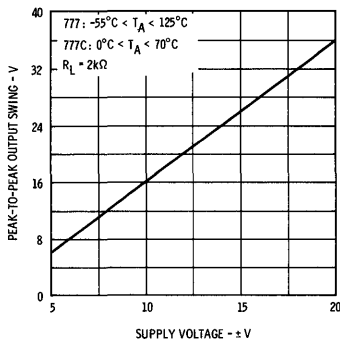
FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A777$

TYPICAL PERFORMANCE CURVES FOR 777 AND 777C

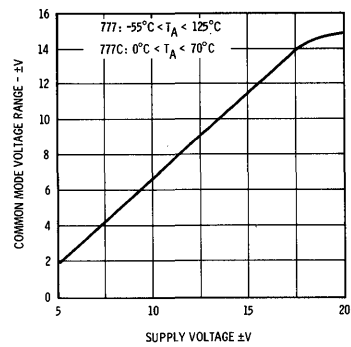
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



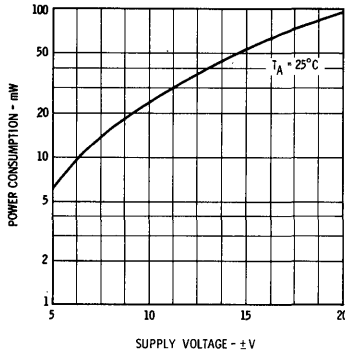
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



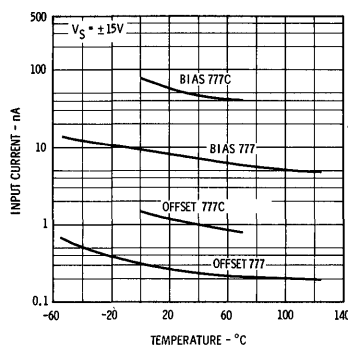
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



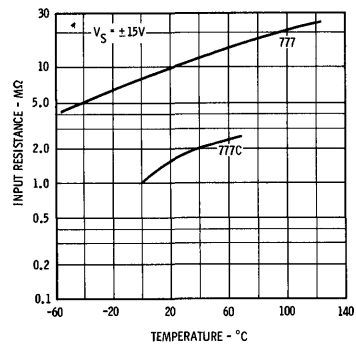
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



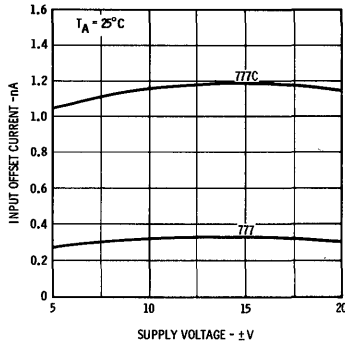
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



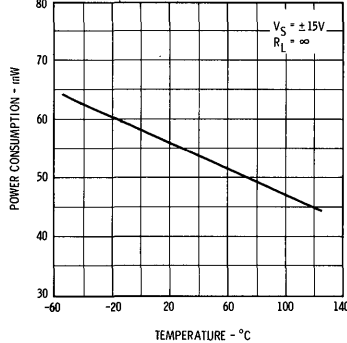
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



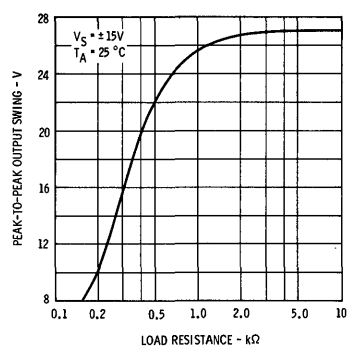
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



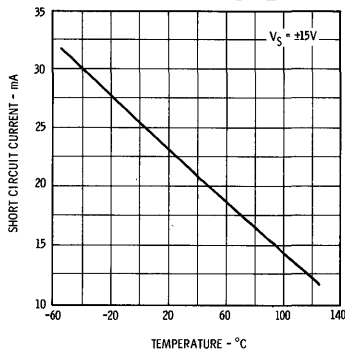
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



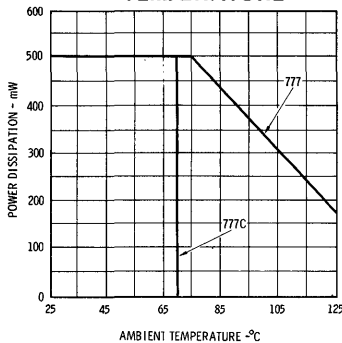
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



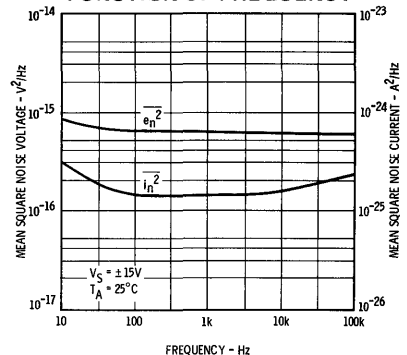
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

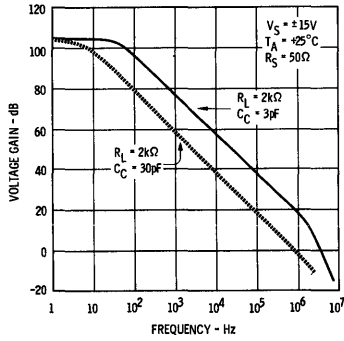


INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY

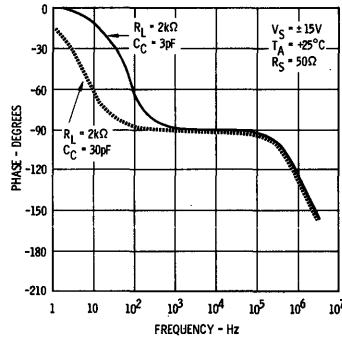


TYPICAL PERFORMANCE CURVES FOR 777 AND 777C

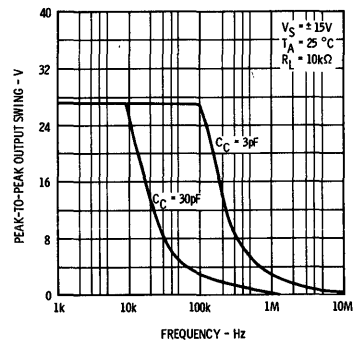
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



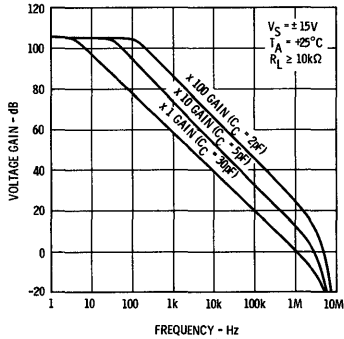
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



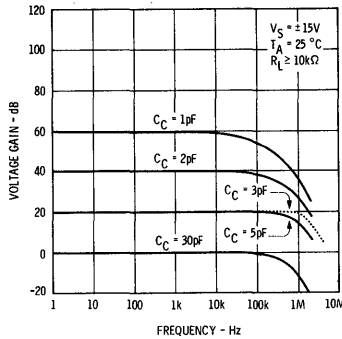
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



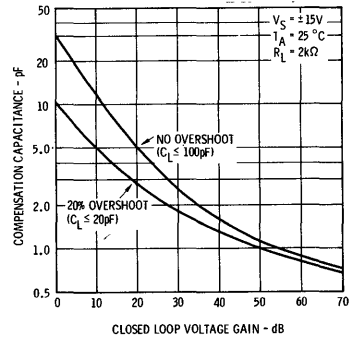
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



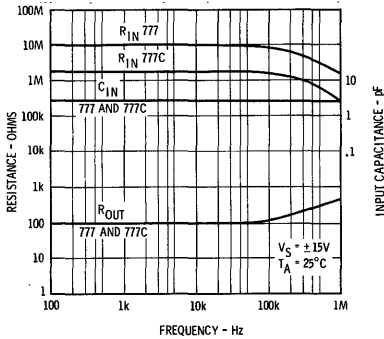
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



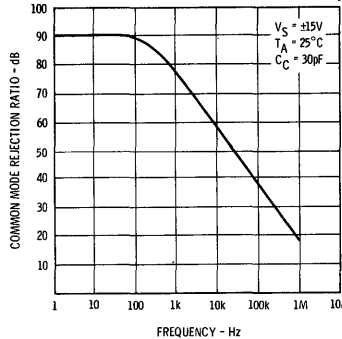
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



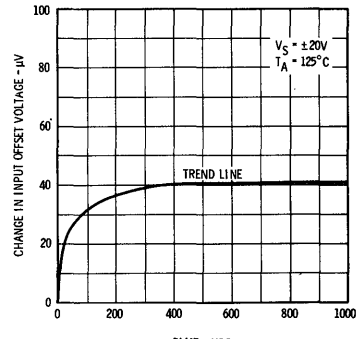
INPUT RESISTANCE, OUTPUT RESISTANCE, AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



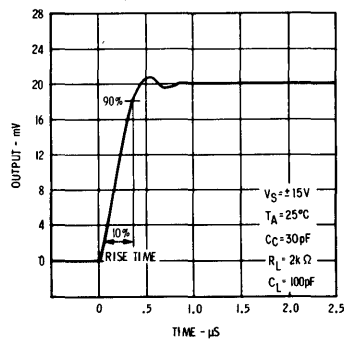
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



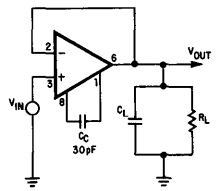
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



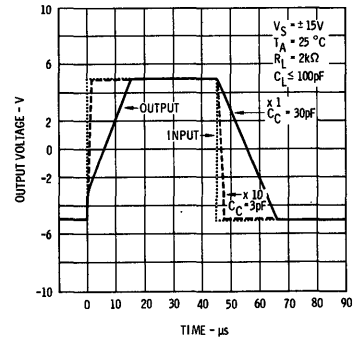
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

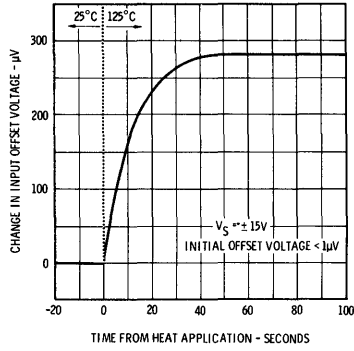


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

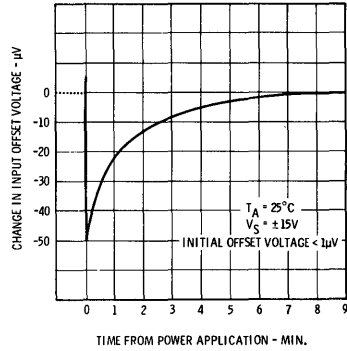


TYPICAL PERFORMANCE CURVES FOR 777 AND 777C

THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE

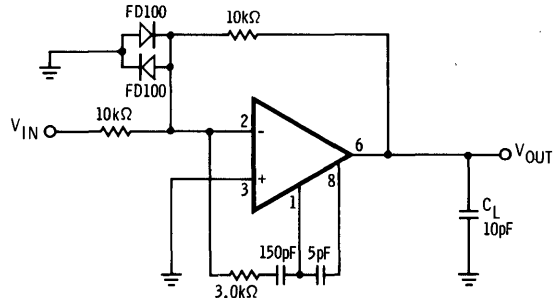
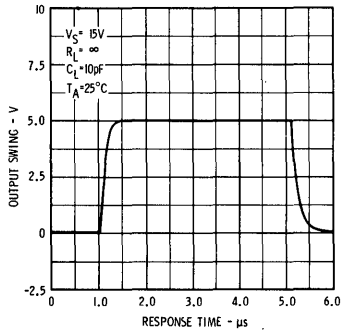


STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON

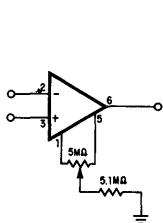


FEED-FORWARD COMPENSATION

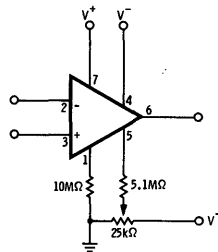
LARGE SIGNAL FEEDFORWARD TRANSIENT RESPONSE



VOLTAGE OFFSET NULL CIRCUIT

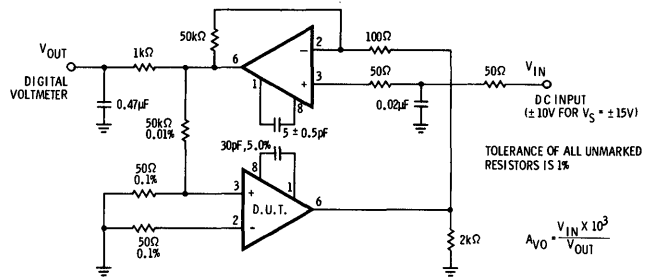


SUGGESTED



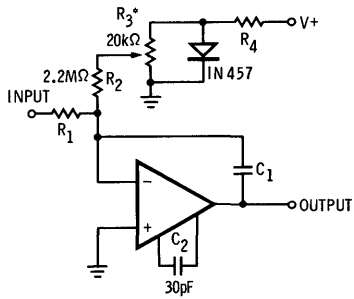
ALTERNATE

GAIN TEST CIRCUIT



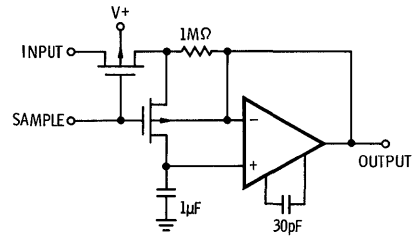
TYPICAL APPLICATIONS

BIAS COMPENSATED LONG TIME INTEGRATOR

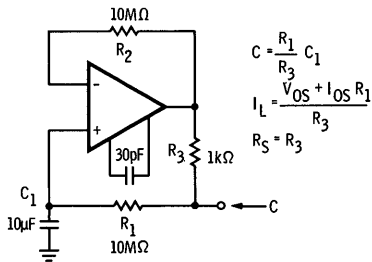


* Adjust R_3 for minimum integrator drift

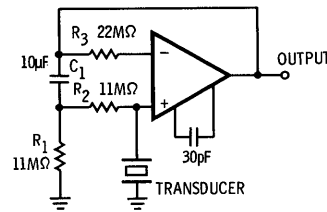
SAMPLE AND HOLD



CAPACITANCE MULTIPLIER

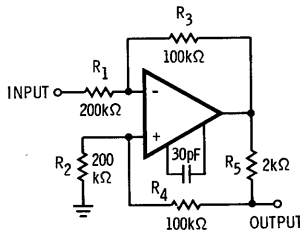


AMPLIFIER FOR CAPACITANCE TRANSDUCERS



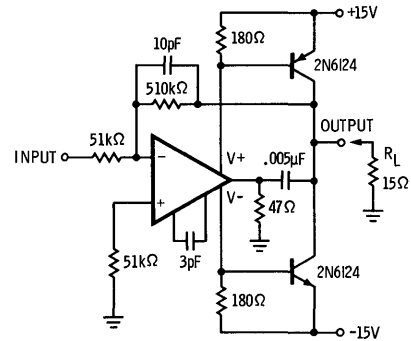
Low Frequency Cutoff $R_1 \times C_1$

BILATERAL CURRENT SOURCE

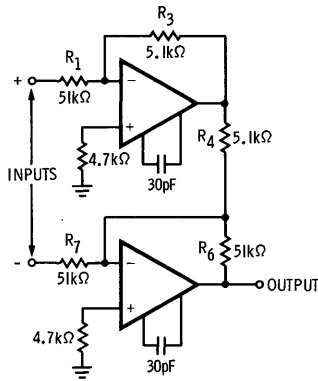


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}; R_1 = R_2; R_3 = R_4 + R_5$$

HIGH SLEW RATE POWER AMPLIFIER



± 100 V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER



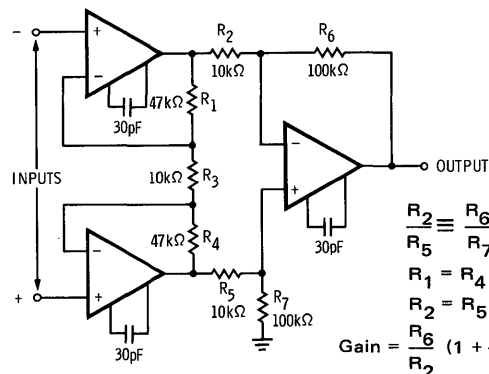
$$\frac{R_1}{R_7} \equiv \frac{R_3}{R_4} \text{ for best CMRR}$$

$$R_3 = R_4$$

$$R_1 = R_6 = 10R_3$$

$$\text{Gain} = \frac{R_7}{R_6}$$

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$$\frac{R_2}{R_5} \equiv \frac{R_6}{R_7} \text{ for best CMRR}$$

$$R_1 = R_4$$

$$R_2 = R_5$$

$$\text{Gain} = \frac{R_6}{R_2} \left(1 + \frac{2R_1}{R_3} \right)$$

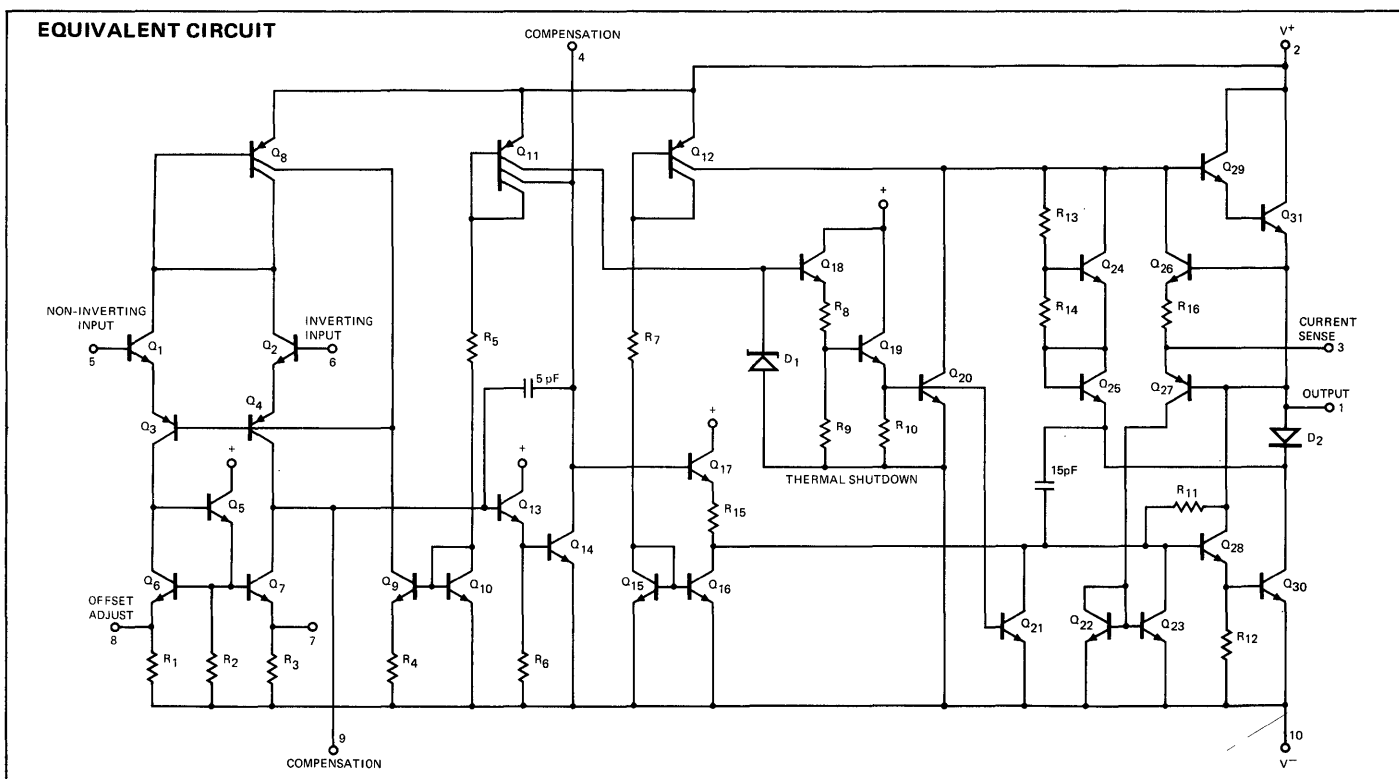
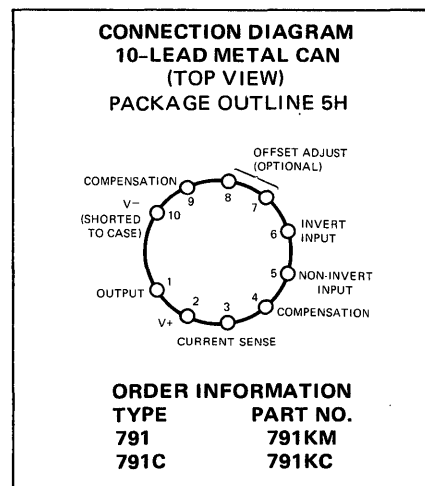
μA791

POWER OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA791 is a high performance Monolithic Operational Amplifier constructed using the Fairchild Planar* Epitaxial process with input characteristics similar to the μA741 operational amplifier and 1 amp available output current. It is intended for use in a wide variety of applications including audio amplifiers, servo amplifiers, and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required. The μA791 is thermal and short circuit protected.

- **CURRENT OUTPUT TO 1 AMP**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **NO LATCH-UP**
- **LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES**
- **THERMAL OVERLOAD PROTECTION**



*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A791

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 3)	
Military (791)	±22 V
Commercial (791C)	±18 V
Peak Output Current (Note 3)	1.25 A
Continuous Internal Power Dissipation (Total Package) (Note 1)	15 W
Continuous Internal Power Dissipation (Per Output Transistor) (Note 1)	10 W
Peak Internal Power Dissipation (Per Output Transistor for $t \leq 5$ seconds)	15 W
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltages between offset Null and V_{-}	±0.5 V
Operating Temperature Range	
Military (791)	-55°C to +125°C
Commercial (791C)	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds max.)	+280°C

NOTES

1. Rating applies for 25°C case temperature, maximum power dissipation and safe area limitations must be observed for case temperatures above 25°C.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Under short circuit conditions, the safe operating area and dc power dissipation limitations must be observed.

±15 VOLT OPERATION FOR 791

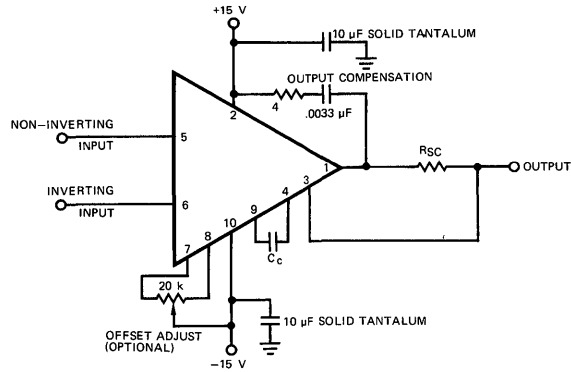
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		M Ω
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	$\mu\text{V/V}$
Large Signal Voltage Gain	$R_L = 1 \text{ k}\Omega$	50,000			V/V
	$R_L = 11\Omega$	50,000			V/V
Output Voltage Swing	$R_{SC} = 0, R_L = 1 \text{ k}\Omega$	±12	±14		V
	$R_{SC} = 0, R_L = 11\Omega$	±12	±12.2		V
Output Short Circuit Current	$R_{SC} = 0.7\Omega$		1000		mA
	$R_{SC} = 1.5\Omega$		500		mA
Supply Current (Zero Signal)				25	mA

The following specifications apply for $-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$

Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$			6	mV
Input Offset Current				500	nA
Input Bias Current				1.5	μA
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	$\mu\text{V/V}$
Large Signal Voltage Gain	$R_L = 1 \text{ k}\Omega$	25,000			V/V
	$R_L = 11\Omega$	25,000			V/V
Output Voltage Swing	$R_{SC} = 0, R_L = 1 \text{ k}\Omega$	±11.5			V
	$R_{SC} = 0, R_L = 11\Omega$	±11.5			V
Supply Current (Zero Signal)				30	mA

FREQUENCY COMPENSATION



GAIN	C_C
1	100 pF
10	5 pF
100	Not. Req.

R_{SC}	I_{SC}
0.6Ω	1.0 A
1.5Ω	500 mA
3.0Ω	250 mA

NOTE

1. Power supply decoupling capacitors and compensation networks must have short leads and must be located at the amplifier pins.

±15 VOLT OPERATION FOR 791C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ C$ unless otherwise specified)

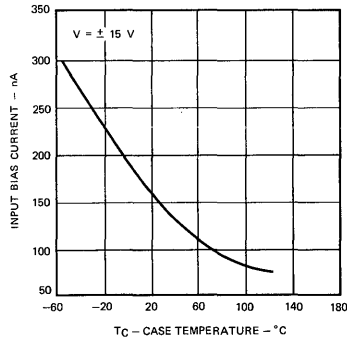
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	1.0		MΩ
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	$\mu V/V$
Large Signal Voltage Gain	$R_L = 1 \text{ k}\Omega$	20k			V/V
	$R_L = 11\Omega$	20k			V/V
Output Voltage Swing	$R_{SC} = 0, R_L = 1 \text{ k}\Omega$	±11.5	±14		V
	$R_{SC} = 0, R_L = 11\Omega$	±11.5	±12.2		V
Output Short Circuit Current	$R_{SC} = 0.7\Omega$		1000		mA
	$R_{SC} = 1.5\Omega$		500		mA
Supply Current (Zero Signal)				25	mA

The following specifications apply for $0^\circ C < T_C < 70^\circ C$

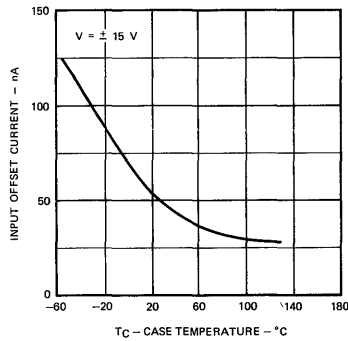
Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	$\mu V/V$
Large Signal Voltage Gain	$R_L = 1 \text{ k}\Omega$	15k			V/V
	$R_L = 11\Omega$	15k			V/V
Output Voltage Swing	$R_{SC} = 0, R_L = 1 \text{ k}\Omega$	±11.0			V
	$R_{SC} = 0, R_L = 11\Omega$	±11.0			V
Supply Current (Zero signal)				30	mA

TYPICAL PERFORMANCE CURVES FOR 791 AND 791C

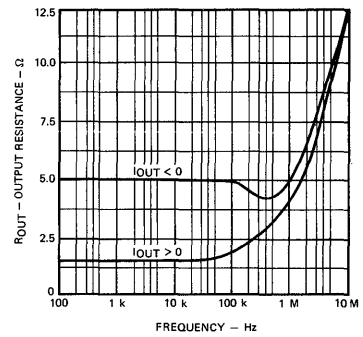
TYPICAL INPUT BIAS CURRENT AS A FUNCTION OF CASE TEMPERATURE



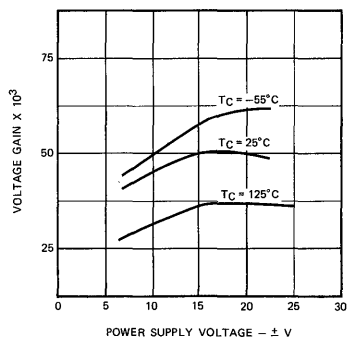
TYPICAL INPUT OFFSET CURRENT AS A FUNCTION OF CASE TEMPERATURE



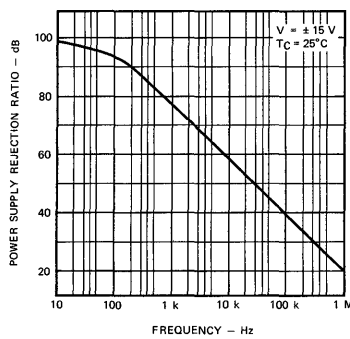
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY (OPEN LOOP)



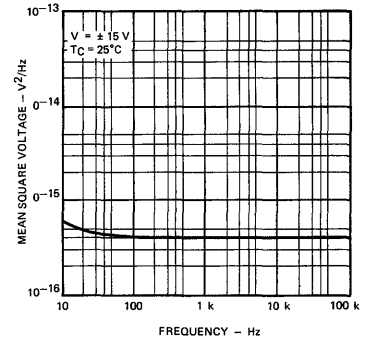
TYPICAL PERFORMANCE CURVE VOLTAGE GAIN AS A FUNCTION OF POWER SUPPLY VOLTAGE



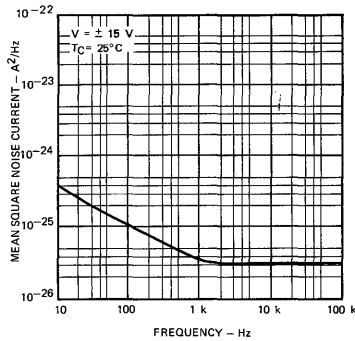
TYPICAL POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREQUENCY (791)



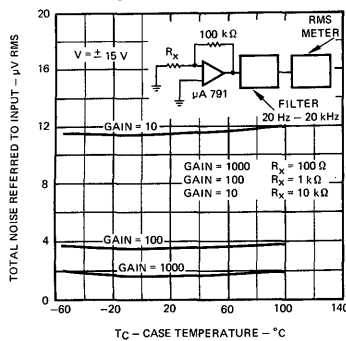
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



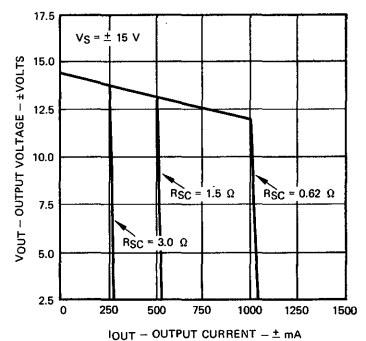
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



TOTAL NOISE (20 Hz-20 kHz) AS A FUNCTION OF CASE TEMPERATURE

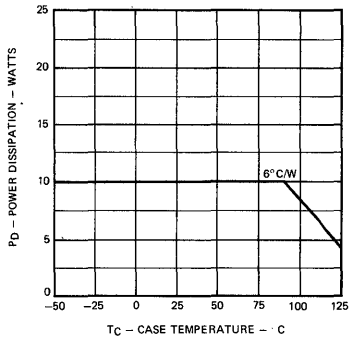


OUTPUT VOLTAGE SWING AS A FUNCTION OF OUTPUT CURRENT

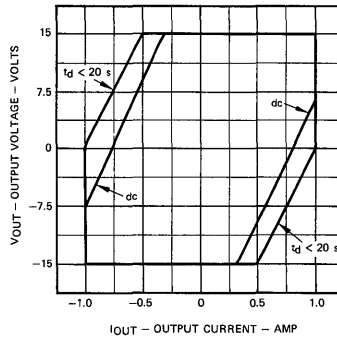


TYPICAL PERFORMANCE CURVES FOR 791 AND 791C (Cont'd)

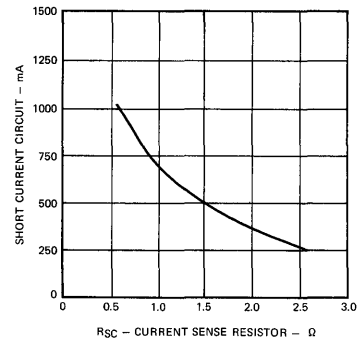
MAXIMUM POWER DISSIPATION PER OUTPUT TRANSISTOR AS A FUNCTION OF CASE TEMPERATURE



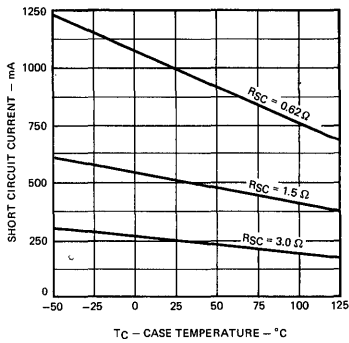
OUTPUT SAFE OPERATING AREA PER OUTPUT TRANSISTOR



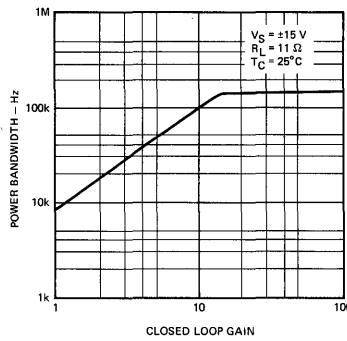
SHORT CIRCUIT CURRENT AS A FUNCTION OF CURRENT SENSE RESISTOR, Rsc



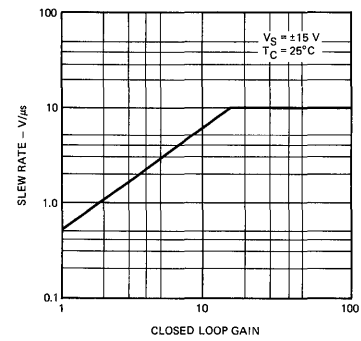
SHORT CIRCUIT CURRENT AS A FUNCTION OF CASE TEMPERATURE



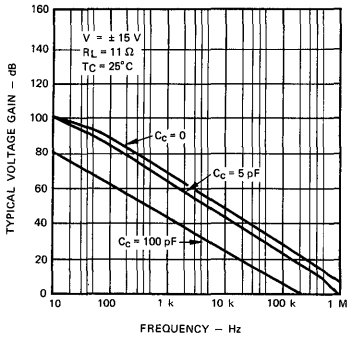
POWER BANDWIDTH AS A FUNCTION OF CLOSED LOOP GAIN



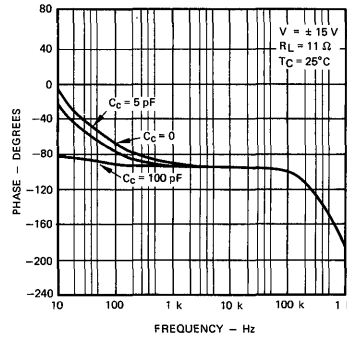
SLEW RATE AS A FUNCTION OF CLOSED LOOP GAIN



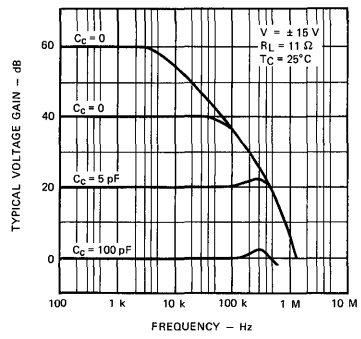
VOLTAGE GAIN AS A FUNCTION OF OPEN LOOP FREQUENCY RESPONSE



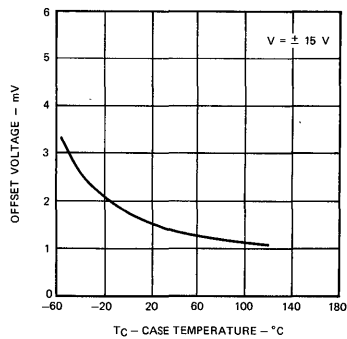
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



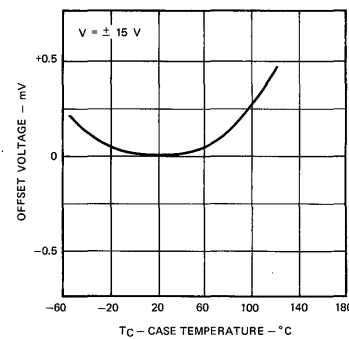
FREQUENCY RESPONSE FOR CLOSED LOOP GAINS



TYPICAL OFFSET VOLTAGE UN-NULLED AS A FUNCTION OF CASE TEMPERATURE

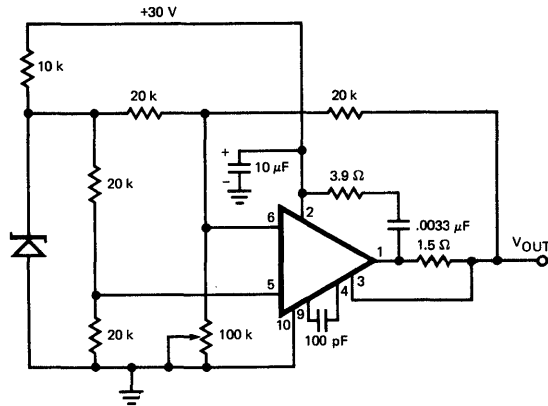


TYPICAL OFFSET VOLTAGE NULLED AS A FUNCTION OF CASE TEMPERATURE



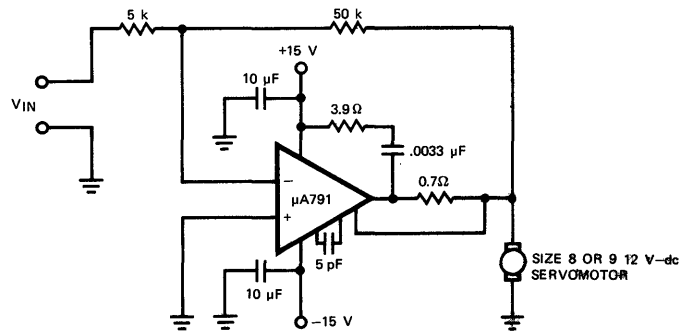
TYPICAL APPLICATIONS

POSITIVE VOLTAGE REGULATOR

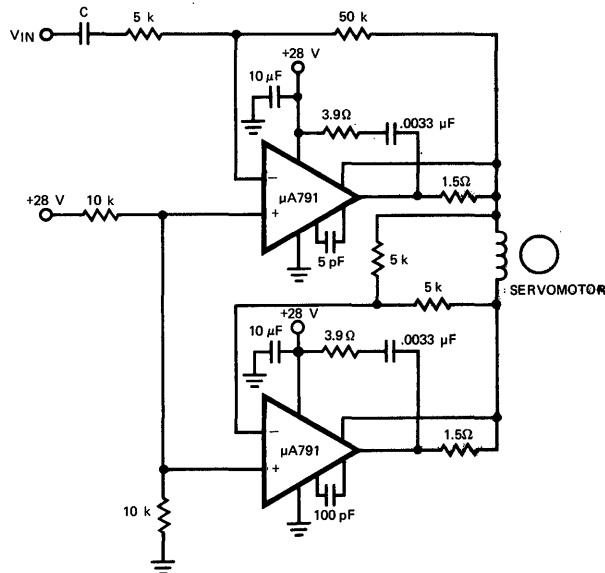


NOTES:
0 to 27 V regulator
500 mA output current

DC SERVO AMPLIFIER



AC SERVO AMPLIFIER
BRIDGE TYPE



101 • 201

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

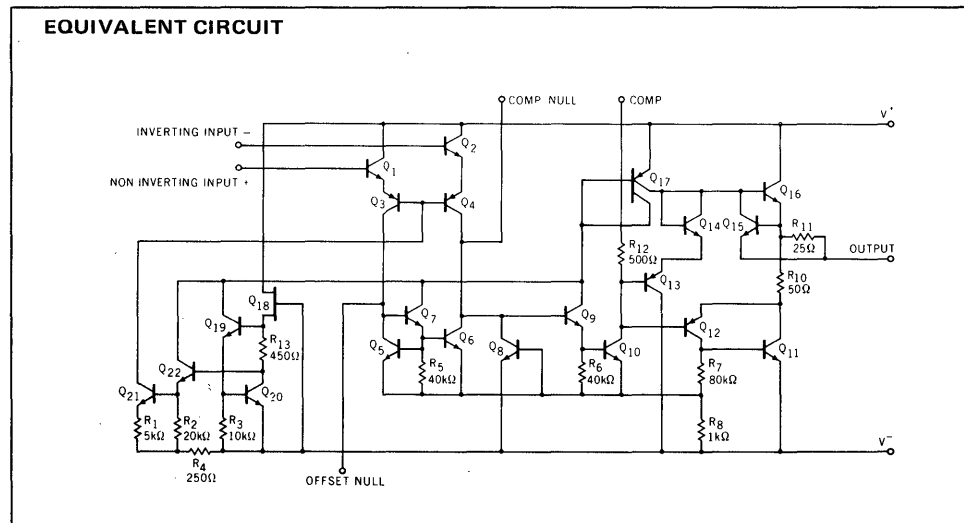
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 101 and 201 are General Purpose monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. The 101 and 201 compensate easily with a single external component. High common mode voltage range and absence of "latch-up" make the 101 and 201 ideal for use as voltage followers. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The 101 and 201 are short-circuit protected and have the same pin configuration as the popular μ A741, μ A748 and μ A709.

- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

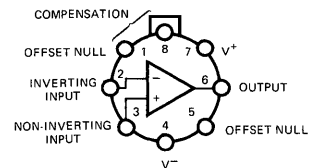
Supply Voltage	$\pm 22V$
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	$\pm 30V$
Input Voltage (Note 2)	$\pm 15V$
Storage Temperature Range	
Metal Can, DIP	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	
Military (101)	$-55^{\circ}C$ to $+125^{\circ}C$
Commercial (201)	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 60 seconds)	$300^{\circ}C$



Notes on following pages

CONNECTION DIAGRAMS

8-LEAD METAL CAN (TOP VIEW) PACKAGE OUTLINE 5B

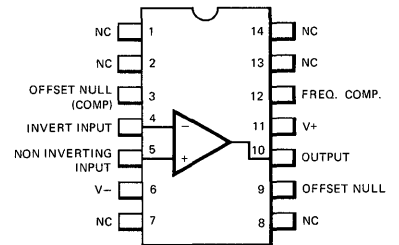


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
101	LM101H
201	LM201H

14-LEAD DIP (TOP VIEW) PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
101	LM101D
201	LM201D

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 101 • 201

ELECTRICAL CHARACTERISTICS FOR 101 ($\pm 5.0V \leq V_S \leq \pm 20V$, $T_A = 25^\circ C$, $C_1 = 30pF$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0	mV
Input Offset Current			40	200	nA
Input Bias Current			120	500	nA
Input Resistance		300	800		k Ω
Supply Current	$V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	50	160		V/mV
The following specifications apply for $-55^\circ C \leq T_A \leq +125^\circ C$:					
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$		3.0		$\mu V/^\circ C$
	$R_S \leq 10k\Omega$		6.0		$\mu V/^\circ C$
Input Offset Current	$T_A = +125^\circ C$		10	200	nA
	$T_A = -55^\circ C$		100	500	nA
Average Temperature Coefficient of Input Offset Current	$+25^\circ C \leq T_A \leq +125^\circ C$		0.01	0.1	nA/ $^\circ C$
	$-55^\circ C \leq T_A \leq +25^\circ C$		0.02	0.2	nA/ $^\circ C$
Input Bias Current	$T_A = -55^\circ C$		0.28	1.5	μA
Supply Current	$T_A = +125^\circ C, V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$	$R_L = 10k\Omega$	± 12	± 14	V
		$R_L = 2k\Omega$	± 10	± 13	V
Input Voltage Range	$V_S = \pm 15V$	± 12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB

NOTES

1. Rating applies to ambient temperature up to $70^\circ C$. Above $70^\circ C$ ambient derate linearly at $6.3mW/^\circ C$ for the Metal Can and $8.3mW/^\circ C$ for the DIP.
2. For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. The 101 ratings apply to $+125^\circ C$ case temperature or $+75^\circ C$ ambient temperature. The 201 ratings apply to case temperatures up to $+70^\circ C$.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 101 • 201

ELECTRICAL CHARACTERISTICS FOR 201 ($\pm 5.0V \leq V_S \leq \pm 15V$, $T_A = 25^\circ C$, $C_1 = 30pF$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.25	1.5	μA
Input Resistance		100	400		$k\Omega$
Supply Current	$V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	20	150		V/mV
The following specifications apply for $0^\circ C \leq T_A \leq 70^\circ C$:					
Input Offset Voltage	$R_S \leq 10k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$		6.0		$\mu V/^\circ C$
	$R_S \leq 10k\Omega$		10.0		$\mu V/^\circ C$
Input Offset Current	$T_A = 70^\circ C$		50	400	nA
	$T_A = 0^\circ C$		150	750	nA
Average Temperature Coefficient of Input Offset Current	$25^\circ C \leq T_A \leq 70^\circ C$		0.01	0.3	$nA/^\circ C$
	$0^\circ C \leq T_A \leq 25^\circ C$		0.02	0.6	$nA/^\circ C$
Input Bias Current	$T_A = 0^\circ C$		0.32	2.0	μA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$	$R_L = 10k\Omega$	± 12	± 14	V
		$R_L = 2k\Omega$	± 10	± 13	V
Input Voltage Range	$V_S = \pm 15V$	± 12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB

101A • 201A • 301A

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

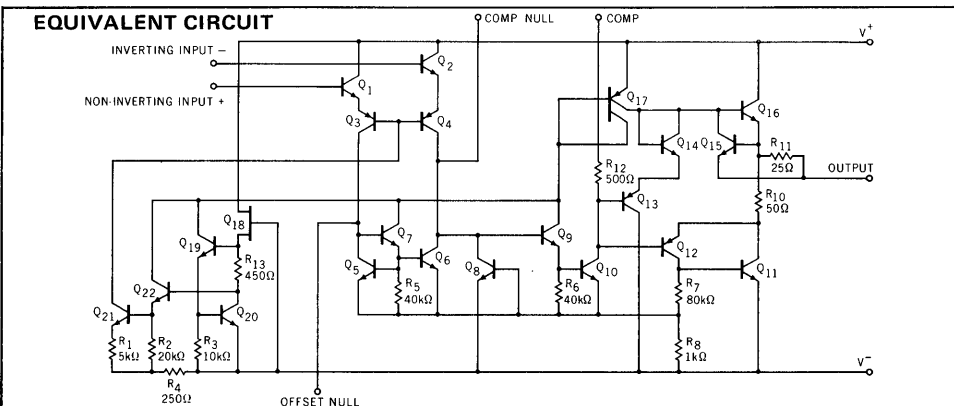
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 101A, 201A and 301A are General Purpose monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. These integrated circuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents of the 101A, 201A, or 301A. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of "latch-up" coupled with internal short circuit protection make the 101A, 201A and 301A virtually foolproof. The 101A, 201A and 301A are pin compatible with the popular μ A709, μ A741, μ A748 and μ A777.

- **LOW OFFSET CURRENT AND VOLTAGE**
- **LOW OFFSET CURRENT DRIFT**
- **LOW BIAS CURRENT**
- **SHORT CIRCUIT PROTECTED**
- **LOW POWER CONSUMPTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		
Military and Instrument (101A and 201A)		±22V
Commercial (301A)		±18V
Internal Power Dissipation (Note 1)		
Metal Can		500 mW
DIP		670 mW
Flatpak		570 mW
Mini DIP		310 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Storage Temperature Range		
Metal Can, DIP, and Flatpak		–65°C to +150°C
Mini DIP		–55°C to +125°C
Operating Temperature Range		
Military (101A)		–55°C to +125°C
Instrument (201A)		–25°C to +85°C
Commercial (301A)		0°C to +70°C
Lead Temperature (Soldering)		
Metal Can, DIP and Flatpak (60 seconds)		300°C
Mini DIP (10 seconds)		260°C
Output Short Circuit Duration (Note 3)		Indefinite



Notes on page 3

CONNECTION DIAGRAMS

8-LEAD METAL CAN (TOP VIEW)

PACKAGE OUTLINE 5B

NOTE: PIN CONNECTED TO CASE

ORDER INFORMATION	
TYPE	PART NO.
101A	LM101AH
201A	LM201AH
301A	LM301AH

14-LEAD DIP (TOP VIEW)

PACKAGE OUTLINE 6A

ORDER INFORMATION	
TYPE	PART NO.
101A	LM101AD
201A	LM201AD
301A	LM301AD

10-LEAD FLATPACK (TOP VIEW)

PACKAGE OUTLINE 3F

Available on special request

ORDER INFORMATION	
TYPE	PART NO.
101A	LM101AF
201A	LM201AF

8-LEAD MINIDIP (TOP VIEW)

PACKAGE OUTLINE 9T

ORDER INFORMATION	
TYPE	PART NO.
301A	LM301AN

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 101A • 201A • 301A

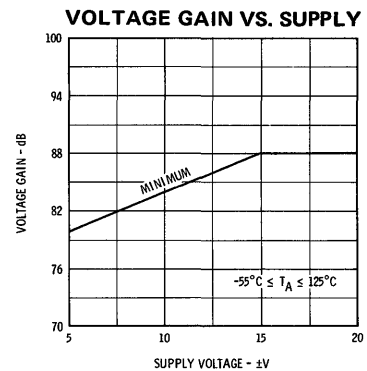
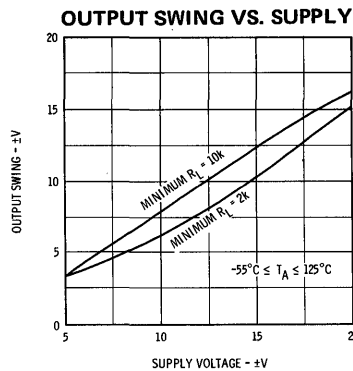
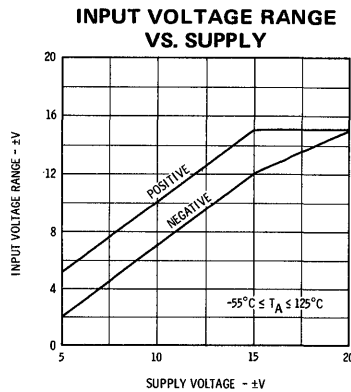
ELECTRICAL CHARACTERISTICS FOR 101A and 201A ($\pm 5.0V \leq V_S \leq \pm 20V$, $T_A = 25^\circ C$, $C_1 = 30pF$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		0.7	2.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			30	75	nA
Input Resistance		1.5	4.0		$M\Omega$
Supply Current	$V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	50	160		V/mV

The following specifications apply for $-55^\circ C \leq T_A \leq +125^\circ C$: (Note 4)

Input Offset Voltage	$R_S \leq 10k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	$\mu V/^\circ C$
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$+25^\circ C \leq T_A \leq +125^\circ C$		0.01	0.1	nA/ $^\circ C$
	$-55^\circ C \leq T_A \leq +25^\circ C$		0.02	0.2	nA/ $^\circ C$
Input Bias Current				100	nA
Supply Current	$T_A = +125^\circ C, V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$		± 12	± 14	V
			± 10	± 13	V
Input Voltage Range	$V_S = \pm 20V$		± 15		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	80	96		dB

GUARANTEED PERFORMANCE CURVES FOR 101A AND 201A



FAIRCHILD LINEAR INTEGRATED CIRCUITS • 101A • 201A • 301A

ELECTRICAL CHARACTERISTICS FOR 301A ($\pm 5.0V \leq V_S \leq \pm 15V$, $T_A = 25^\circ C$, $C_1 = 30pF$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	7.5	mV
Input Offset Current			3	50	nA
Input Bias Current			70	250	nA
Input Resistance		0.5	2		M Ω
Supply Current	$V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	25	160		V/mV

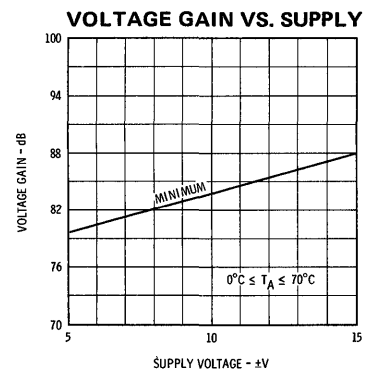
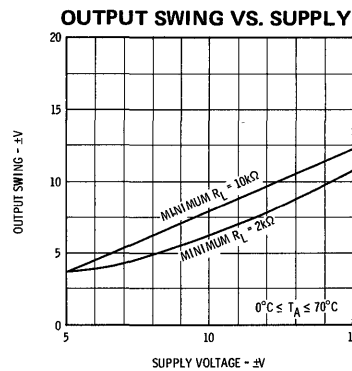
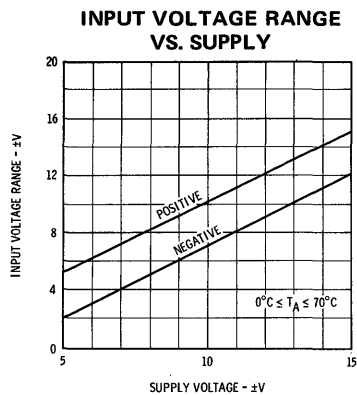
The following specifications apply for $0^\circ C \leq T_A \leq 70^\circ C$:

Input Offset Voltage	$R_S \leq 10k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	$\mu V/^\circ C$
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	$25^\circ C \leq T_A \leq 70^\circ C$		0.01	0.3	nA/ $^\circ C$
	$0^\circ C \leq T_A \leq 25^\circ C$		0.02	0.6	nA/ $^\circ C$
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	± 12	± 14		V
	$R_L = 2k\Omega$	± 10	± 13		V
Input Voltage Range	$V_S = \pm 15V$	± 12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB

NOTES:

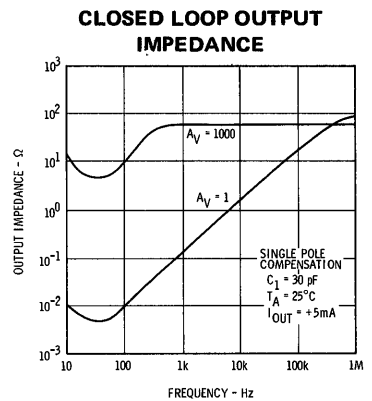
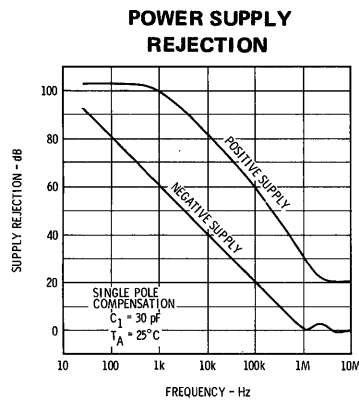
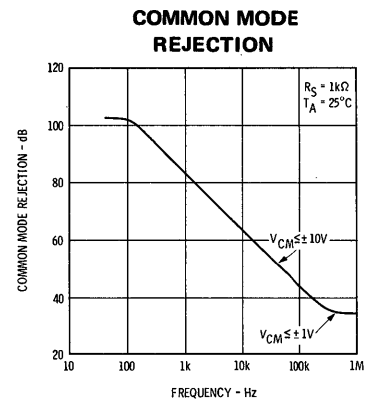
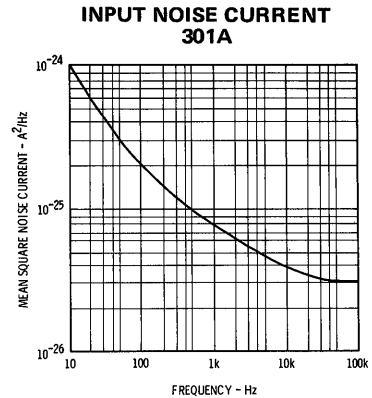
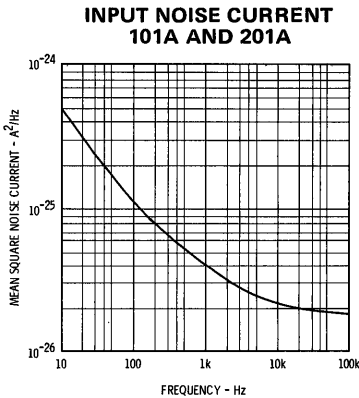
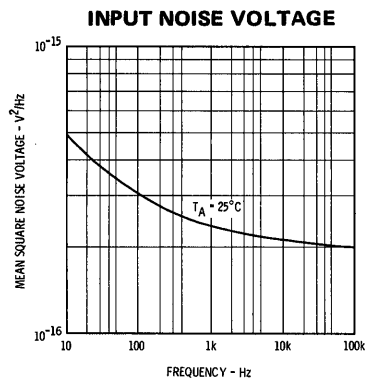
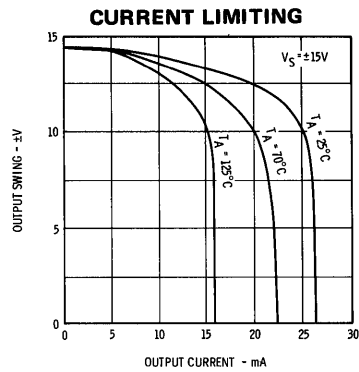
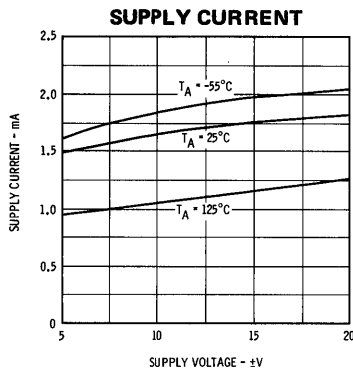
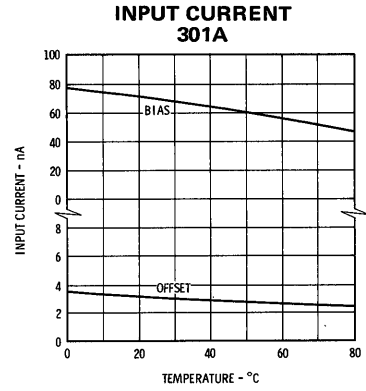
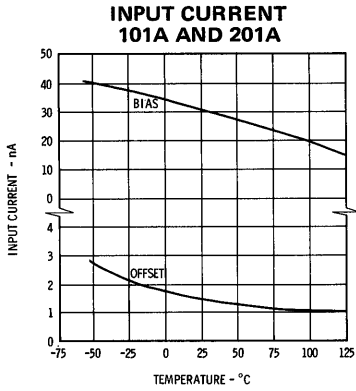
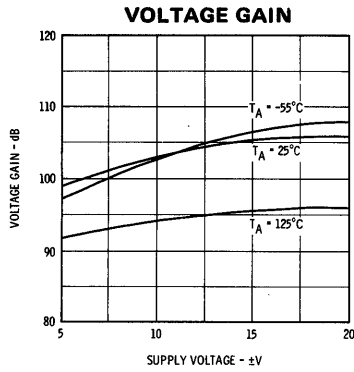
- Rating applies to ambient temperature up to $70^\circ C$. Above $70^\circ C$ ambient derate linearly at 6.3 mW/ $^\circ C$ for the Metal Can, 8.3 mW/ $^\circ C$ for the DIP, 5.6 mW/ $^\circ C$ for the Mini DIP and 7.1 mW/ $^\circ C$ for the Flatpak.
- For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply, 101A and 201A ratings apply to $+125^\circ C$ case temperature or $+75^\circ C$ ambient temperature. 301A ratings apply for case temperatures to $70^\circ C$.
- All 201A specifications apply for $-25^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.

GUARANTEED PERFORMANCE CURVES FOR 301A

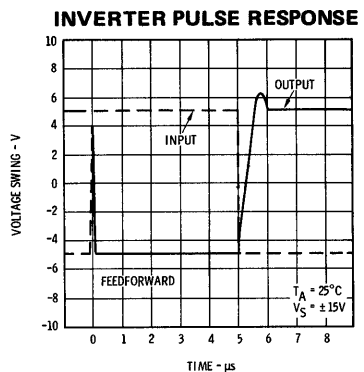
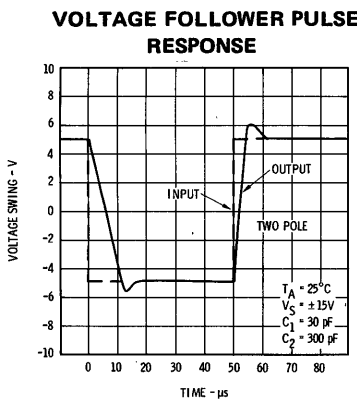
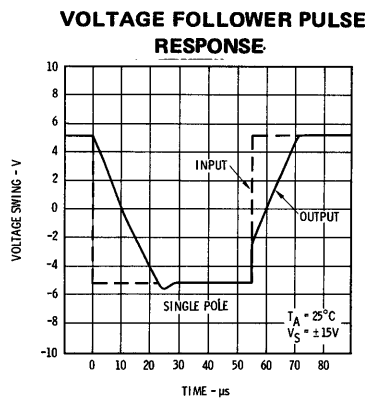
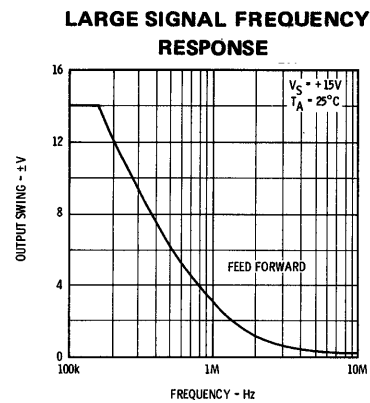
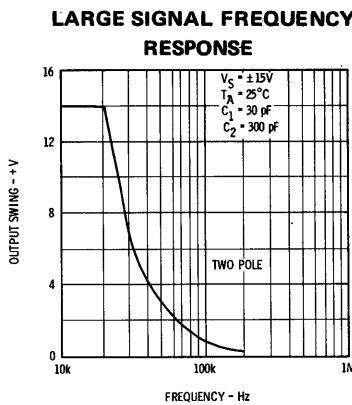
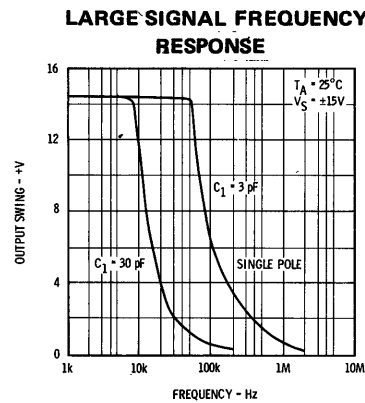
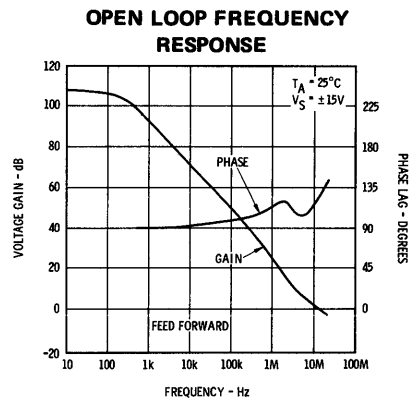
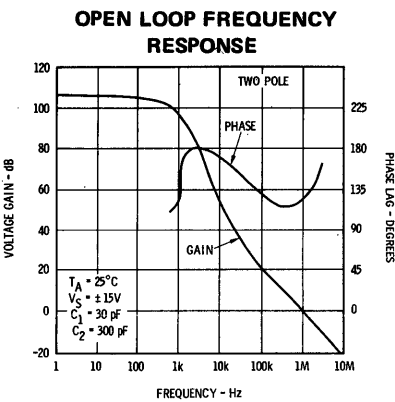
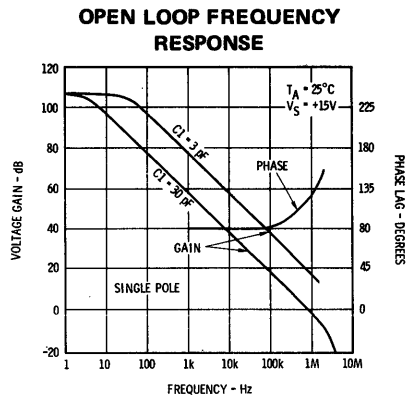


FAIRCHILD LINEAR INTEGRATED CIRCUITS • 101A • 201A • 301A

TYPICAL PERFORMANCE CURVES FOR 101A, 201A AND 301A (Unless Otherwise Specified)



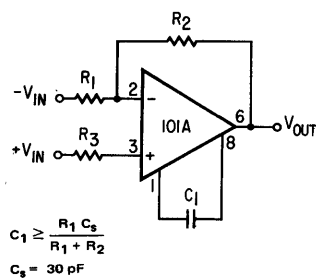
TYPICAL PERFORMANCE CURVES FOR 101A, 201A AND 301A



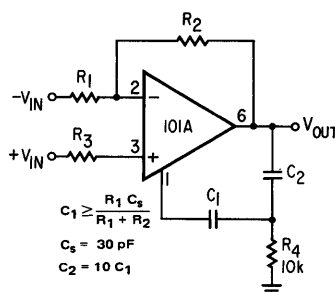
COMPENSATION CIRCUITS

(All pin numbers shown refer to 8 pin TO-5 package)

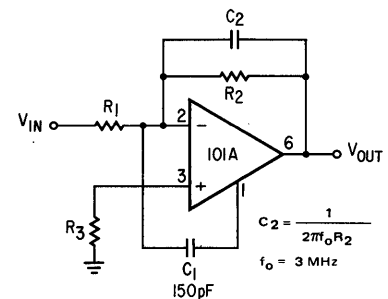
SINGLE POLE COMPENSATION



TWO POLE COMPENSATION

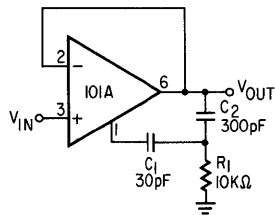


FEEDFORWARD COMPENSATION



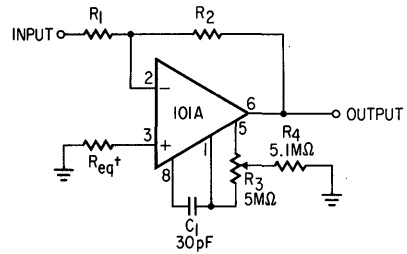
TYPICAL APPLICATIONS
(All pin numbers shown refer to 8 pin TO-5 package)

FAST VOLTAGE FOLLOWER



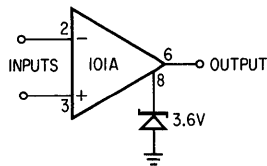
Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

**INVERTING AMPLIFIER
—WITH BALANCING CIRCUIT**

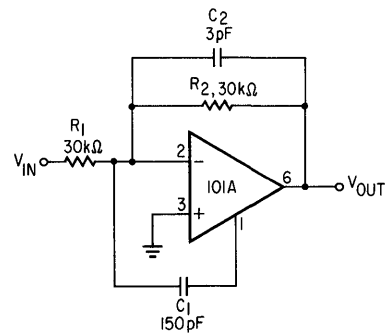


† May be zero or equal to parallel combination of R1 and R2 for minimum offset.

**VOLTAGE COMPARATOR FOR
DRIVING DTL OR TTL
INTEGRATED CIRCUITS**

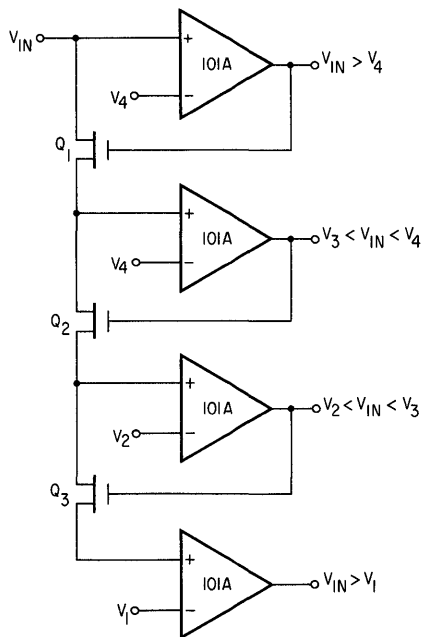


FAST SUMMING AMPLIFIER

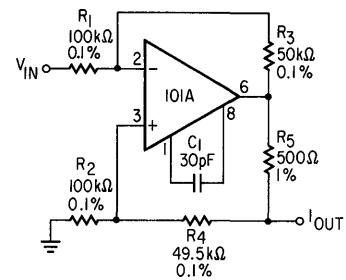


Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

**MULTIPLE APERTURE
WINDOW DISCRIMINATOR**



BILATERAL CURRENT SOURCE



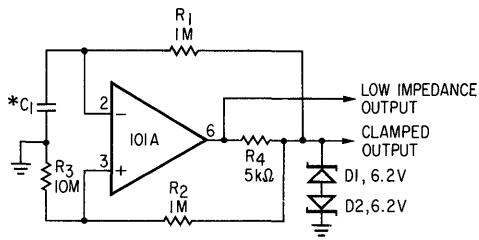
$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}$$

$$R_3 = R_4 + R_5$$

$$R_1 = R_2$$

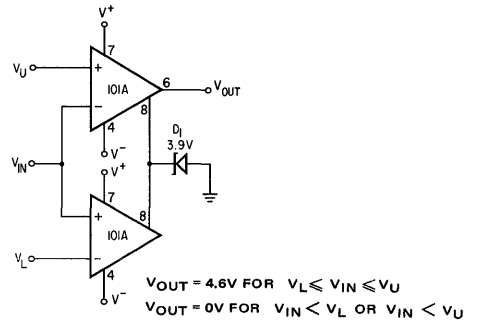
TYPICAL APPLICATIONS (CON'D)
(All pin numbers shown refer to 8 pin TO-5 package)

LOW FREQUENCY SQUARE WAVE GENERATOR



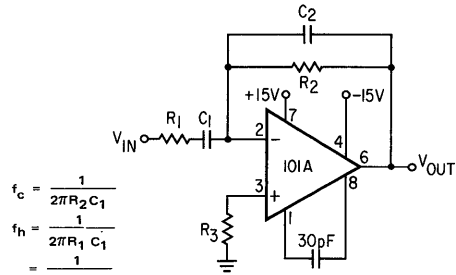
* Adjust C₁ for frequency

DOUBLE ENDED LIMIT DETECTOR



V_{OUT} = 4.6V FOR V_L ≤ V_{IN} ≤ V_U
V_{OUT} = 0V FOR V_{IN} < V_L OR V_{IN} < V_U

PRACTICAL DIFFERENTIATOR



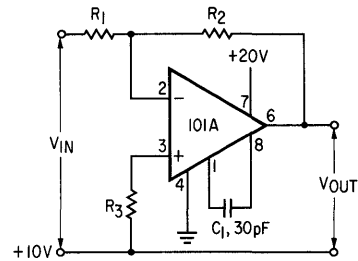
$$f_c = \frac{1}{2\pi R_2 C_1}$$

$$f_h = \frac{1}{2\pi R_1 C_1}$$

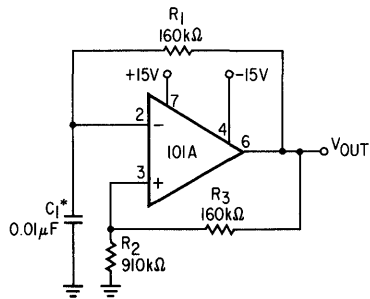
$$= \frac{1}{2\pi R_2 C_2}$$

f_c < f_h < f_{unity gain}

CIRCUIT FOR OPERATING WITHOUT A NEGATIVE SUPPLY

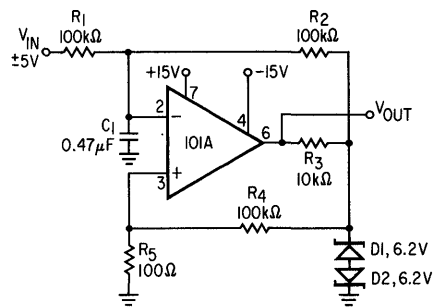


FREE-RUNNING MULTIVIBRATOR

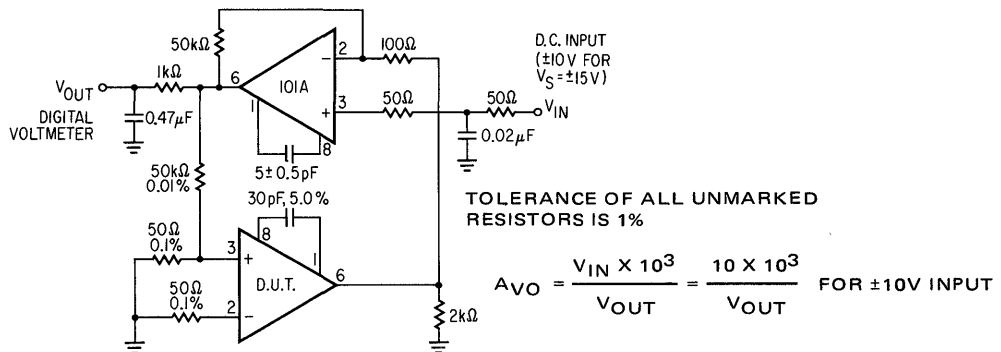


* Chosen for oscillation at 100 Hz

PULSE WIDTH MODULATOR



GAIN TEST CIRCUIT



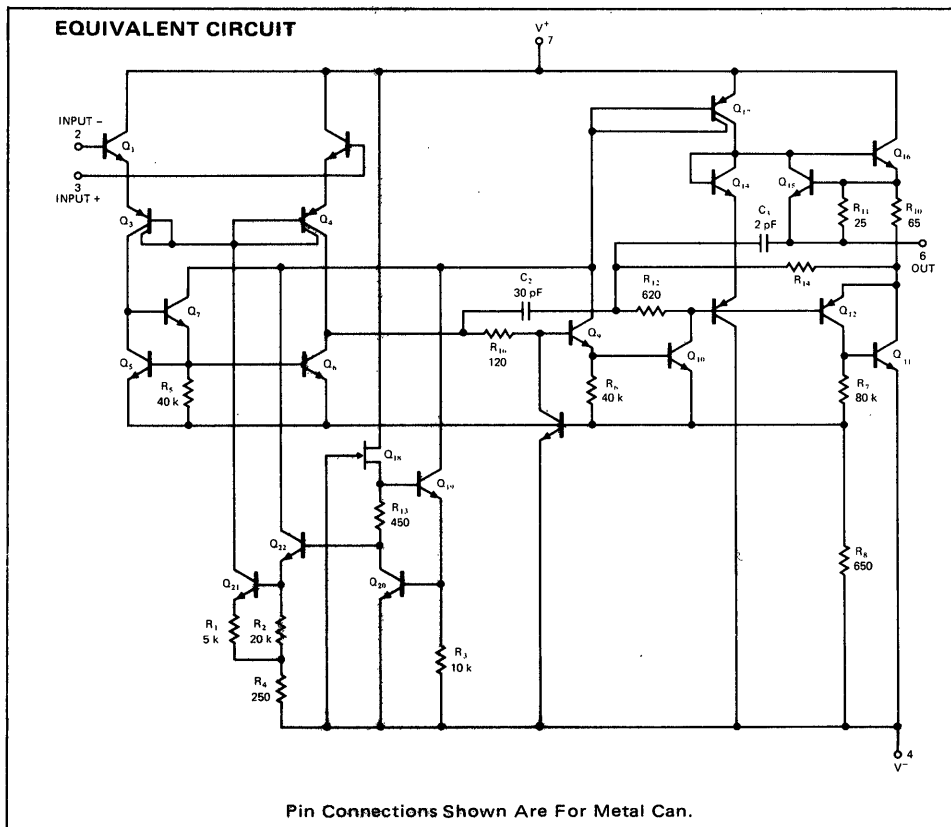
107 • 207 • 307

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

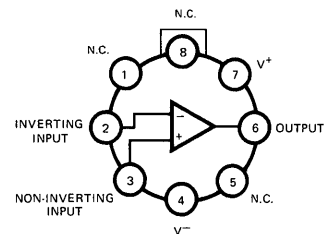
GENERAL DESCRIPTION— The 107 series of General Purpose Operational Amplifiers is constructed using the Fairchild Planar* epitaxial process. Advanced processing techniques have reduced the 107 input current an order of magnitude below industry standards such as the μ A709 while still replacing, pin-for-pin, μ A709, 101, 101A, and μ A741. The 107, 207, and 307 offer better accuracy, internal compensation, and lower noise for high impedance circuit applications while providing features similar to the 101A. The low input currents allow the device to be used in slow-charge applications such as long period integrators, slow ramps, and sample-and-hold circuits. The 207 is identical to the 107 except that 207 performance is guaranteed from -25°C to $+85^{\circ}\text{C}$ while the 107 performance is guaranteed over a -55°C to $+125^{\circ}\text{C}$ temperature range. The 307 is available in both TO-99 and 8-lead mini DIP packages and is guaranteed over a 0°C to $+70^{\circ}\text{C}$ temperature range.

- LOW OFFSET VOLTAGE
- LOW INPUT CURRENT
- LOW OFFSET CURRENT
- GUARANTEED DRIFT CHARACTERISTICS
- GUARANTEED OFFSETS OVER COMMON MODE RANGE



CONNECTION DIAGRAMS 8-LEAD METAL CAN (TOP VIEW)

PACKAGE OUTLINE 5B



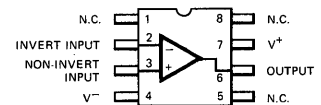
Note: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
107	LM107H
207	LM207H
307	LM307H

8-LEAD MINIDIP (TOP VIEW)

PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
307	LM307N

Dual In-line Package
and Flatpak Available
By Special Request

*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		
Military and Instrument (107 and 207)		±22 V
Commercial (307)		±18 V
Internal Power Dissipation (Note 1)		
Metal Can		500 mW
Mini DIP		310 mW
Differential Input Voltage		±30 V
Input Voltage (Note 2)		±15 V
Storage Temperature Range		
Metal Can		-65°C to +150°C
Mini DIP		-55°C to +125°C
Operating Temperature Range		
Military (107)		-55°C to +125°C
Instrument (207)		-25°C to +85°C
Commercial (307)		0°C to +70°C
Lead Temperature (Soldering)		
Metal Can (60 seconds)		300°C
Mini DIP (10 seconds)		260°C
Output Short Circuit Duration (107 and 207)		Indefinite
(307, Note 3)		Indefinite

NOTES:

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can and 5.6 mW/°C for the Mini DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.

107 AND 207

ELECTRICAL CHARACTERISTICS (±5 V ≤ V_S ≤ ±20 V, T_A = 25°C for 107 and 207) unless otherwise specified.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	R _S ≤ 10 kΩ		0.7	2.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			30	75	nA
Input Resistance		1.5	4.0		MΩ
Supply Current	V _S = ±20 V		1.8	3.0	mA
Large Signal Voltage Gain	V _S = ±15 V V _{OUT} = ±10 V, R _L ≥ 2 kΩ	50	160		V/mV
The following specs apply for 55°C ≤ T _A ≤ 125°C unless otherwise specified					
Input Offset Voltage	R _S ≤ 10 kΩ			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	μV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	25°C ≤ T _A ≤ 125°C		0.01	0.1	nA/°C
	-55°C ≤ T _A ≤ 25°C		0.02	0.2	nA/°C
Input Bias Current				100	nA
Supply Current	T _A = +125°C, V _S = ±20 V		1.2	2.5	mA
Large Signal Voltage Gain	V _S = ±15 V, V _{OUT} = ±10 V R _L ≥ 2 kΩ	25			V/mV
Output Voltage Swing	V _S = ±15 V	R _L = 10 kΩ	±12	±14	V
		R _L = 2 kΩ	±10	±13	V
Input Voltage Range	V _S = ±20 V		±15		V
Common Mode Rejection Ratio	R _S ≤ 10 kΩ	80	96		dB
Supply Voltage Rejection Ratio	R _S ≤ 10 kΩ	80	96		dB

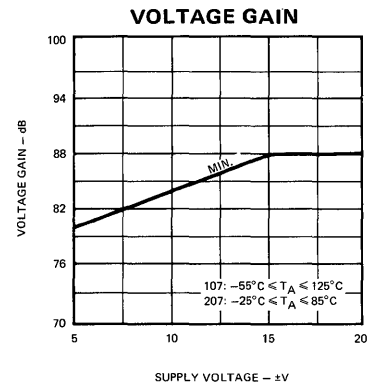
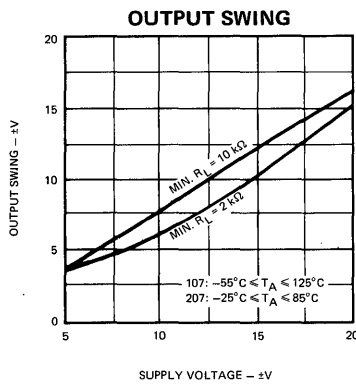
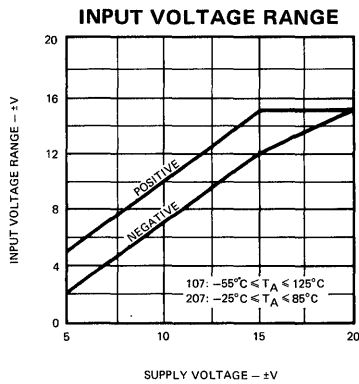
ELECTRICAL CHARACTERISTICS ($\pm 5\text{ V} \leq V_S \leq \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$		2.0	7.5	mV
Input Offset Current			3.0	50	nA
Input Bias Current			70	250	nA
Input Resistance		0.5	2.0		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$ $V_{OUT} = \pm 10\text{ V}$, $R_L \geq 2\text{ k}\Omega$	25	160		V/mV

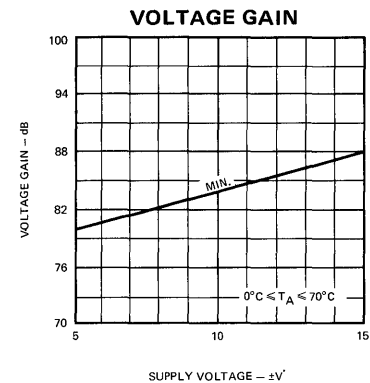
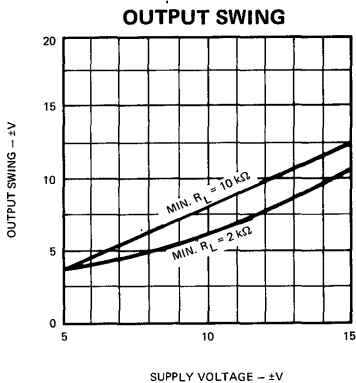
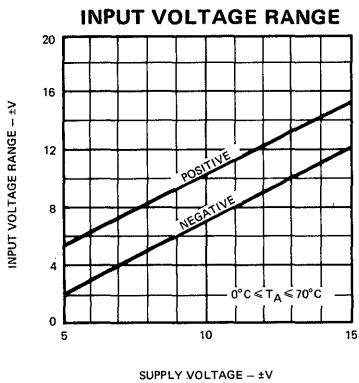
The following specifications apply for $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$

Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	$25^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.01	0.3	nA/ $^\circ\text{C}$
	$0^\circ\text{C} \leq T_A \leq 25^\circ\text{C}$		0.02	0.6	nA/ $^\circ\text{C}$
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $V_{OUT} = \pm 10\text{ V}$ $R_L \geq 2\text{ k}\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15\text{ V}$	$R_L = 10\text{ k}\Omega$ ± 12	± 14		V
		$R_L = 2\text{ k}\Omega$ ± 10	± 13		V
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 12			V
Common Mode Rejection Ratio	$R_S \leq 10\text{ k}\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{ k}\Omega$	70	96		dB

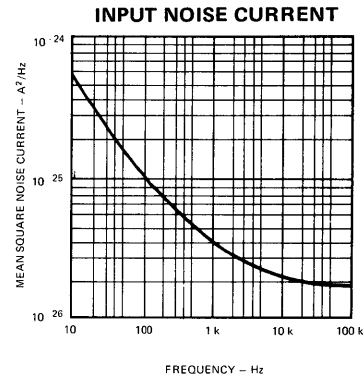
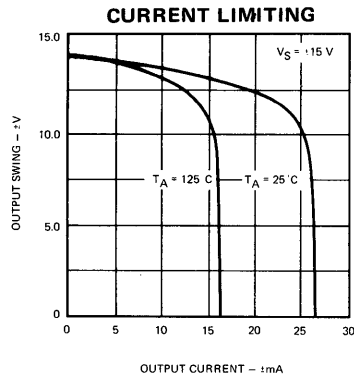
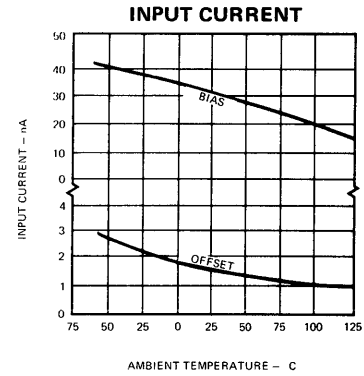
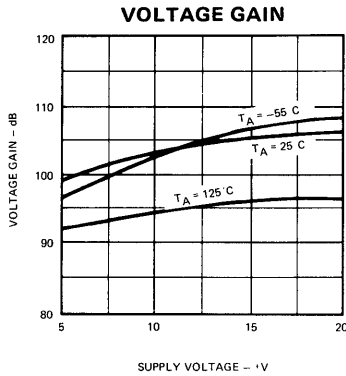
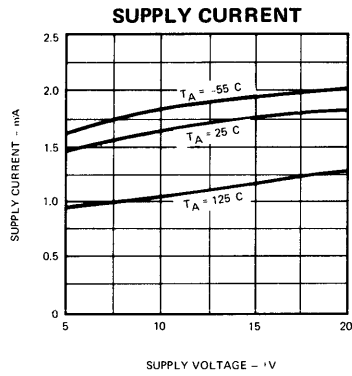
GUARANTEED PERFORMANCE CURVES FOR 107 AND 207



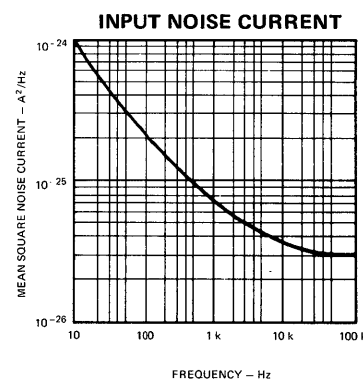
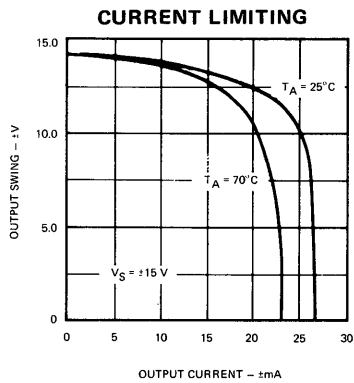
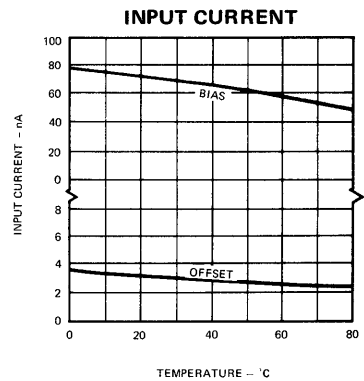
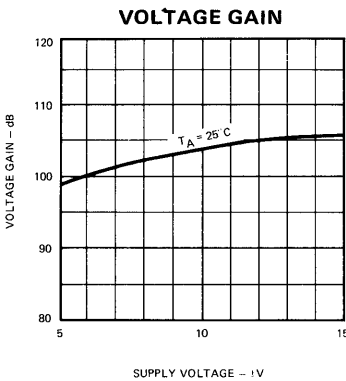
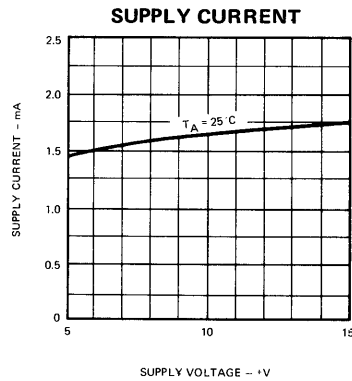
GUARANTEED PERFORMANCE CURVES FOR 307



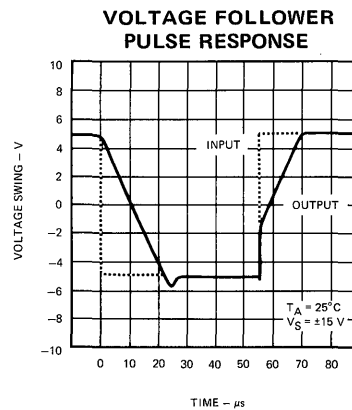
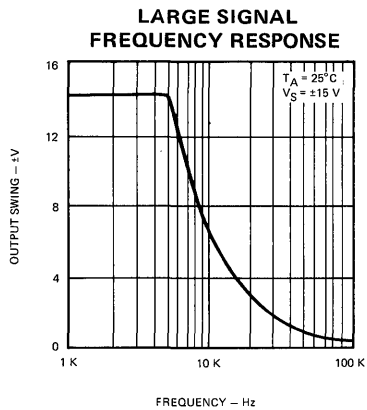
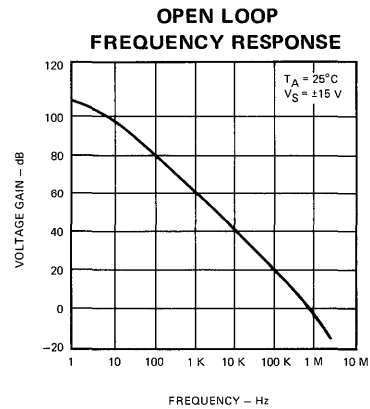
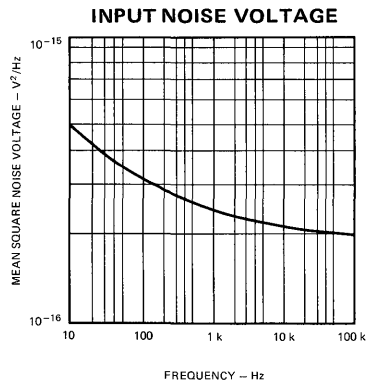
TYPICAL PERFORMANCE CURVES FOR 107 AND 207



TYPICAL PERFORMANCE CURVES FOR 307



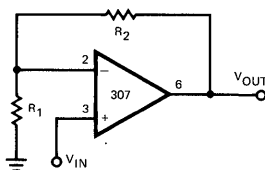
TYPICAL PERFORMANCE CURVES



TYPICAL APPLICATIONS

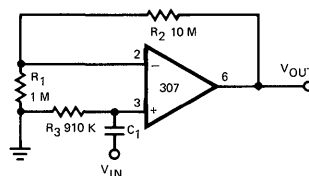
(All pin numbers shown refer to 8-lead TO-5 package)

NON-INVERTING AMPLIFIER



$$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$$

NON-INVERTING AC AMPLIFIER

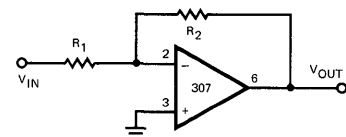


$$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$$

$$R_{IN} = R_3$$

$$R_3 = R_1 R_2$$

INVERTING AMPLIFIER



$$V_{OUT} = \frac{R_2}{R_1} V_{IN}$$

$$R_{IN} = R_1$$

108A • 208A • 308A 108 • 208 • 308

SUPER BETA OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

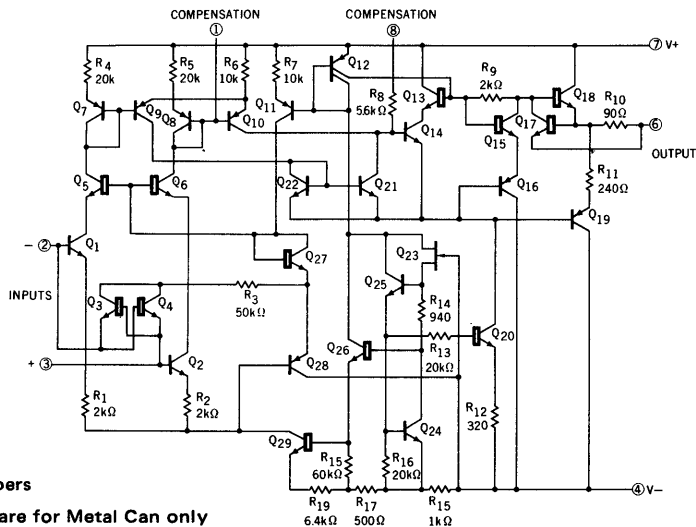
GENERAL DESCRIPTION — The 108 series of Super Beta Operational Amplifiers is constructed using the Fairchild Planar* epitaxial process. High input impedance, low noise, input offsets, and temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The 108A series is specially selected for extremely low offset voltage and drift, and high common mode rejection, making possible superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- GUARANTEED LOW INPUT OFFSET CHARACTERISTICS
- HIGH INPUT IMPEDANCE
- LOW OFFSET CURRENT
- LOW BIAS CURRENT
- OPERATION OVER WIDE SUPPLY RANGE

ABSOLUTE MAXIMUM RATINGS

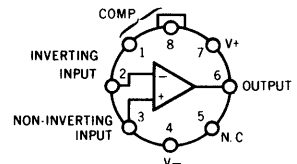
Supply Voltage	±20 V
108A, 108, 208A, 208	±18 V
308A, 308	500 mW
Internal Power Dissipation (Note 1)	±10 mA
Differential Input Current (Note 2)	±15 V
Input Voltage (Note 3)	-65°C to +150°C
Storage Temperature Range	-55°C to +125°C
Operating Temperature Range	-25°C to +85°C
Military (108A, 108)	0°C to +70°C
Industrial (208A, 208)	300°C
Commercial (308A, 308)	Indefinite
Lead Temperature (Soldering, 60 Seconds)	
Output Short Circuit Duration (Note 4)	

EQUIVALENT CIRCUIT



0 = Pin Numbers
Pin numbers are for Metal Can only

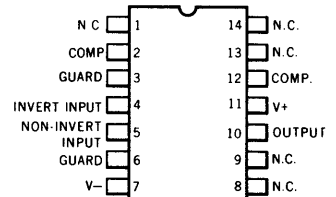
**CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B**



ORDER INFORMATION

TYPE	PART NO.
108A	LM108AH
108	LM108H
208A	LM208AH
208	LM208H
308A	LM308AH
308	LM308H

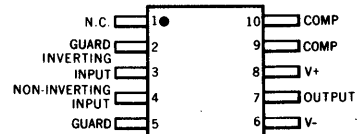
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A**



ORDER INFORMATION

TYPE	PART NO.
108A	LM108AD
108	LM108D
208A	LM208AD
208	LM208D
308A	LM308AD
308	LM308D

10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F**



ORDER INFORMATION

TYPE	PART NO.
108A	LM108AF
108	LM108F
208A	LM208AF
208	LM208F

** Available on special order

See notes on following pages.

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR IC 108A • 208A • 308A • 108 • 208 • 308

ELECTRICAL CHARACTERISTICS FOR 108A AND 208A ($\pm 5\text{ V} \leq V_S \leq \pm 20\text{ V}$, $T_A = 25^\circ\text{C}$, $C_C = 30\text{ pF}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		0.3	0.6	mA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	80,000	300,000		V/V

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (see note 5)

Input Offset Voltage				1.0	mV
Average Input Offset Voltage Drift			1.0	5.0	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	$\text{pA}/^\circ\text{C}$
Input Bias Current			0.8	3.0	nA
Supply Current	$T_A = +125^\circ\text{C}$		0.15	0.4	mA
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	40,000			V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$	± 13	± 14		V

ELECTRICAL CHARACTERISTICS FOR 308A ($\pm 5\text{ V} \leq V_S \leq \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $C_C = 30\text{ pF}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	80,000	300,000		V/V

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$

Input Offset Voltage				0.73	mV
Average Input Offset Voltage Drift			1.0	5.0	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	$\text{pA}/^\circ\text{C}$
Input Bias Current				10	nA
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	60,000			V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$	± 13	± 14		V

NOTES:

- The maximum junction temperature of the 108A/108 is 150°C , while that of the 208A/208 is 100°C , and 308A/308 is 85°C . For operating at elevated temperatures, devices in the TO-99 package must be derated based on thermal resistance of $150^\circ\text{C}/\text{W}$, junction to ambient, or $45^\circ\text{C}/\text{W}$, junction to case. For the flat package a maximum rating of 300 mW applies and derating is based on a thermal resistance of $185^\circ\text{C}/\text{W}$ when mounted on a 1/16 inch thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the Dual-In-line Package is $100^\circ\text{C}/\text{W}$, junction to ambient.
- The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless adequate limiting resistance is used.
- For supply voltages less than $\pm 15\text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to either supply or ground. Rating applies to operation up to the maximum operating temperature range.
- For the 208A/208, all temperature specifications apply over $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$.

FAIRCHILD LINEAR IC 108A • 208A • 308A • 108 • 208 • 308

ELECTRICAL CHARACTERISTICS FOR 108 AND 208 ($\pm 5\text{ V} \leq V_S \leq \pm 20\text{ V}$, $T_A = 25^\circ\text{C}$, $C_C = 30\text{ pF}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage			0.7	2.0	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		0.3	0.6	mA
Large Signal Voltage Gain	$R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$ $V_S = \pm 15\text{ V}$	50,000	300,000		V/V

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ (see note 5)

Input Offset Voltage				3.0	mV
Average Input Offset Voltage Drift			3.0	15	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	$\text{pA}/^\circ\text{C}$
Input Bias Current				3.0	nA
Supply Current	$T_A = +125^\circ\text{C}$		0.15	0.4	mA
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 13.5			V
Common Mode Rejection Ratio		85	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	25,000			V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$	± 13	± 14		V

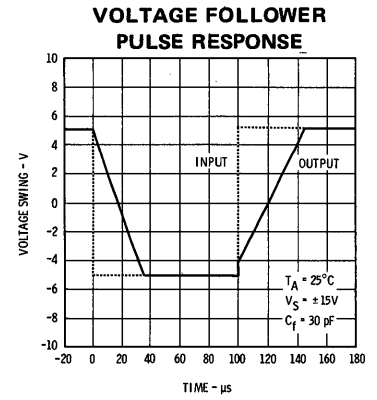
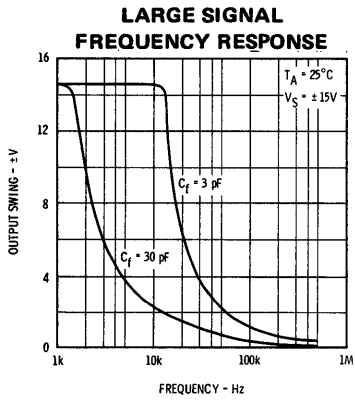
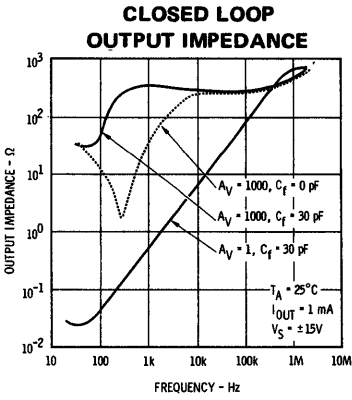
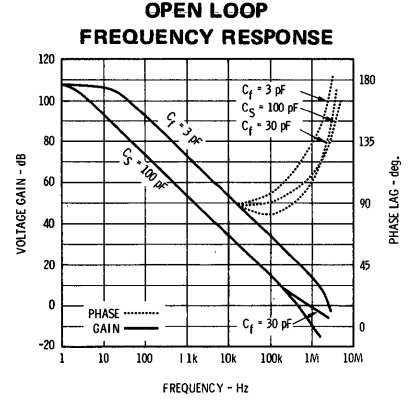
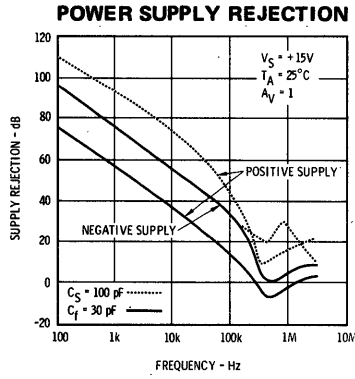
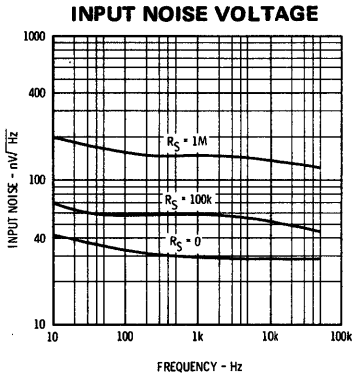
ELECTRICAL CHARACTERISTICS FOR 308 ($\pm 5\text{ V} \leq V_S \leq \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $C_C = 30\text{ pF}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage			2.0	7.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	25,000	300,000		V/V

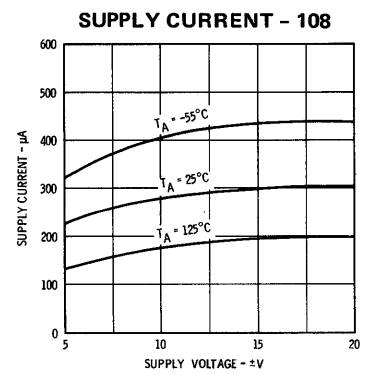
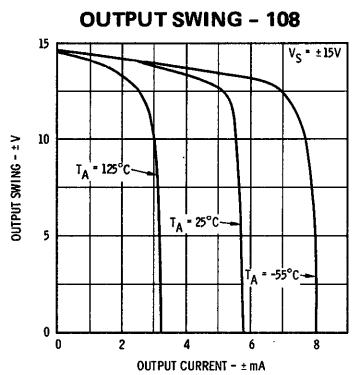
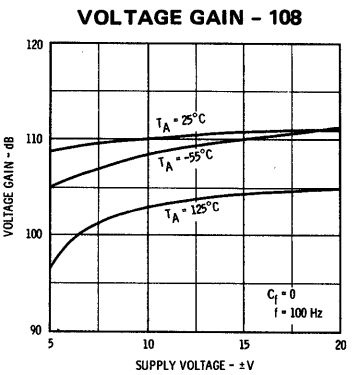
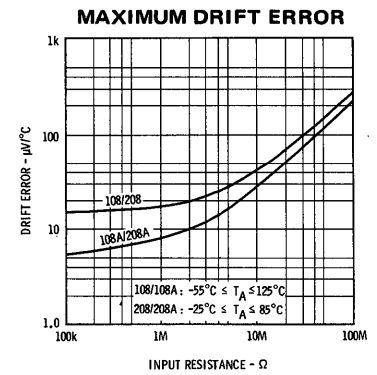
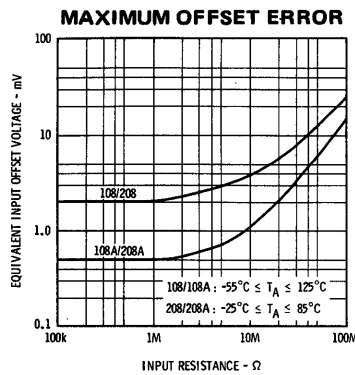
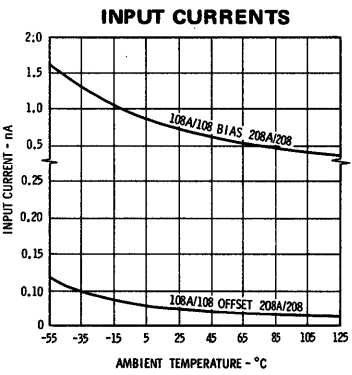
The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$

Input Offset Voltage				10	mV
Average Input Offset Voltage Drift			6.0	30	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	$\text{pA}/^\circ\text{C}$
Input Bias Current				10	nA
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 13.5			V
Common Mode Rejection Ratio		80	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	15,000			V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$	± 13	± 14		V

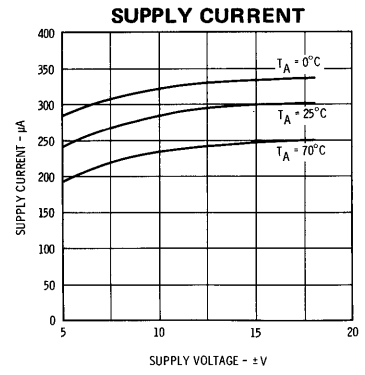
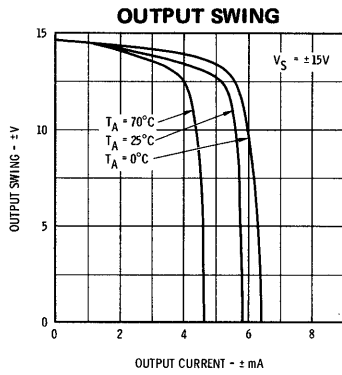
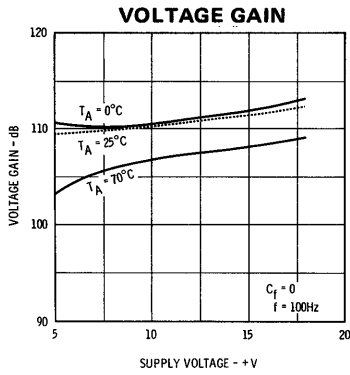
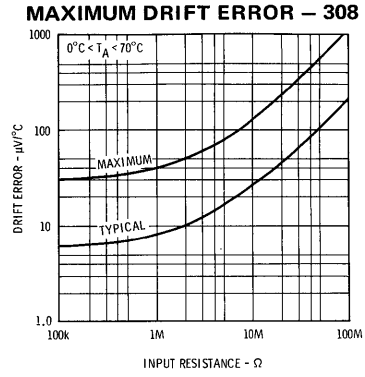
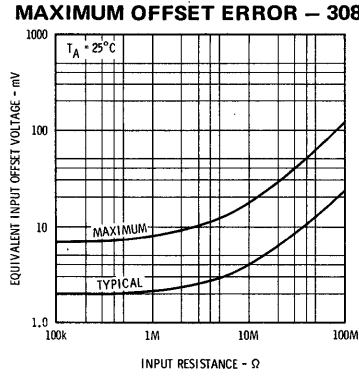
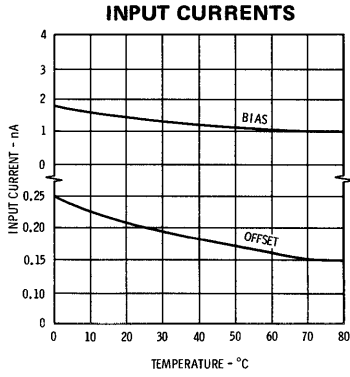
TYPICAL PERFORMANCE CURVES FOR 108 SERIES



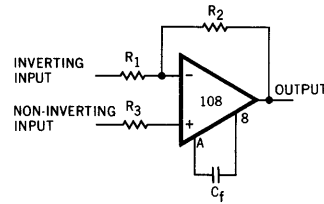
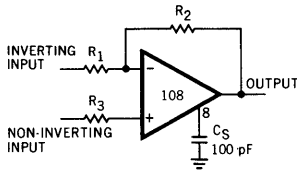
TYPICAL PERFORMANCE CURVES FOR 108A • 208A • 108 • 208 (unless otherwise specified)



TYPICAL PERFORMANCE CURVES FOR 308A AND 308 (unless otherwise specified)



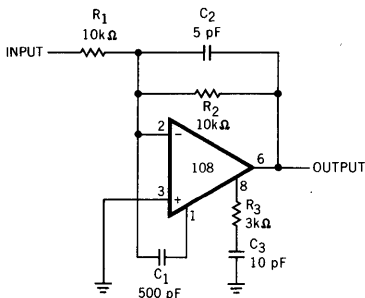
STANDARD COMPENSATION CIRCUITS



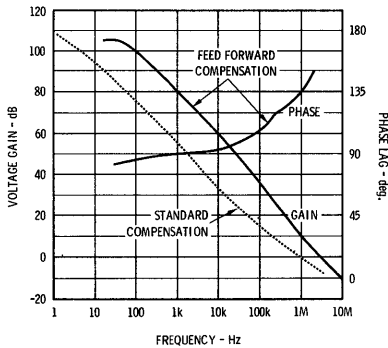
$$C_f \geq 30 \left(\frac{1}{1 + \frac{R_2}{R_1}} \right)$$

FEEDFORWARD COMPENSATION
HIGHER SLEW RATES AND WIDER BANDWIDTH

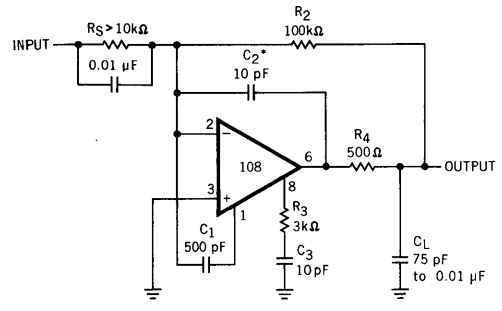
STANDARD FEEDFORWARD



OPEN LOOP VOLTAGE GAIN



FEEDFORWARD COMPENSATION
FOR DECOUPLING LOAD CAPACITANCE



$$*C_2 > \frac{5 \times 10^5}{R_2} \text{ pF}$$

GUARDING

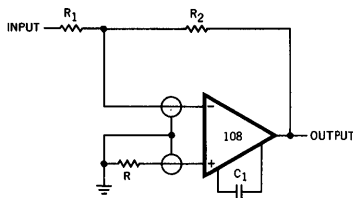
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

The pin configuration of the Dual In-line Package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard μ A741 and 101A pin configuration).

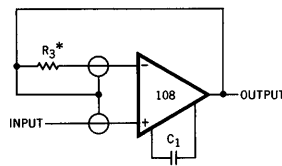
CONNECTION OF INPUT GUARDS

INVERTING AMPLIFIER



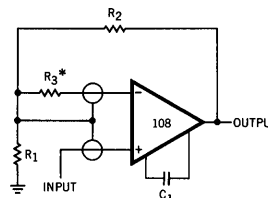
$$R = \frac{R_1 R_2}{R_1 + R_2}$$

FOLLOWER



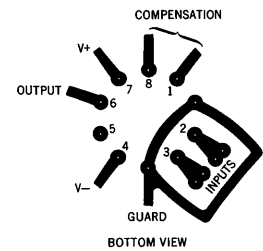
* Use to compensate for large source resistances.

NON-INVERTING AMPLIFIER



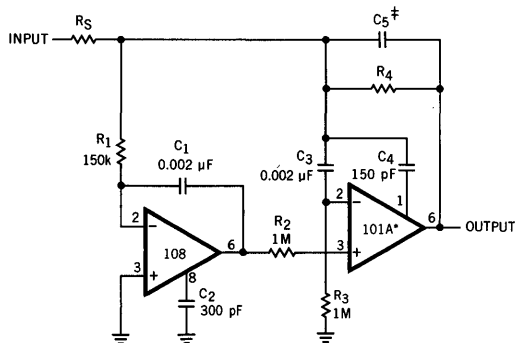
NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be low impedance

BOARD LAYOUT FOR INPUT GUARDING WITH TO-99 PACKAGE (BOTTOM VIEW)



TYPICAL APPLICATIONS

FAST[†] SUMMING AMPLIFIER WITH LOW INPUT CURRENT

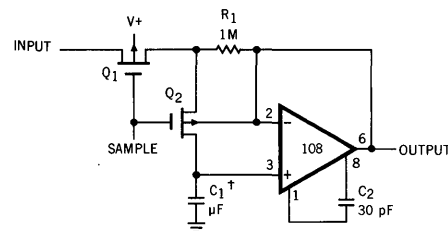


* In addition to increasing speed, the 101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/ μ s

$$\ddagger C_5 = \frac{6 \times 10^{-8}}{R_1}$$

SAMPLE AND HOLD



* Worst case drift less than 2.5 mV/s

† Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

102 • 302 • 110 • 310 VOLTAGE FOLLOWER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

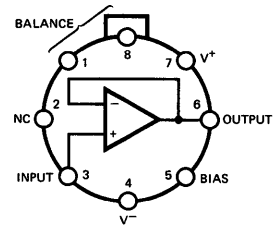
GENERAL DESCRIPTION – The 102/302 and 110/310 are monolithic Operational Amplifiers internally connected as unity gain non-inverting amplifiers. They are constructed using the Fairchild Planar* epitaxial process. These circuits are ideal for such applications as fast sample and hold circuits, active filters, or as general purpose buffers. Super-beta transistors are used allowing the devices to operate at very low input currents without sacrificing speed. They may be used interchangeably with the 101 and the $\mu A741$ in voltage follower applications. The 110/310 are suggested for new designs and are direct replacements for the 102/302. They feature lower offset voltage, drift, bias current, noise, plus higher speed and a wider operating voltage range.

- HIGH SLEW RATE . . . 30 V/ μ s
- LOW INPUT CURRENT
- INTERNALLY COMPENSATED
- PLUG-IN REPLACEMENT FOR BOTH THE 101 AND $\mu A741$ VOLTAGE FOLLOWER APPLICATIONS
- WIDE RANGE OF SUPPLY VOLTAGES

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 18 V
Internal Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	± 15 V
Output Short Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	-65° C to $+150^{\circ}$ C
Operating Temperature Range	
Military (102/110)	-55° C to $+125^{\circ}$ C
Commercial (302/310)	0° C to $+70^{\circ}$ C
Lead Temperature (soldering, 60 seconds)	300° C

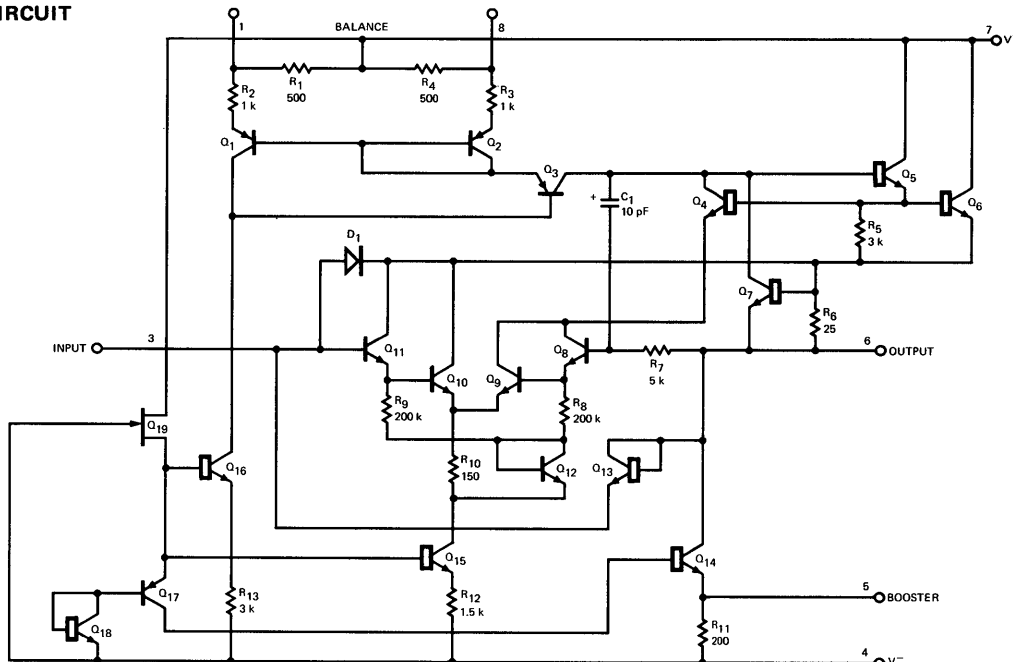
**CONNECTION DIAGRAM
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B**



ORDER INFORMATION

TYPE	PART NO.
102	LM102H
302	LM302H
110	LM110H
310	LM310H

EQUIVALENT CIRCUIT



102

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L \leq 100\text{ pF}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Offset Voltage			2.0	5.0	mV
Average Temperature Coefficient of Offset Voltage			6.0		$\mu\text{V}/^\circ\text{C}$
Input Current			3.0	10	nA
Input Resistance		10^{10}	10^{12}		Ω
Voltage Gain	$R_L \geq 10\text{ k}\Omega$	0.999	0.9996		
Output Resistance			0.8	2.5	Ω
Output Voltage Swing (Note 4)	$R_L \geq 8\text{ k}\Omega$	± 10	± 13		V
Supply Current			3.5	5.5	mA
Positive Supply Rejection		60			dB
Negative Supply Rejection		70			dB
Input Capacitance				3.0	pF
Offset Voltage	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			7.5	mV
Input Current	$T_A = 125^\circ\text{C}$		3.0	10	nA
	$T_A = -55^\circ\text{C}$		30	100	nA
Voltage Gain	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ $R_L \geq 10\text{ k}\Omega$	0.999			
Output Voltage Swing	$R_L \geq 10\text{ k}\Omega$	± 10			V
Supply Current	$T_A = 125^\circ\text{C}$		2.6	4.0	mA

302

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L \leq 100\text{ pF}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Offset Voltage			5.0	15	mV
Average Temperature Coefficient of Offset Voltage			20		$\mu\text{V}/^\circ\text{C}$
Input Current			10	30	nA
Input Resistance		10^9	10^{12}		Ω
Voltage Gain	$R_L > 8\text{ k}\Omega$	0.9985	0.9995	1.000	
Output Resistance			0.8	2.5	Ω
Output Voltage Swing (Note 4)	$R_L \geq 8\text{ k}\Omega$	± 10			V
Supply Current			3.5	5.5	mA
Positive Supply Rejection		60			dB
Negative Supply Rejection		70			dB
Input Capacitance			3.0		pF
Offset Voltage	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$			20	mV
Input Current	$T_A = 70^\circ\text{C}$		3.0	15	nA
	$T_A = 0^\circ\text{C}$		20	50	nA

110

ELECTRICAL CHARACTERISTICS ($\pm 5\text{ V} \leq V_S \leq \pm 18\text{ V}$, $-55^\circ\text{C} < T_A \leq 125^\circ\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$T_A = 25^\circ\text{C}$		1.5	4.0	mV
Input Bias Current	$T_A = 25^\circ\text{C}$		1.0	3.0	nA
Input Resistance	$T_A = 25^\circ\text{C}$	10^{10}	10^{12}		Ω
Input Capacitance			1.5		pF
Large Signal Voltage Gain	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ $V_{OUT} = \pm 10\text{ V}$, $R_L = 8\text{ k}\Omega$	0.999	0.9999		
Output Resistance	$T_A = 25^\circ\text{C}$		0.75	2.5	Ω
Supply Current	$T_A = 25^\circ\text{C}$		3.9	5.5	mA
Input Offset Voltage				6.0	mV
Offset Voltage Temperature Drift	$-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		6.0		$\mu\text{V}/^\circ\text{C}$
	$T_A = 125^\circ\text{C}$		12		$\mu\text{V}/^\circ\text{C}$
Input Bias Current				10	nA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $V_{OUT} = \pm 10\text{ V}$ $R_L = 10\text{ k}\Omega$	0.999			
Output Voltage Swing (Note 4)	$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$	± 10			V
Supply Current	$T_A = 125^\circ\text{C}$		2.0	4.0	mA
Supply Voltage Rejection Ratio	$\pm 5\text{ V} \leq V_S \leq \pm 18\text{ V}$	70	80		dB

310

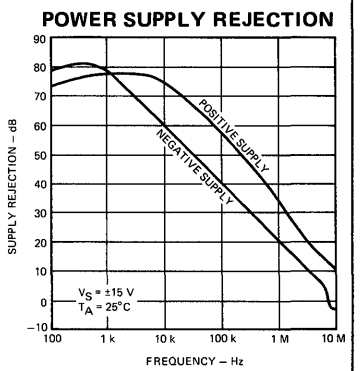
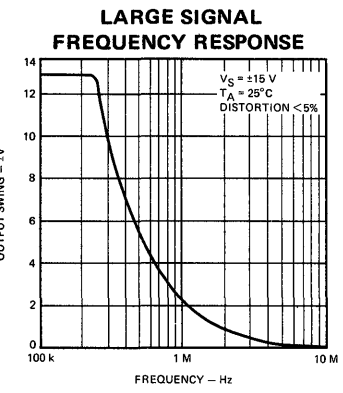
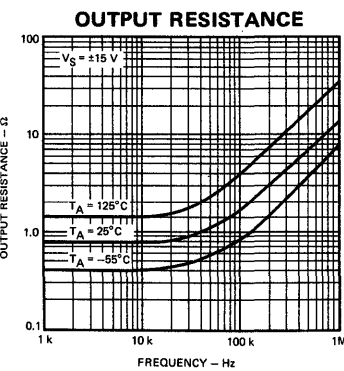
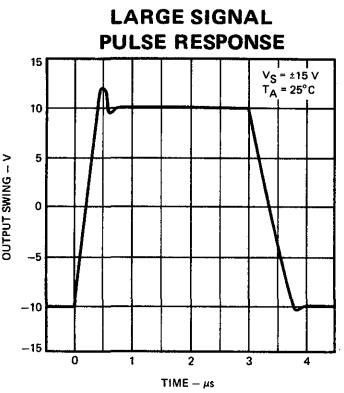
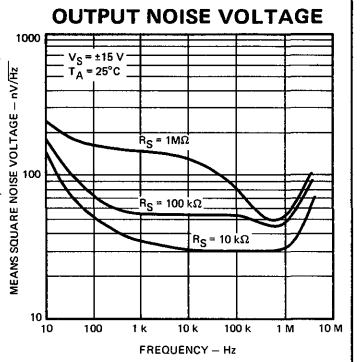
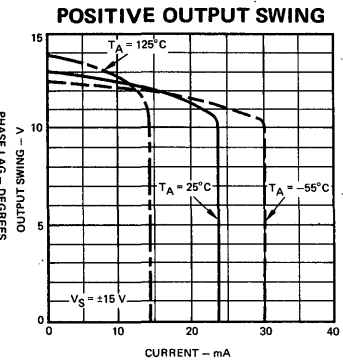
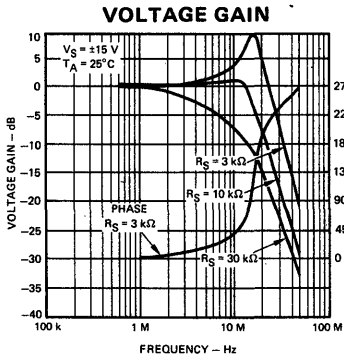
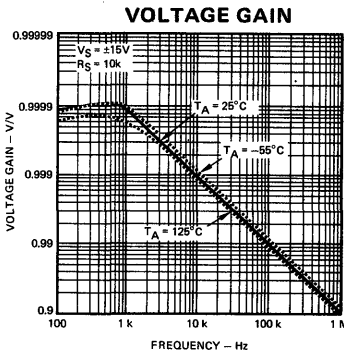
ELECTRICAL CHARACTERISTICS ($\pm 5\text{ V} \leq V_S \leq \pm 18\text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$T_A = 25^\circ\text{C}$		2.5	7.5	mV
Input Bias Current	$T_A = 25^\circ\text{C}$		2.0	7.0	nA
Input Resistance	$T_A = 25^\circ\text{C}$	10^{10}	10^{12}		Ω
Input Capacitance			1.5		pF
Large Signal Voltage Gain	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ $V_{OUT} = \pm 10\text{ V}$, $R_L = 8\text{ k}\Omega$	0.999	0.9999		
Output Resistance	$T_A = 25^\circ\text{C}$		0.75	2.5	Ω
Supply Current	$T_A = 25^\circ\text{C}$		3.9	5.5	mA
Input Offset Voltage				10	mV
Offset Voltage Temperature Drift			10		$\mu\text{V}/^\circ\text{C}$
Input Bias Current				10	nA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $V_{OUT} = \pm 10\text{ V}$ $R_L = 10\text{ k}\Omega$	0.999			
Output Voltage Swing (Note 4)	$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$	± 10			V
Supply Voltage Rejection Ratio	$\pm 5\text{ V} \leq V_S \leq \pm 18\text{ V}$	70	80		dB

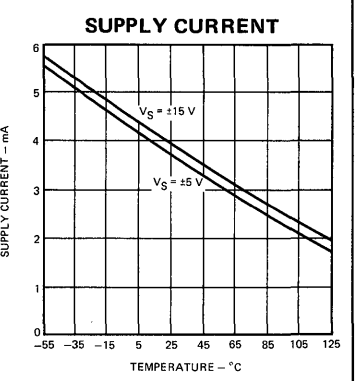
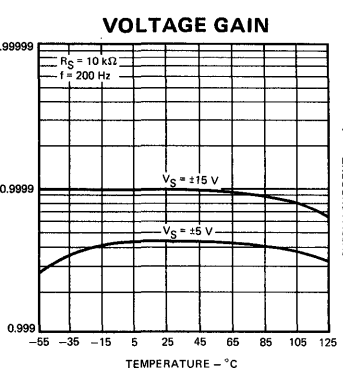
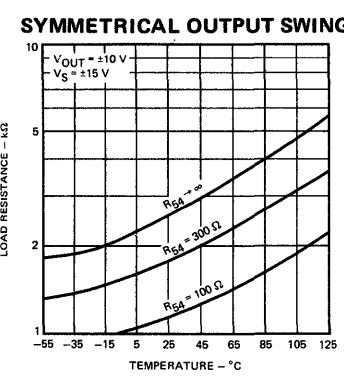
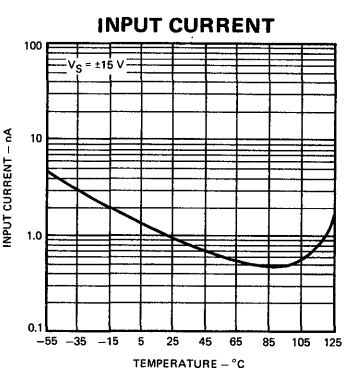
NOTES:

- Rating applies to ambient temperatures up to $+70^\circ\text{C}$. Above $+70^\circ\text{C}$ ambient, derate linearly at $6.3\text{ mW}/^\circ\text{C}$.
- For supply voltages less than $\pm 15\text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
- For 102 and 110 continuous short circuit is allowed for case temperature of $+125^\circ\text{C}$ and ambient temperature to $+70^\circ\text{C}$. For 302 and 310 continuous short circuit is allowed for case temperature to $+70^\circ\text{C}$ and ambient temperature to $+55^\circ\text{C}$. It is necessary to insert a resistor greater than $2\text{ k}\Omega$ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.
- Increased output swing under load can be obtained by connecting an external resistor between the booster and V_- terminals (see curve).

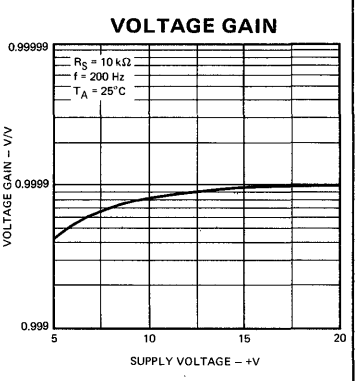
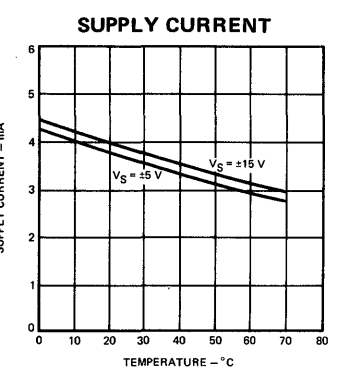
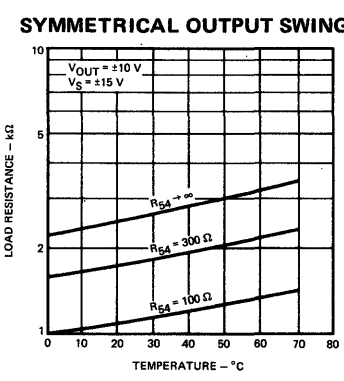
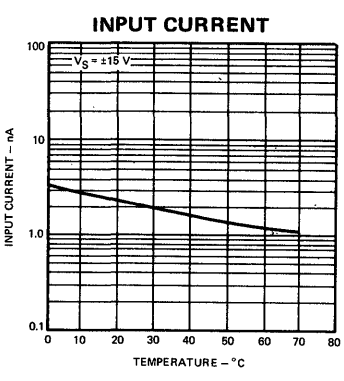
TYPICAL PERFORMANCE CURVES FOR 102/302, 110/310



TYPICAL PERFORMANCE CURVES FOR 102/110

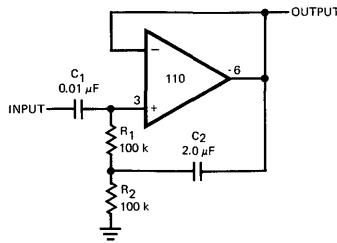


TYPICAL PERFORMANCE CURVES FOR 302/310

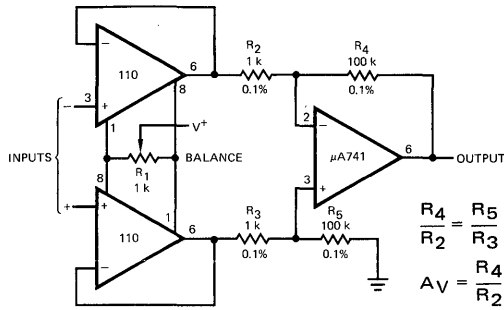


TYPICAL APPLICATIONS

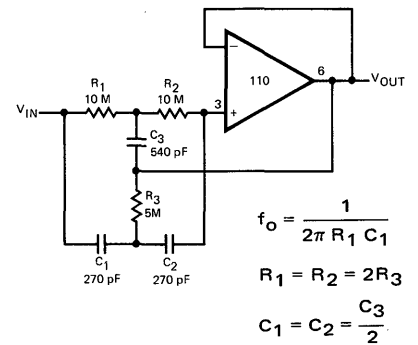
HIGH INPUT IMPEDANCE AC AMPLIFIER



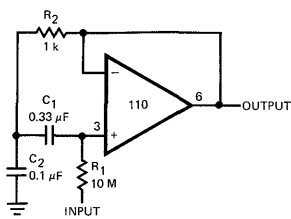
DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



HIGH Q NOTCH FILTER

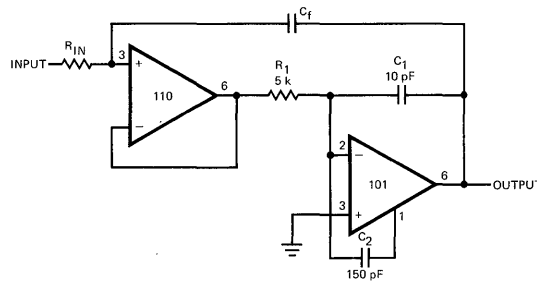


BANDPASS FILTER

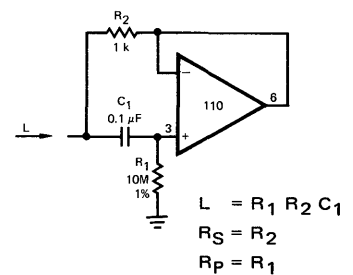


$$f_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

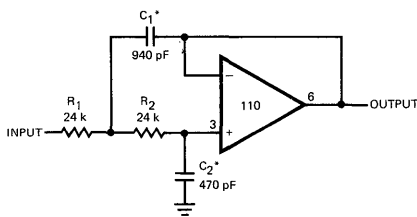
FAST INTEGRATOR WITH LOW INPUT CURRENT



SIMULATED INDUCTOR

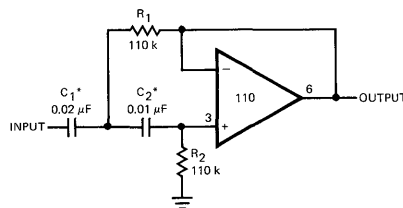


LOW PASS ACTIVE FILTER



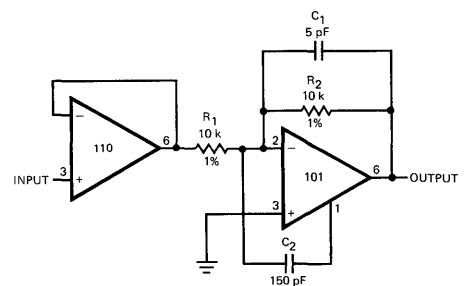
* Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

HIGH PASS ACTIVE FILTER

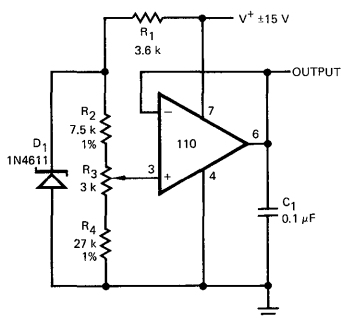


* Values are 100 Hz cutoff. Use metallized polycarbonate capacitors for good temperature stability

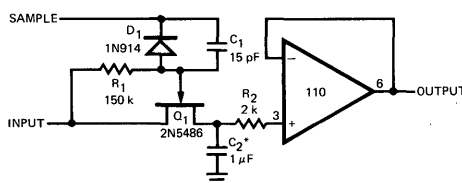
FAST INVERTING AMPLIFIER WITH HIGH INPUT IMPEDANCE



BUFFERED REFERENCE SOURCE

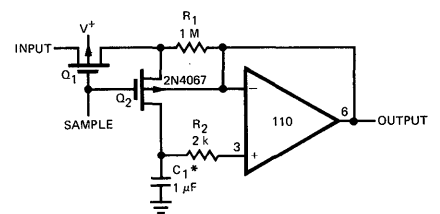


SAMPLE AND HOLD



* Use capacitor with polycarbonate teflon or polyethylene dielectric.

LOW DRIFT SAMPLE AND HOLD**



* Teflon, polyethylene or polycarbonate dielectric capacitor

** Worst case drift less than 3 mV/s

1558 • 1458 • 1458C

INTERNALLY COMPENSATED, HIGH PERFORMANCE DUAL MONOLITHIC OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

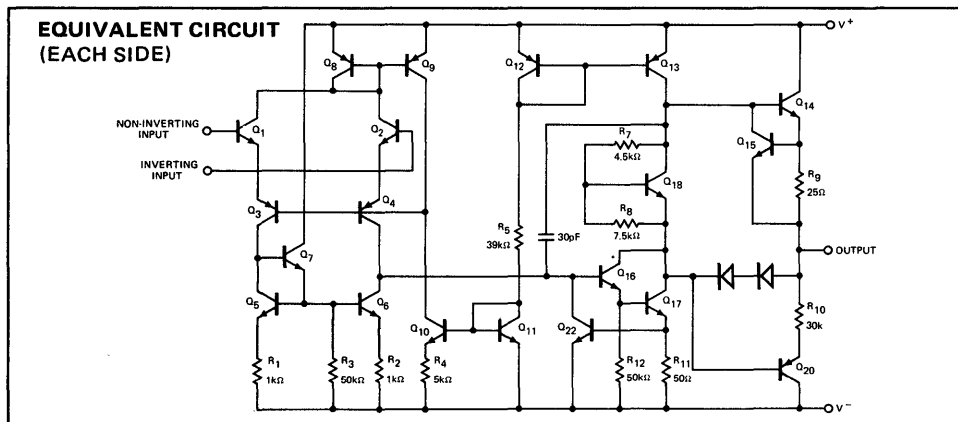
GENERAL DESCRIPTION — The 1558/1458 are a monolithic pair of Internally Compensated High Performance Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the 1558/1458 ideal for use as voltage followers. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

The 1558/1458 are short-circuit protected and require no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see the μ A741 data sheet.

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP
- MINI DIP PACKAGE

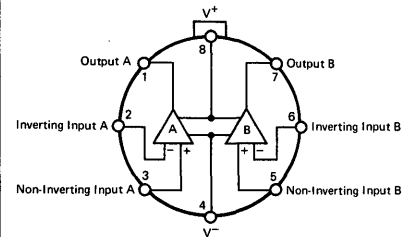
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military (1558)	± 22 V
Commercial (1458 and 1458C)	± 18 V
Internal Power Dissipation (Note 1)	
Metal Can	800 mW
Mini DIP	560 mW
Differential Input Voltage (Note 2)	± 30 V
Common-Mode Input Swing (Note 2)	± 15 V
Output Short Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	
Military (1558)	-55°C to $+125^{\circ}\text{C}$
Commercial (1458 and 1458C)	0°C to 70°C
Lead Temperature	
Metal Can (Soldering, 60 seconds)	300°C
Mini DIP (Soldering, 10 seconds)	260°C



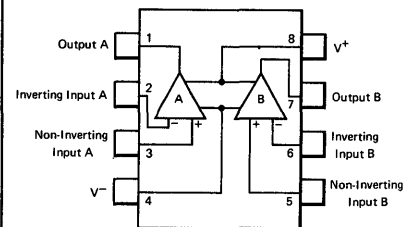
Notes on following page.

CONNECTION DIAGRAMS 8-LEAD METAL CAN (TOP VIEW) PACKAGE OUTLINE 5B



ORDER INFORMATION	
TYPE	PART NO.
1558	MC1558G
1458	MC1458G
1458C	MC1458CG

8-LEAD MINI DIP (TOP VIEW) PACKAGE OUTLINE 9T



ORDER INFORMATION	
TYPE	PART NO.
1458	1458PI
1458C	1458CPI

*Planar is a patented Fairchild process.

1558

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0	mV
Input Offset Current			0.03	0.2	μA
Input Bias Current			0.2	0.5	μA
Differential Input Impedance					
Parallel Input Resistance	$f = 20Hz$, Open Loop	0.3	1.0		$M\Omega$
Parallel Input Capacitance			6.0		pF
Common-Mode Input Impedance	$f = 20Hz$		200		$M\Omega$
Common-Mode Input Voltage Swing		± 12	± 13		V
Equivalent Input Noise Voltage	$A_V = 100$, $R_S = 10k\Omega$, $f = 1.0kHz$, $BW = 1.0Hz$		45		nV/\sqrt{Hz}
Common-Mode Rejection Ratio	$f = 100Hz$	70	90		dB
Open-Loop Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2.0k\Omega$	50k	200k		V/V
Power Bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, $THD \leq 5\%$, $V_O = 20V_{p-p}$		14		kHz
Unity Gain Crossover Frequency (Open Loop)			1.1		MHz
Phase Margin (Open Loop, Unity Gain)			65		Degrees
Gain Margin			11		dB
Slew Rate	$A_V = 1$		0.8		$V/\mu s$
Output Impedance	$f = 20Hz$		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	$R_L = 10k\Omega$	± 12	± 14		V
Power Supply Sensitivity					
$V_- = \text{Constant}$	$R_S \leq 10k\Omega$		30	150	$\mu V/V$
$V_+ = \text{Constant}$			30	150	$\mu V/V$
Power Supply Current	I_+		2.3	5.0	mA
	I_-		2.3	5.0	mA
Power Dissipation	$V_{OUT} = 0$		70	150	mW

The Following Specifications Apply For $-55^\circ C \leq T_A \leq +125^\circ C$

Input Offset Voltage	$R_S \leq 10k\Omega$			6.0	mV
Input Offset Current				0.5	μA
Input Bias Current				1.5	μA
Open-Loop Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2.0k\Omega$	25k			V/V
Output Voltage Swing	$R_L = 2k\Omega$	± 10	± 13		V
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		15		$\mu V/^\circ C$

NOTES:

1. Rating applies to ambient temperatures up to $25^\circ C$. Above $25^\circ C$ ambient derate linearly at $6.3 mW/^\circ C$ for the metal can and $5.6 mW/^\circ C$ for the mini DIP.
2. For supply voltages less than $\pm 15 V$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to $+125^\circ C$ case temperature or $70^\circ C$ ambient temperature.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 1558 • 1458 • 1458C

1458

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0	mV
Input Offset Current			.03	0.2	μA
Input Bias Current			0.2	0.5	μA
Differential Input Impedance					
Parallel Input Resistance	$f = 20Hz$, Open Loop	0.3	1.0		$M\Omega$
Parallel Input Capacitance			6.0		pF
Common-Mode Input Impedance	$f = 20Hz$		200		$M\Omega$
Common-Mode Input Voltage Swing		± 12	± 13		V
Equivalent Input Noise Voltage	$A_V = 100$, $R_S = 10k\Omega$, $f = 1.0kHz$, $BW = 1.0Hz$		45		nV/\sqrt{Hz}
Common-Mode Rejection Ratio	$f = 100Hz$	70	90		dB
Open-Loop Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2.0k\Omega$	20k	100k		V/V
Power Bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, THD $\leq 5\%$, $V_O = 20V_{p-p}$		14		kHz
Unity Gain Crossover Frequency (Open-Loop)			1.1		MHz
Phase Margin (Open-Loop, Unity Gain)			65		Degrees
Gain Margin			11		dB
Slew Rate	$A_V = 1$		0.8		V/ μs
Output Impedance	$f = 20Hz$		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	$R_L = 10k\Omega$	± 12	± 14		V
Power Supply Sensitivity					
$V_- = \text{Constant}$	$R_S \leq 10k\Omega$		30	150	$\mu V/V$
$V_+ = \text{Constant}$			30	150	$\mu V/V$
Power Supply Current	I_+		2.3	5.6	mA
	I_-		2.3	5.6	mA
Power Dissipation	$V_{OUT} = 0$		70	170	mW

The Following Specifications Apply For $0^\circ C \leq T_A \leq 70^\circ C$

Input Offset Voltage	$R_S \leq 10k\Omega$			7.5	mV
Input Offset Current				0.3	μA
Input Bias Current				0.8	μA
Open Loop Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2.0k\Omega$	15k			V/V
Output Voltage Swing	$R_L = 2.0k\Omega$	± 10	± 13		V
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		15		$\mu V/^\circ C$

1458C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	10	mV
Input Offset Current			.03	0.3	μA
Input Bias Current			0.2	0.7	μA
Differential Input Impedance					
Parallel Input Resistance	$f = 20Hz$, Open Loop		1.0		$M\Omega$
Parallel Input Capacitance			6.0		pF
Common-Mode Input Impedance	$f = 20Hz$		200		$M\Omega$
Common-Mode Input Voltage Swing		± 11	± 13		V
Equivalent Input Noise Voltage	$A_V = 100$, $R_S = 10k\Omega$, $f = 1.0kHz$, $BW = 1.0Hz$		45		nV/\sqrt{Hz}
Common-Mode Rejection Ratio	$f = 100Hz$	60	90		dB
Open-Loop Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 10k\Omega$	20k	100k		V/V
Power Bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, $THD \leq 5\%$, $V_O = 20V_{p-p}$		14		kHz
Unity Gain Crossover Frequency (Open-Loop)			1.1		MHz
Phase Margin (Open-Loop, Unity Gain)			65		Degrees
Gain Margin			11		dB
Slew Rate	$A_V = 1$		0.8		$V/\mu s$
Output Impedance	$f = 20Hz$		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	$R_L = 10k\Omega$	± 11	± 14		V
Power Supply Sensitivity					
$V_- = \text{Constant}$	$R_S \leq 10k\Omega$		30		$\mu V/V$
$V_+ = \text{Constant}$			30		$\mu V/V$
Power Supply Current	I_+		2.3	8.0	mA
	I_-		2.3	8.0	mA
Power Dissipation	$V_{OUT} = 0$		70	240	mW

The Following Specifications Apply For $0^\circ C \leq T_A \leq +70^\circ C$

Input Offset Voltage	$R_S \leq 10k\Omega$			12	mV
Input Offset Current				0.4	μA
Input Bias Current				1.0	μA
Open Loop Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 10k\Omega$	15k			V/V
Output Voltage Swing	$R_L = 2.0k\Omega$	± 9.0	± 13		V
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		15		$\mu V/^\circ C$

TYPICAL PERFORMANCE CURVES FOR 1558, 1458 AND 1458C

($V_+ = +15V$, $V_- = -15V$, $T_A = 25^\circ C$ unless otherwise noted)

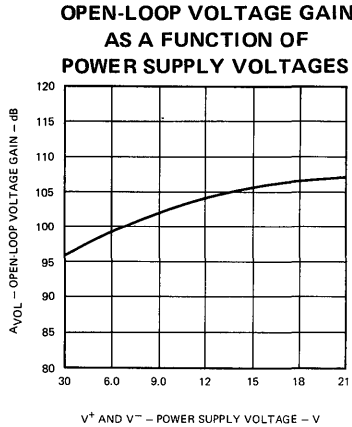


Fig. 1

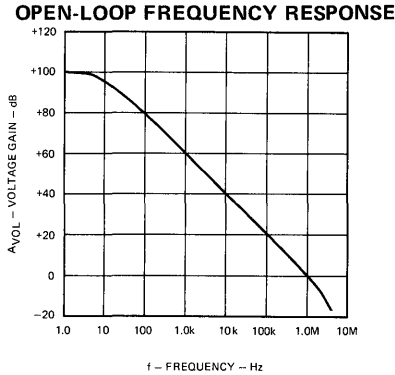


Fig. 2

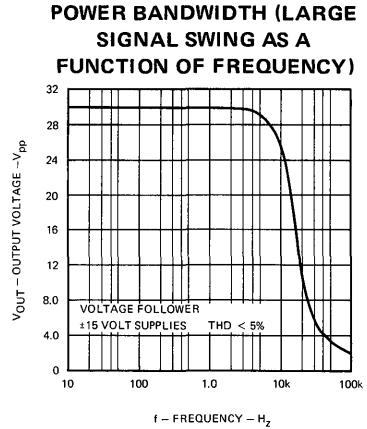


Fig. 3

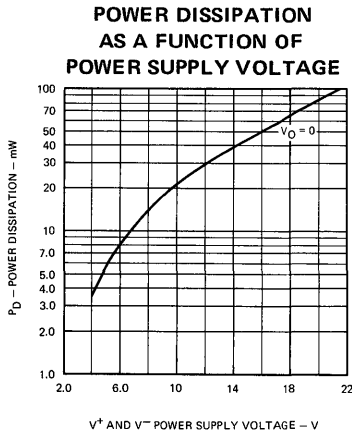


Fig. 4

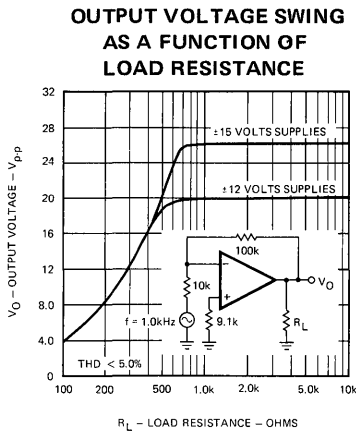


Fig. 5

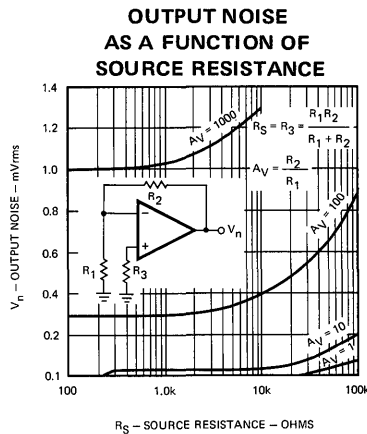


Fig. 6

HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER

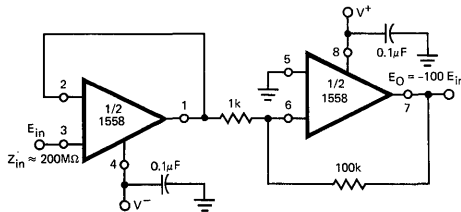


Fig. 7

QUADRATURE OSCILLATOR

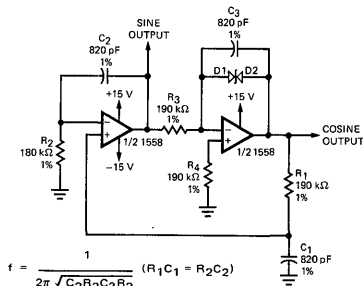


Fig. 8

ANALOG MULTIPLIER

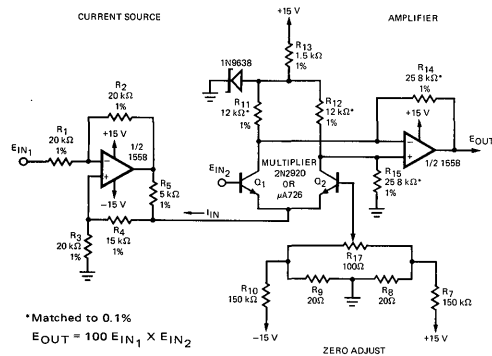


Fig. 9

COMPRESSOR/EXPANDER AMPLIFIERS

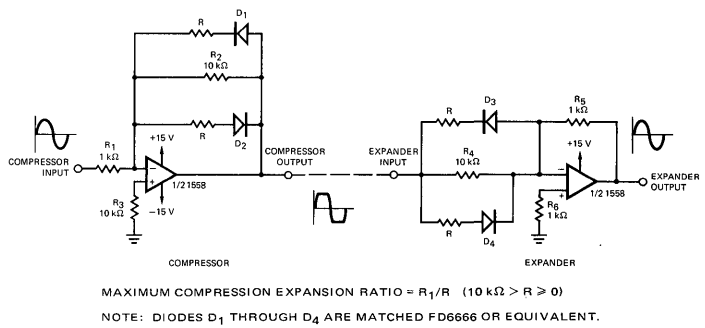


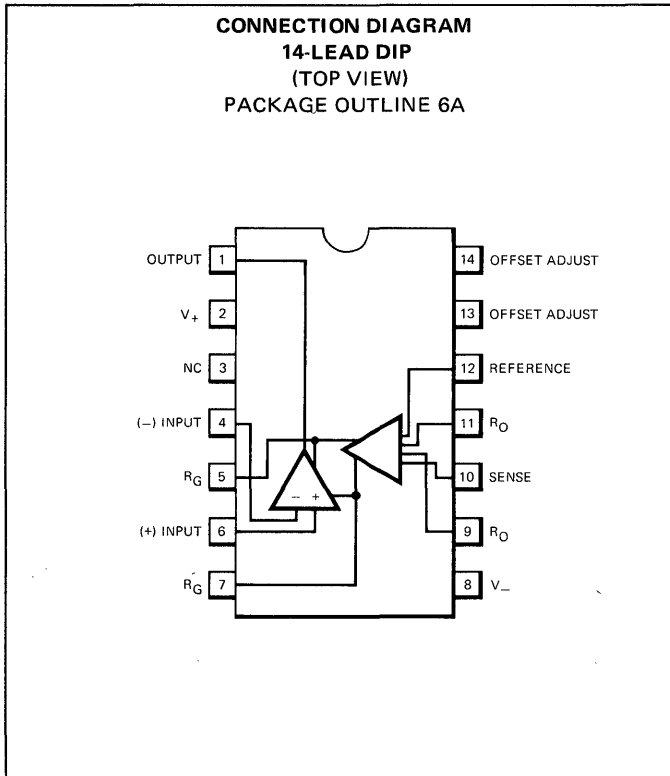
Fig. 10

μA771

INSTRUMENTATION AMPLIFIER

GENERAL DESCRIPTION — The μA771 is a true Instrumentation Amplifier with an internally closed feedback loop determining the device gain. The μA771 instrumentation amplifier is distinguished from operational amplifiers with external resistor feedback because the input terminals are totally uncommitted and need be connected only to the signal source. The μA771 also features very high input impedance, very low bias and offset currents, low offset drifts, low noise and high common mode and power supply rejection. The addition of a few external components enables the user to "add-on" a derived common mode voltage follower for driving shielded input lines, if desired. Typical applications include strain gauge, transducer and transconductance amplifiers, physiological (biomedical) probes, and thermocouple preamplifiers.

- GAIN DETERMINED BY INTERNALLY CLOSED FEEDBACK LOOP
- VERY HIGH INPUT IMPEDANCE
- LOW OFFSET DRIFTS
- LOW NOISE
- HIGH COMMON MODE AND POWER SUPPLY REJECTION
- VERY LOW BIAS AND OFFSET CURRENTS
- VERY SIMPLE GAIN SETTING AND ADJUSTMENT

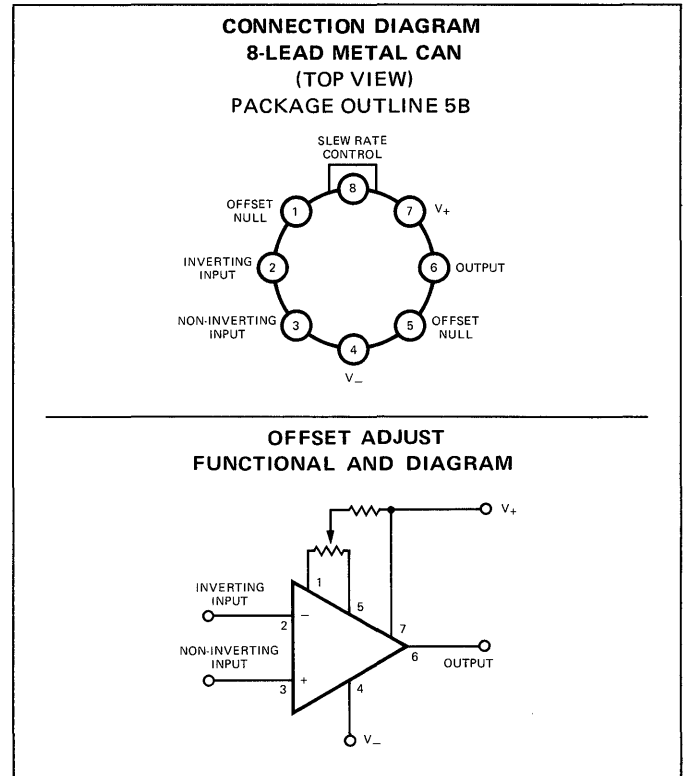


μA772

HIGH SLEW RATE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION — The μA772 is a monolithic High Slew Rate Operational Amplifier, constructed using the Fairchild Planar* epitaxial process. The μA772 features high slew rate and fast settling time, with excellent dc characteristics. Additional features such as internal compensation, offset null capability and current limiting are provided. The μA772 is ideal for use in A/D, D/A and sampled data systems, and in pulse amplifiers.

- FAST SETTLING TIME . . . 300 ns
- HIGH SLEW RATE . . . 60 V/μs
- HIGH GAIN BANDWIDTH . . . 10 MHz
- EXCELLENT INPUT CHARACTERISTICS
- CAN BE OPERATED NON-INVERTING OR INVERTING
- INTERNALLY COMPENSATED
- WIDE DIFFERENTIAL AND COMMON-MODE INPUT VOLTAGE RANGE
- WIDE SUPPLY RANGE



*Planar is a patented Fairchild process.

GLOSSARY

OPERATIONAL AMPLIFIERS

Average Temperature Coefficient of Input Offset Current — The change in input offset current over the operating temperature range divided by the operating temperature range.

Average Temperature Coefficient of Input Offset Voltage — The change in input offset voltage over the operating temperature range divided by the operating temperature range.

Bandwidth — That frequency at which the open loop voltage gain is reduced to 0.707 of its dc value.

Broadband Noise Figure — The common logarithm of the ratio of the input signal-to-noise ratio to the output signal-to-noise ratio over the frequency range for which this parameter is nominally flat.

Channel Separation — The level of output signal from an undriven amplifier with respect to the output from an adjacent driven amplifier.

Common Mode Input Resistance — The resistance seen looking into both inputs tied together.

Common Mode Output Voltage — The output voltage resulting from the application of a specified voltage common to both inputs.

Common Mode Rejection Ratio — The ratio of the change of input offset voltage to the change in common mode voltage producing it.

Common Mode Input Voltage Swing — The peak value of the common mode input voltage which can be applied for linear operation.

Differential Input Capacitance — The effective capacitance between the two inputs, operating open loop.

Differential Input Resistance — The effective resistance between the two inputs, operating open loop.

Differential Load Rejection — The ratio of the change in input offset voltage to the change in differential load current producing it.

Differential Voltage Gain — The ratio of the change in differential output voltage to the change in differential input voltage producing it.

Equivalent Input Noise Voltage — The equivalent input noise voltage which would reproduce the noise seen at the output if all amplifier noise sources and the source resistances were set to zero.

Equivalent Input Noise Current — The equivalent input noise current which would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

Input Bias Current — The average of the two input currents with no signal applied.

Input Bias Current Drift — The rate of change of input bias current with temperature, supply voltage, or time.

Input Capacitance — The capacitance seen looking into either input terminal with the other grounded.

Input Offset Current — The difference in current into the two input terminals with the output voltage at zero.

Input Offset Voltage — That voltage which must be applied between the input terminals, through two equal resistances, to obtain zero output voltage.

Input Resistance — The resistance seen looking into either input with the other grounded.

Input Voltage Range — The range of voltage on either input terminal over which the amplifier will operate as specified. Exceeding the input voltage range may cause the amplifier to function improperly.

Internal Power Dissipation — The power required to operate the amplifier with no load and no input signal.

Large Signal Voltage Gain — The ratio of the Output Voltage Swing to the change in input voltage required to produce it.

Open Loop Voltage Gain — The ratio of the output signal voltage to the differential input signal voltage producing it, with no feedback applied.

Output Resistance — The small signal ac resistance seen looking into the output with no feedback applied and the output dc voltage near zero.

Output Short-Circuit Current — The maximum output current obtainable with the output shorted to ground or to either supply.

Output Voltage Swing — The peak output voltage swing that can be obtained without clipping of the output voltage waveform.

Power Bandwidth — The maximum frequency at which the maximum output can be maintained without significant distortion.

Power Consumption — See Internal Power Dissipation.

Power Supply Current — The current required from the power supply to operate the amplifier with no load and no signal applied.

Power Supply Rejection Ratio — The ratio of the change in input offset voltage to the change in supply voltage producing it.

Power Supply Sensitivity — The ratio of the change of a specified parameter to the change in supply voltage causing it.

Settling Time — The time from a step change of input to the time the corresponding output settles to within a specified percentage of the final value.

Slew Rate — The maximum rate of change of output under large signal conditions.

Transient Response — The closed loop step function response of the circuit under small signal conditions.

Unity Gain Bandwidth — The frequency at which the open loop gain is reduced to unity.

Unity Gain Crossover Frequency — See Unity Gain Bandwidth.

LINEAR LINEAR LINEAR LINEAR LINEAR

CONTENTS AND SECTION SELECTOR

COMPARATORS	4
VOLTAGE REGULATORS	5
COMPUTER / INTERFACE	6
CONSUMER	7
TRANSISTOR / DIODE ARRAYS / ANALOG SWITCHES	8
PACKAGE OUTLINES	9
ORDER INFORMATION	10
MIL-M-38510 / MIL-STD-883	11
DICE	12
INDUSTRY CROSS REFERENCE GUIDE	13
APPLICATION INFORMATION	14

INDEX

Comparator Data Sheets are presented in alphanumeric sequence.

Selection Guide 4-3

DATA SHEETS

μ A710 High Speed Differential Comparator 4-5

μ A711 Dual Comparator 4-9

μ A734 Precision Voltage Comparator 4-13

μ A750 Dual Comparator Subsystem 4-20

μ A760 High Speed Differential Comparator 4-24

111-311 Voltage Comparator 4-29

Glossary 4-34

SELECTION GUIDE FOR MILITARY VOLTAGE COMPARATORS ⁽¹⁾

PARAMETER	UNITS	111	μ A710	μ A711	μ A734	μ A760
Input Offset Voltage, Max.	mV (2)	4.0	3.0	4.5	4.0	6.0
Temperature Coefficient of Input Offset Voltage	μ V/ $^{\circ}$ C	2.0	3.5	5.0	2.5	3.0
Input Bias Current, Max.	μ A	0.150	45	150	0.15	60
Input Offset Current, Max.	μ A	0.02	7.0	20	0.02	7.5
Supply Voltage	V	0, +5.0 to \pm 15	+12, -6.0	+12, -6.0	\pm 5.0 to \pm 15	\pm 4.5 to \pm 6.5
Response Time	ns	200	40	40	200	16
Input Voltage Range	V	\pm 14	\pm 5.0 (3)	\pm 5.0 (3)	\pm 10	\pm 4.0
Output Voltage Swing	V	N/A	-0.5 to +3.2	-0.5 to +3.2	0 to +8.0	0 to +3.0
Voltage Gain, Min.	V/mV	200 (4)	1.0	0.5	25	5.0 (4)
Power Consumption, Max.	mW	165	150	200 (5)	145	312
TTL Fanout		5.0 (Min)	1	1	2	2
Diff. Input Voltage Range	V	\pm 16	\pm 5.0	\pm 5.0	\pm 10	\pm 5.0

1. Typical values at 20 $^{\circ}$ C unless otherwise specified.
2. Maximum or minimum value for -55 $^{\circ}$ C \leq T_A \leq +125 $^{\circ}$ C.
3. V₋ = -7.0 V
4. Typical.
5. T_A = +25 $^{\circ}$ C.

SELECTION GUIDE FOR COMMERCIAL VOLTAGE COMPARATORS ⁽¹⁾

4

PARAMETER	UNITS	311	μ A710	μ A711	μ A734	μ A750	μ A760
Input Offset Voltage, Max.	mV (2)	10	5.0	5.0	7.5	20 (4) + Hyster.	6.0
Temperature Coefficient of Input Offset Voltage	μ V/ $^{\circ}$ C	6.0	5.0	5.0	3.5	100	3.0
Input Bias Current, Max.	μ A	0.3	40	150	0.15	5.0	60
Input Offset Current, Max.	μ A	0.07	7.5	25	0.045	N.A.	7.5
Supply Voltage	V	0, +5.0 to \pm 15	+12, -6.0	+12, -6.0	\pm 5.0 to \pm 15	+24	\pm 4.5 to \pm 6.5
Response Time (ns)	ns	200	40	40	200	470	16
Input Voltage Range	V	\pm 14	\pm 5.0 (3)	\pm 5.0 (3)	\pm 5.0	3 to V ₊ -2	\pm 4.0
Output Voltage Swing	V	N.A.	-0.5 to -3.2	-0.5 to +3.2	0 to +8.0	V ₊ -2	0 to \pm 3.0
Voltage Gain, Min.	V/mV	200 (4)	0.8	0.5	25	N.A.	5.0 (4)
Power Consumption, Max.	mW	205	150	230 (5)	145	150 (4)	325
TTL Fanout		5.0 (Min)	1	1	2	20	2
Diff. Input Voltage Range	V	\pm 16	\pm 5.0	\pm 5.0	\pm 10	\pm 5.0	\pm 5.0

1. Typical values at 25 $^{\circ}$ C unless otherwise specified.
2. Minimum or maximum value for 0 $^{\circ}$ C \leq T_A \leq 70 $^{\circ}$ C.
3. V₋ = -7.0 V.
4. Typical.
5. T_A = +25 $^{\circ}$ C.

μA710

HIGH SPEED DIFFERENTIAL COMPARATOR

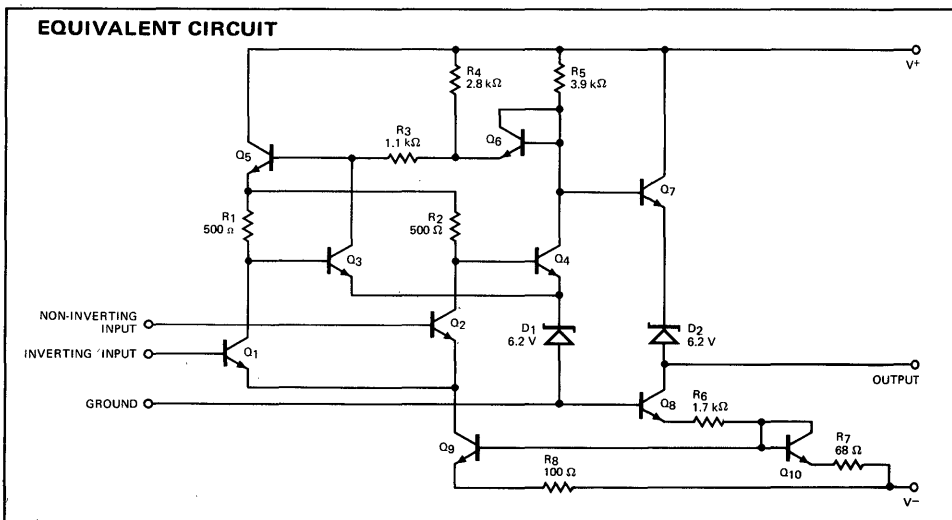
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA710 is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

- 5 mV MAXIMUM OFFSET VOLTAGE
- 5 μA MAXIMUM OFFSET CURRENT
- 1000 MINIMUM VOLTAGE GAIN
- 20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	-7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Storage Temperature Range	
Metal Can, DIP, and Flatpak	-65° C to +150° C
Operating Temperature Range	
Military (710)	-55° C to +125° C
Commercial (710C)	0° C to + 70° C
Lead Temperature	
Metal Can, DIP and Flatpak (Soldering, 60 seconds)	300° C

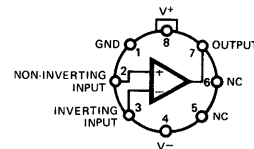


Notes on following pages.

CONNECTION DIAGRAMS

8-LEAD METAL CAN (TOP VIEW)

PACKAGE OUTLINE 5B



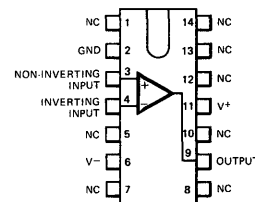
NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
710	710HM
710C	710HC

14-LEAD DIP (TOP VIEW)

PACKAGE OUTLINE 6A

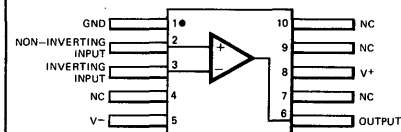


ORDER INFORMATION

TYPE	PART NO.
710	710DM
710C	710DC

10-LEAD FLATPAK (TOP VIEW)

PACKAGE OUTLINE 3F



ORDER INFORMATION

TYPE	PART NO.
710	710FM

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A710

710

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_+ = 12.0\text{ V}$, $V_- = -6.0\text{ V}$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 0$	2.0	2.5		mA
Response Time (Note 3)			40		ns

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$:

Input Offset Voltage	$R_S \leq 200\ \Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25^\circ\text{C}$ to $T_A = +125^\circ\text{C}$		3.5	10	$\mu\text{V}/^\circ\text{C}$
	$R_S = 50\ \Omega$, $T_A = 25^\circ\text{C}$ to $T_A = -55^\circ\text{C}$		2.7	10	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$T_A = +125^\circ\text{C}$		0.25	3.0	μA
	$T_A = -55^\circ\text{C}$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25^\circ\text{C}$ to $T_A = +125^\circ\text{C}$		5.0	25	nA/ $^\circ\text{C}$
	$T_A = 25^\circ\text{C}$ to $T_A = -55^\circ\text{C}$		15	75	nA/ $^\circ\text{C}$
Input Bias Current	$T_A = -55^\circ\text{C}$		27	45	μA
Input Voltage Range	$V_- = -7.0\text{ V}$	± 5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	80	100		dB
Differential Input Voltage Range		± 5.0			V
Voltage Gain		1000			
Output HIGH Voltage	$\Delta V_{IN} \geq 5\text{ mV}$, $0 \leq I_{OUT} \leq 5.0\text{ mA}$	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5\text{ mV}$	-1.0	-0.5	0	V
Output Sink Current	$T_A = +125^\circ\text{C}$, $\Delta V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 0$	0.5	1.7		mA
	$T_A = -55^\circ\text{C}$, $\Delta V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	$V_{OUT} = \text{Gnd}$, Inverting Input = +5mV.		4.6	7.0	mA
Power Consumption	$V_{OUT} = \text{Gnd}$, Inverting Input = +10mV.		90	150	mW

710C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_+ = 12.0\text{ V}$, $V_- = -6.0\text{ V}$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns

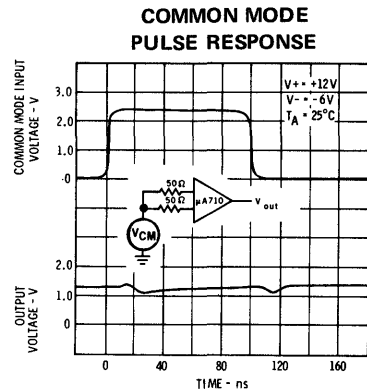
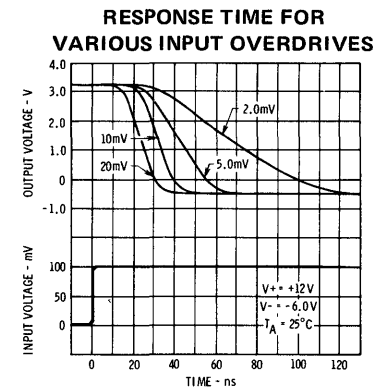
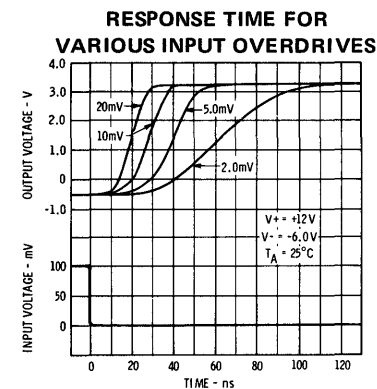
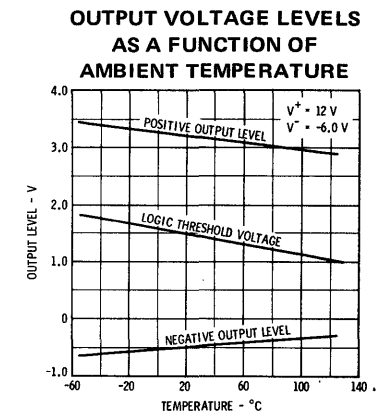
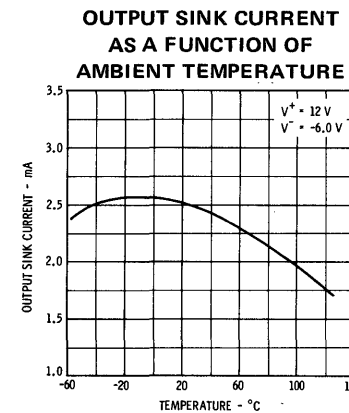
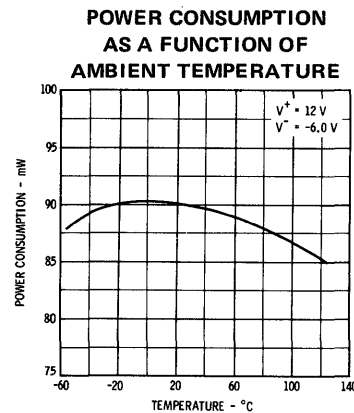
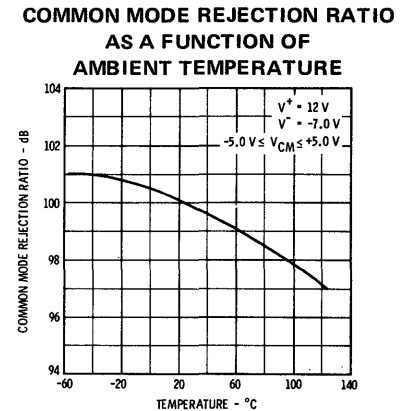
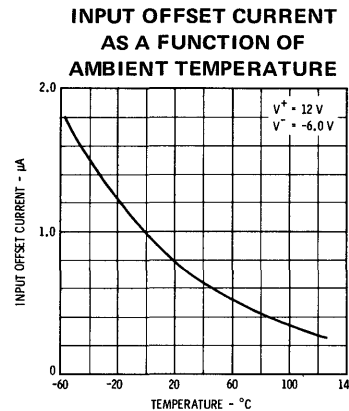
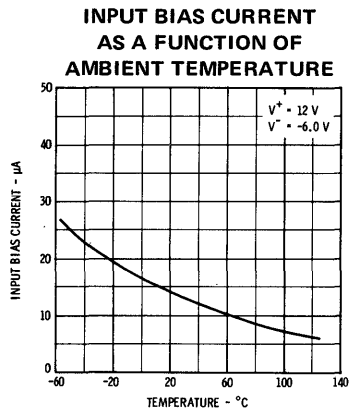
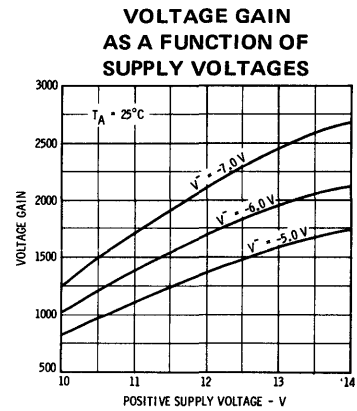
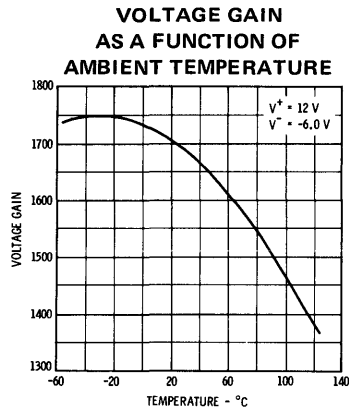
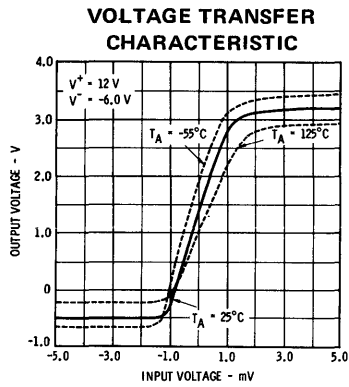
The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$:

Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0^\circ\text{C}$ to $T_A = +70^\circ\text{C}$		5.0	20	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25^\circ\text{C}$ to $T_A = +70^\circ\text{C}$		15	50	nA/ $^\circ\text{C}$
	$T_A = 25^\circ\text{C}$ to $T_A = 0^\circ\text{C}$		24	100	nA/ $^\circ\text{C}$
Input Bias Current	$T_A = 0^\circ\text{C}$		25	40	μA
Input Voltage Range	$V_- = -7.0\text{ V}$	± 5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	70	98		dB
Differential Input Voltage Range		± 5.0			V
Voltage Gain		800			
Output HIGH Voltage	$\Delta V_{IN} \geq 5\text{ mV}$, $0 \leq I_{OUT} \leq 5.0\text{ mA}$	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5\text{ mV}$	-1.0	-0.5	0	V
Output Sink Current	$\Delta V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 0$	0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	$V_{OUT} = \text{Gnd}$, Inverting Input = +5mV.		4.6	7.0	mA
Power Consumption	$V_{OUT} = \text{Gnd}$, Inverting Input = +10mV.		90	150	mW

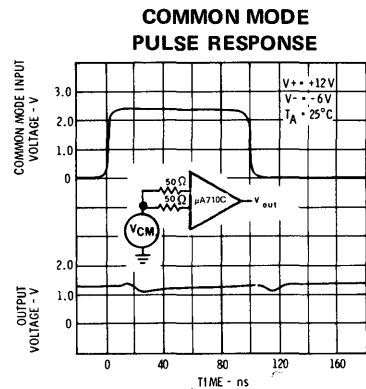
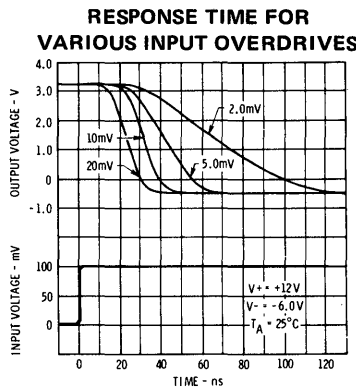
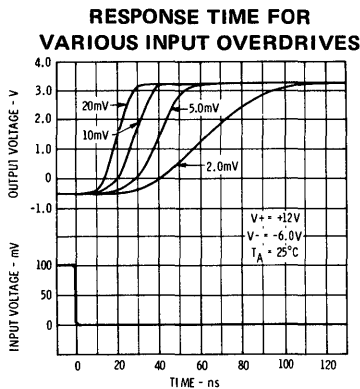
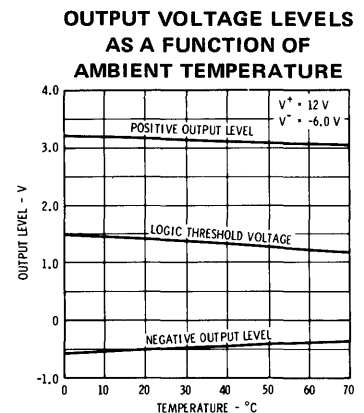
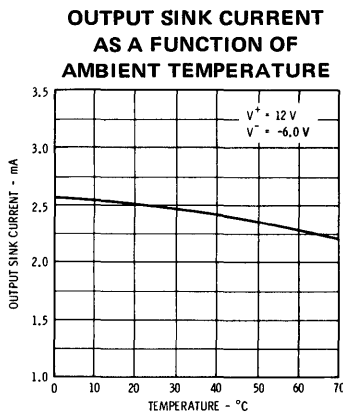
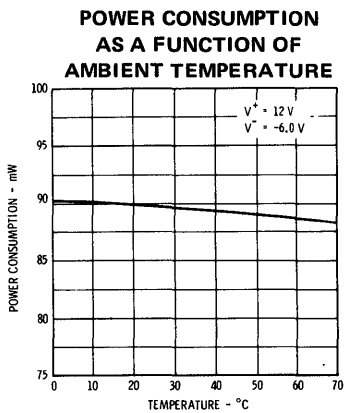
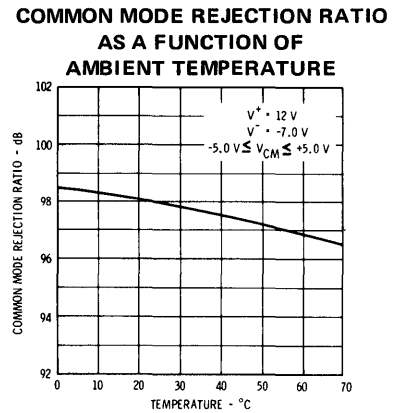
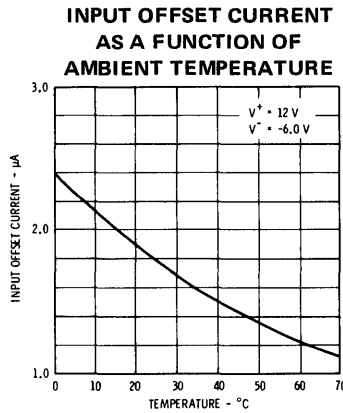
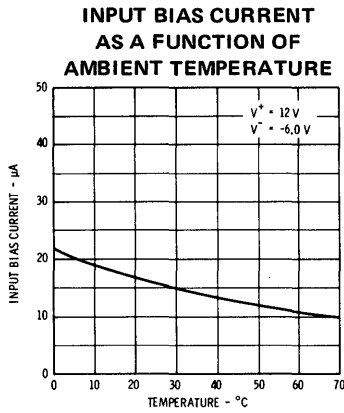
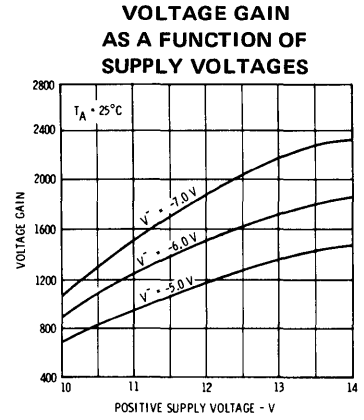
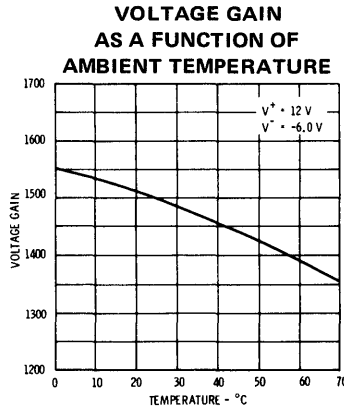
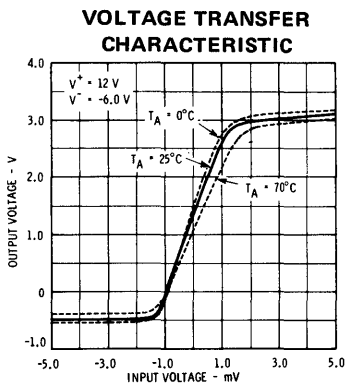
NOTES:

- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3\text{ mW}/^\circ\text{C}$ for Metal Can, $8.3\text{ mW}/^\circ\text{C}$ for DIP, and $7.1\text{ mW}/^\circ\text{C}$ for the Flatpak.
- The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage as follows: For 710, 1.8 V at -55°C , 1.4 V at $+25^\circ\text{C}$, 1.0 V at $+125^\circ\text{C}$. For 710C, 1.5 V at 0°C , 1.4 V at $+25^\circ\text{C}$, and 1.2 V at $+70^\circ\text{C}$.
- The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL PERFORMANCE CURVES FOR 710



TYPICAL PERFORMANCE CURVES FOR 710C



μA711

DUAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

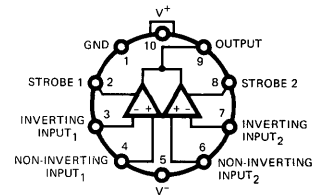
GENERAL DESCRIPTION — The μA711 is a Dual, Differential Voltage Comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-Go testing equipment. The μA711, which is similar to the μA710 differential comparator, is constructed using the Fairchild Planar* epitaxial process.

- **FAST RESPONSE TIME . . . 40 ns TYPICAL**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **10μA MAXIMUM OFFSET CURRENT**
- **INDEPENDENT STROBING OF EACH COMPARATOR**

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14 V
Negative Supply Voltage	-7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (711)	-55°C to +125°C
Commercial (711C)	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
Metal Can, DIP and Flatpak (Soldering, 60 seconds)	300°C

CONNECTION DIAGRAMS
10-LEAD METAL CAN
 (TOP VIEW)
PACKAGE OUTLINE 5F

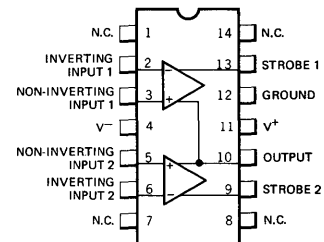


Note: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
711	711HM
711C	711HC

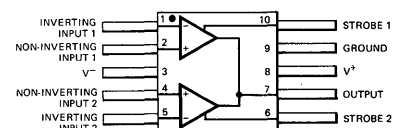
14-LEAD DIP
 (TOP VIEW)
PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
711	711DM
711C	711DC

10-LEAD FLATPAK
 (TOP VIEW)
PACKAGE OUTLINE 3F

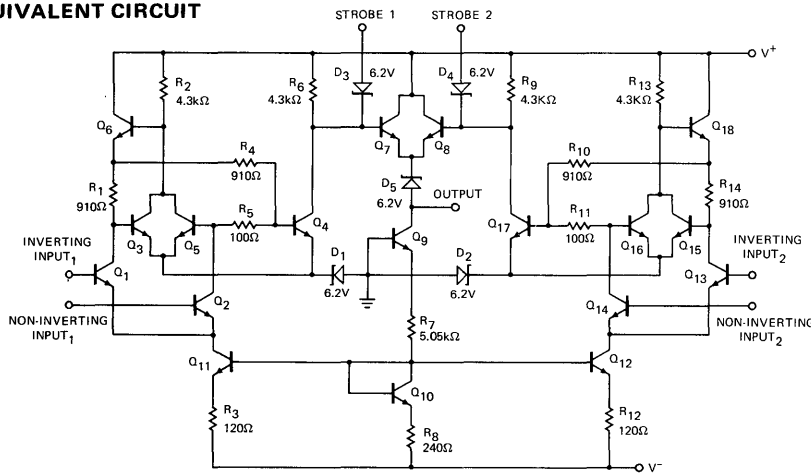


ORDER INFORMATION

TYPE	PART NO.
711	711FM

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



Notes on following page.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A711

711

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V^+ = 12\text{ V}$, $V^- = -6.0\text{ V}$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$V_{OUT} = +1.4\text{ V}$, $R_S \leq 200\ \Omega$, $V_{CM} = 0$		1.0	3.5	mV
	$V_{OUT} = +1.4\text{ V}$, $R_S \leq 200\ \Omega$		1.0	5.0	mV
Input Offset Current	$V_{OUT} = 1.4\text{ V}$		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0\text{ V}$	± 5.0			V
Differential Input Voltage Range		± 5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	$V_{IN} \geq 10\text{ mV}$		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq 10\text{ mV}$, $I_O = 5\text{ mA}$	2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq 10\text{ mV}$	-1.0	-0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3\text{ V}$	-1.0		0	V
Output Sink Current	$V_{IN} \geq 10\text{ mV}$, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 100\text{ mV}$		1.2	2.5	mA
Positive Supply Current	$V_{OUT} = \text{Gnd}$, Inverting Input = +5mV		8.6		mA
Negative Supply Current	$V_{OUT} = \text{Gnd}$, Inverting Input = +5mV		3.9		mA
Power Consumption			130	200	mW

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$:

Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\ \Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		$\mu\text{V}/^\circ\text{C}$
Voltage Gain		500			

NOTES:

- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3\text{ mW}/^\circ\text{C}$ for the Metal Can, $8.3\text{ mW}/^\circ\text{C}$ for the DIP, and $7.1\text{ mW}/^\circ\text{C}$ for the Flatpak.
- The response time specified (see definitions) is for a 100 mV step input with 5 mV overdrive.
- The input offset voltage is specified for a logic threshold as follows:
 711: 1.8 V at -55°C , 1.4 V at $+25^\circ\text{C}$, 1.0 V at $+125^\circ\text{C}$
 711C: 1.5 V at 0°C , 1.4 V at $+25^\circ\text{C}$, 1.2 V at $+70^\circ\text{C}$

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A711

711C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V^+ = 12\text{V}$, $V^- = -6.0\text{V}$ unless otherwise specified)

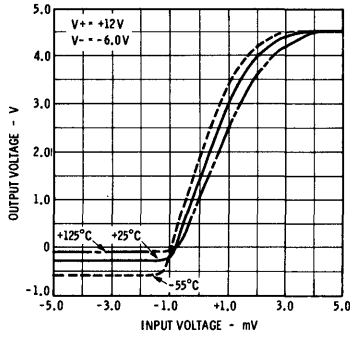
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$V_{OUT} = +1.4\text{V}$, $R_S \leq 200\ \Omega$, $V_{CM} = 0$		1.0	5.0	mV
	$V_{OUT} = +1.4\text{V}$, $R_S \leq 200\ \Omega$		1.0	7.5	mV
Input Offset Current	$V_{OUT} = +1.4\text{V}$		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0\text{V}$	± 5.0			V
Differential Input Voltage Range		± 5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	$V_{IN} \geq 10\text{mV}$		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq 10\text{mV}$, $I_O = 5\text{mA}$	2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq 10\text{mV}$	-1.0	-0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3\text{V}$	-1.0		0	V
Output Sink Current	$V_{IN} \geq 10\text{mV}$, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 100\text{mV}$		1.2	2.5	mA
Positive Supply Current	$V_{OUT}\text{Gnd}$, Inverting Input = +10mV.		8.6		mA
Negative Supply Current	$V_{OUT}\text{Gnd}$, Inverting Input = +10mV.		3.9		mA
Power Consumption			130	230	mW

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$:

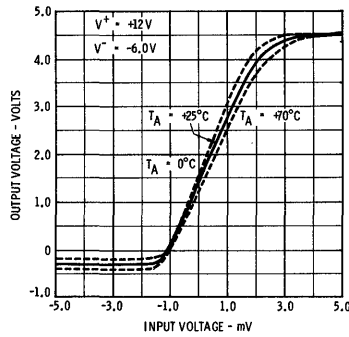
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, $V_{CM} = 0$			6.0	mV
	$R_S \leq 200\ \Omega$			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		$\mu\text{V}/^\circ\text{C}$
Voltage Gain		500			

TYPICAL PERFORMANCE CURVES FOR 711 AND 711C

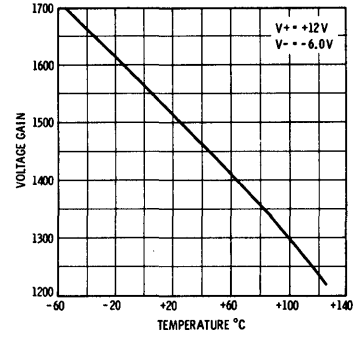
VOLTAGE TRANSFER CHARACTERISTIC
711



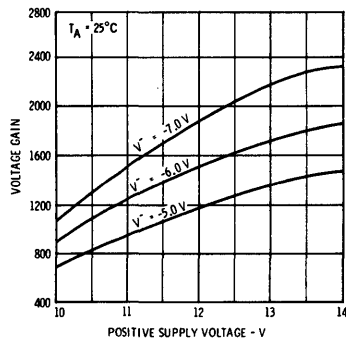
VOLTAGE TRANSFER CHARACTERISTIC
711C



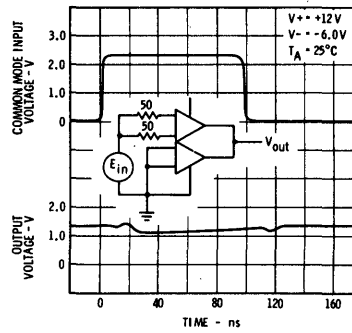
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



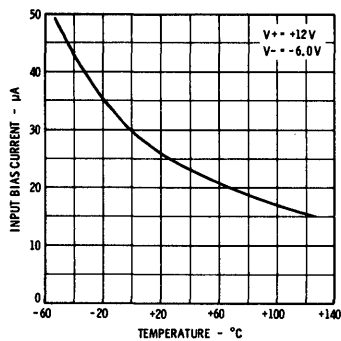
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



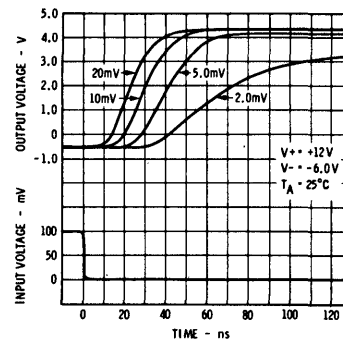
COMMON MODE PULSE RESPONSE



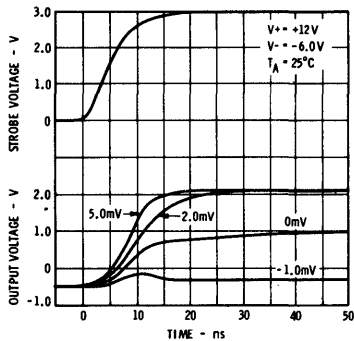
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



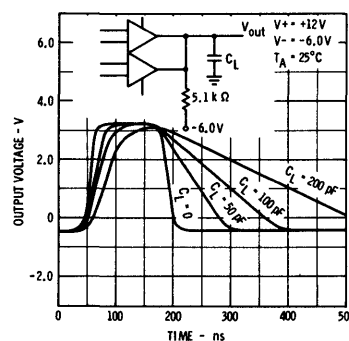
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



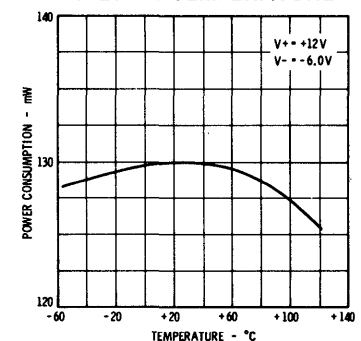
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



μA734

PRECISION VOLTAGE COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA734 is a Precision Voltage Comparator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is specifically designed for high accuracy level sensing and measuring applications. The μA734 is extremely useful for analog-to-digital converters with twelve bit accuracies and one mega-bit conversion rates. Maximum resolution is obtained by high gain, low input offset current, and low input offset voltage. Its superior temperature stability can be improved by offset nulling which further reduces offset voltage drift. Balanced or unbalanced supply operation and standard TTL logic compatibility enhance the μA734's versatility.

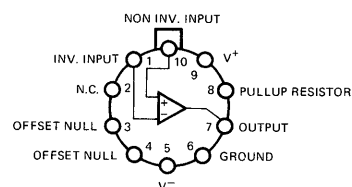
- **CONSTANT INPUT IMPEDANCE OVER DIFFERENTIAL INPUT RANGE**
- **HIGH INPUT IMPEDANCE . . . 55 MΩ**
- **LOW DRIFT . . . 3.5 μV/°C**
- **HIGH GAIN . . . 60 k**
- **BALANCED OFFSET NULL CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE . . . ±5 V to ±18 V**
- **TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Peak Output Current	10 mA
Differential Input Voltage	±10 V
Input Voltage Range (Note 1)	±13 V
Voltage Between Offset Null and V ⁻	±0.5 V
Internal Power Dissipation (Note 2)	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	
Military (734)	-55° C to +125° C
Commercial (734C)	0° C to +70° C
Storage Temperature Range	
Metal Can, DIP	-65° C to +150° C
Lead Temperature (Soldering, 60 Seconds Max.)	300° C

CONNECTION DIAGRAMS

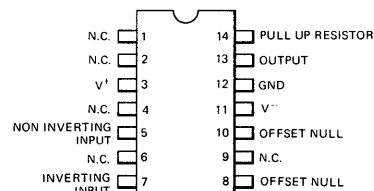
**10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F**



ORDER INFORMATION

TYPE	PART NO.
734	734HM
734C	734HC

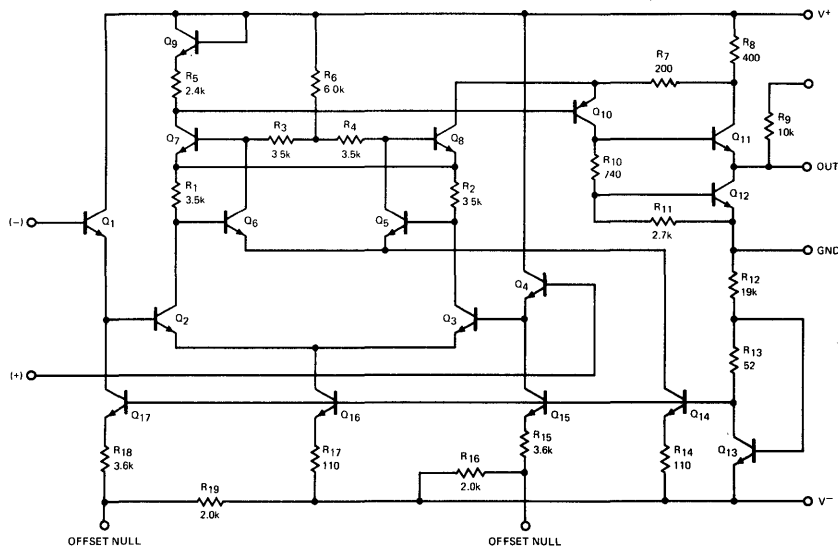
**14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A**



ORDER INFORMATION

TYPE	PART NO.
734	734DM
734C	734DC

EQUIVALENT CIRCUIT



Notes on following pages.

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A734

± 15 VOLT OPERATION FOR 734C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Pin 8 tied to +15 V, unless otherwise specified) Note 3.

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\text{ k}\Omega$		1.1	5.0	mV
Input Offset Current			3.5	25	nA
Input Bias Current			30	100	nA
Input Resistance		7.0	55		M Ω
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	$R_L = 1.5\text{ k}\Omega$ to +5.0 V	35 k	60 k		V/V
Positive Supply Current – Output LOW			4.0	5.0	mA
Negative Supply Current – Output LOW			1.5	2.0	mA
Power Consumption – Output LOW			82	105	mW
Transient Response	$R_L = 1.5\text{ k}\Omega$ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$

Input Offset Voltage	$R_S \leq 50\text{ k}\Omega$		1.2	7.5	mV
Input Offset Current			4.0	45	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50\ \Omega$		3.5	20	$\mu\text{V}/^\circ\text{C}$
Average Input Offset Current Drift	$T_A = +25^\circ\text{C}$ to $+70^\circ\text{C}$		0.02	0.3	nA/ $^\circ\text{C}$
	$T_A = +25^\circ\text{C}$ to 0°C		0.05	0.75	nA/ $^\circ\text{C}$
Input Bias Current				150	nA
Large Signal Voltage Gain	$R_L = 1.5\text{ k}\Omega$ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		± 10			V
Differential Input Voltage Range		± 10			V
Common Mode Rejection Ratio	$R_S \leq 50\text{ k}\Omega$	70	100		dB
Supply Voltage Rejection Ratio $V_S = \pm 5\text{ V}$ to $\pm 18\text{ V}$	$R_S \leq 50\text{ k}\Omega$		6.0	100	$\mu\text{V}/\text{V}$
Output HIGH Voltage	$I_O = 0.080\text{ mA}$	7.0			V
	$I_O = 0.080\text{ mA}$, $V_g = +5.0\text{ V}$	2.4		5.0	V
Output LOW Voltage	$I_{\text{SINK}} = 3.2\text{ mA}$			0.4	V
Positive Supply Current – Output LOW				7.0	mA
Negative Supply Current – Output LOW				2.5	mA
Power Dissipation – Output LOW				145	mW

FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A734$

± 15 VOLT OPERATION FOR 734

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Pin 8 tied to +15 V, unless otherwise specified) Note 3.

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\text{ k}\Omega$		0.9	3.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			28	50	nA
Input Resistance		20	60		$M\Omega$
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	$R_L = 1.5\text{ k}\Omega$ to +5.0 V	35 k	70 k		V/V
Positive Supply Current – Output LOW			4.0	5.0	mA
Negative Supply Current – Output LOW			1.5	2.0	mA
Power Consumption – Output LOW			82	105	mW
Transient Response	$R_L = 1.5\text{ k}\Omega$ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

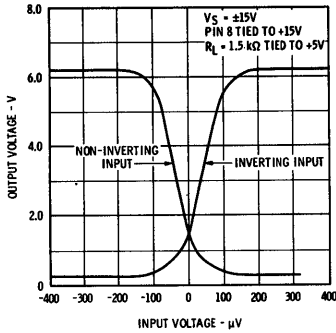
Input Offset Voltage	$R_S \leq 50\text{ k}\Omega$		1.1	4.0	mV
Input Offset Current			3.0	20	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50\text{ k}\Omega$		2.5	15	$\mu\text{V}/^\circ\text{C}$
Average Input Offset Current Drift	$T_A = +25^\circ\text{C}$ to $+125^\circ\text{C}$ $T_A = +25^\circ\text{C}$ to -55°C		0.01 0.05	0.1 0.4	nA/ $^\circ\text{C}$ nA/ $^\circ\text{C}$
Input Bias Current				150	nA
Large Signal Voltage Gain	$R_L = 1.5\text{ k}\Omega$ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		± 10			V
Differential Input Voltage Range		± 10			V
Common Mode Rejection Ratio	$R_S \leq 50\text{ k}\Omega$	70	100		dB
Supply Voltage Rejection Ratio $V_S = \pm 5\text{ V}$ to $\pm 18\text{ V}$	$R_S \leq 50\text{ k}\Omega$		5.0	100	$\mu\text{V}/\text{V}$
Output HIGH Voltage	$I_O = 0.080\text{ mA}$ $I_O = 0.080\text{ mA}, V_G = +5.0\text{ V}$	7.0 2.4		5.0	V V
Output LOW Voltage	$I_{\text{SINK}} = 3.2\text{ mA}$			0.4	V
Positive Supply Current – Output LOW				7.0	mA
Negative Supply Current – Output LOW				2.5	mA
Power Dissipation – Output LOW				145	mW

NOTES:

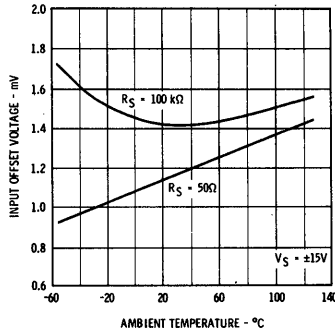
- Rating applies for $\pm 15\text{ V}$ supplies. For other supply voltages the rating is within 2 V of either supply.
- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3\text{ mW}/^\circ\text{C}$ for Metal Can, $8.3\text{ mW}/^\circ\text{C}$ for DIP.
- Pin numbers refer to Metal Can package.

TYPICAL PERFORMANCE CURVES FOR 734 AND 734C (Note 2)

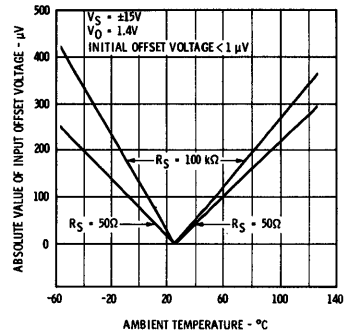
TRANSFER CHARACTERISTICS



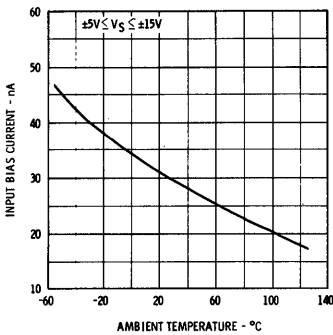
UN-NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



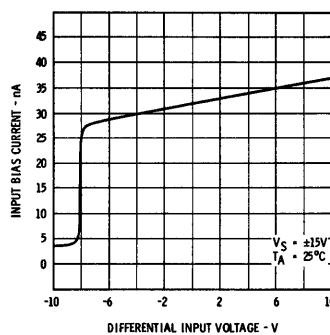
INPUT OFFSET VOLTAGE CHANGE AS A FUNCTION OF AMBIENT TEMPERATURE - NULLED TO ZERO AT 25 $^{\circ}C$



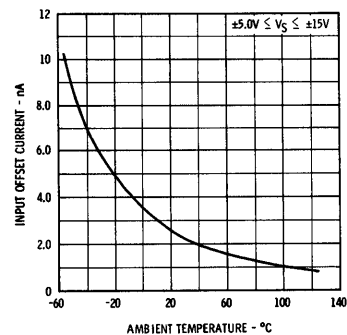
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



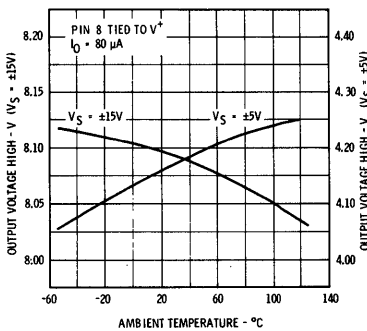
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



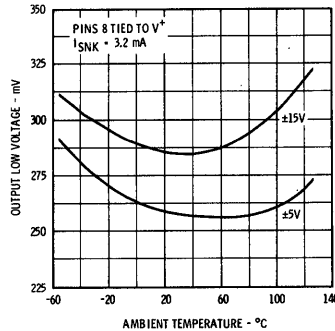
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



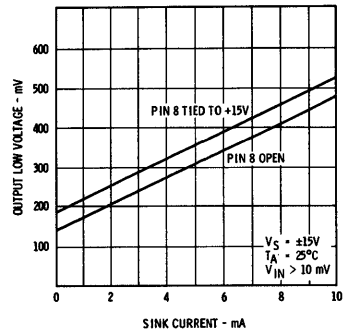
OUTPUT HIGH VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



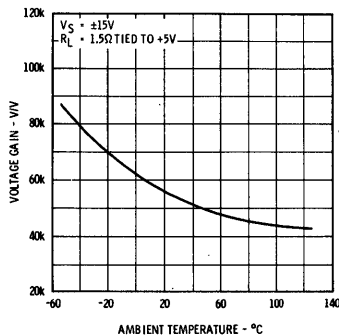
OUTPUT LOW VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



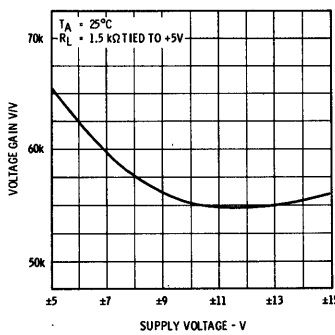
OUTPUT VOLTAGE LOW VS SINK CURRENT



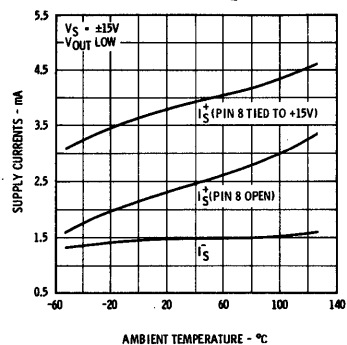
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

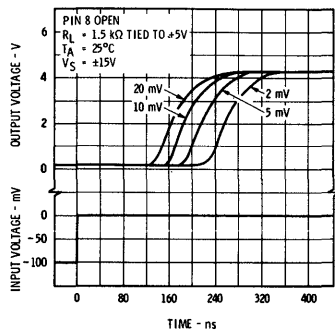


POSITIVE AND NEGATIVE SUPPLY CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE

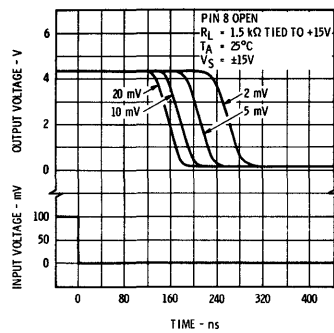


TYPICAL PERFORMANCE CURVES FOR 734 AND 734C (Note 2)

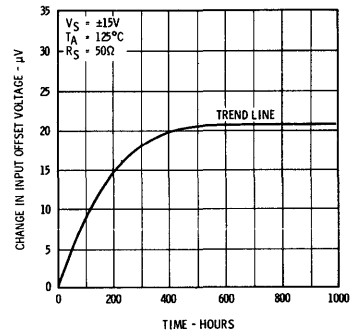
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



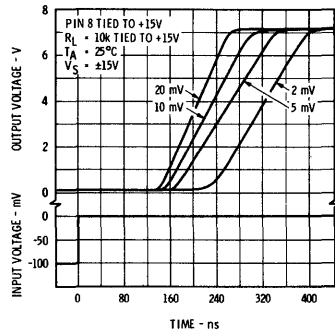
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



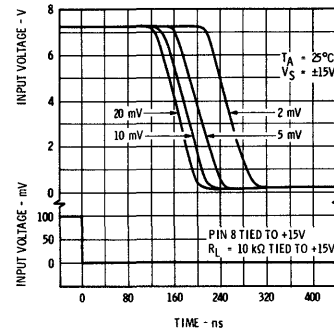
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



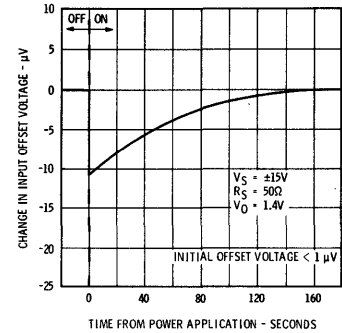
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



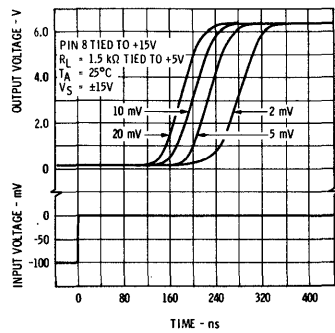
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



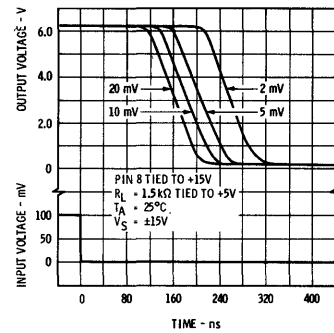
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



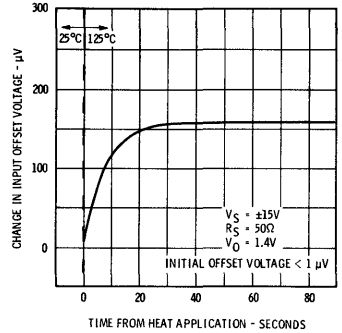
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



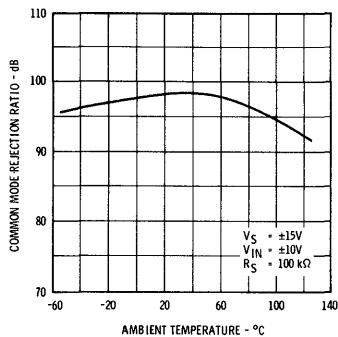
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



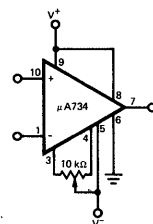
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



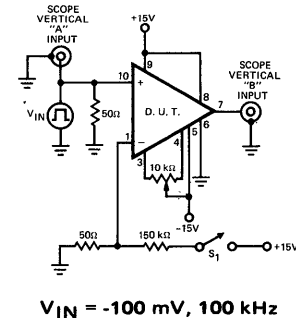
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



OFFSET NULL CIRCUIT (NOTE 2)

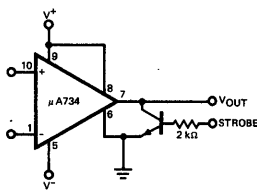


AC TEST CIRCUIT (NOTE 2)

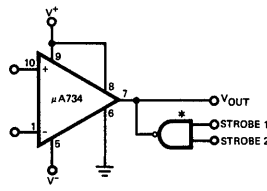


TYPICAL APPLICATIONS (Note 2)

STROBE CIRCUITRY

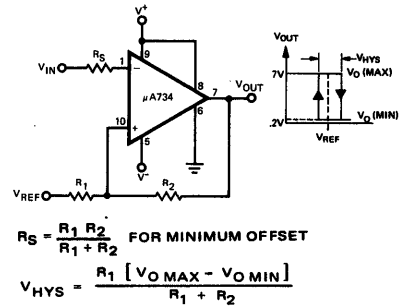


ALTERNATE STROBE CIRCUITRY



* 1/2 9944

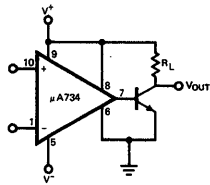
LEVEL DETECTOR WITH HYSTERESIS



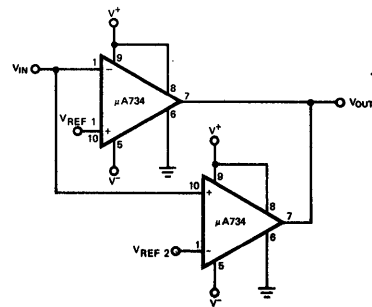
$$R_S = \frac{R_1 R_2}{R_1 + R_2} \text{ FOR MINIMUM OFFSET}$$

$$V_{HYS} = \frac{R_1 [V_{O \text{ MAX}} - V_{O \text{ MIN}}]}{R_1 + R_2}$$

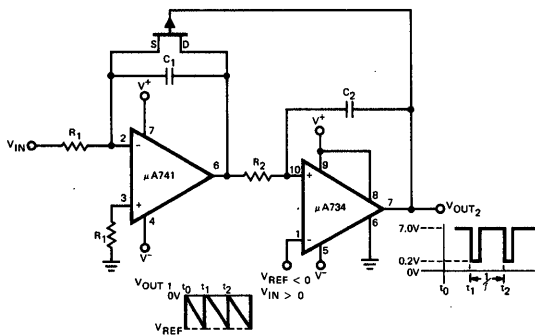
HIGH POWER OUTPUT CIRCUITS



PRECISION DUAL LIMIT GO-NO GO TESTER

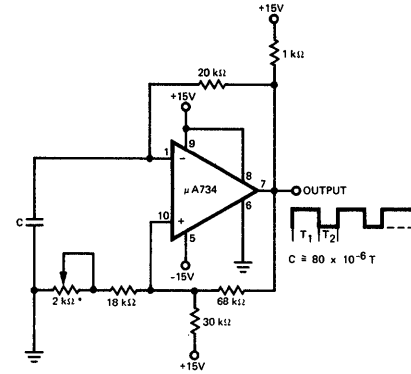


VOLTAGE CONTROLLED OSCILLATOR



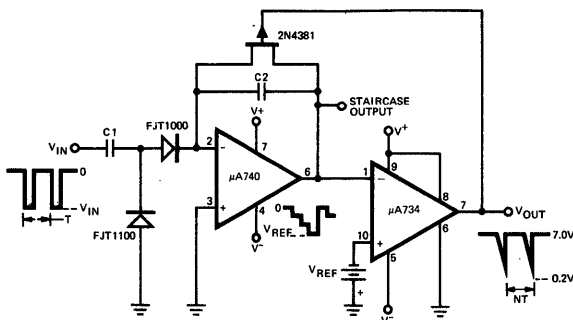
$$f = \frac{V_{IN}}{|V_{REF}| R_1 C_1} \quad R_2 C_2 > \frac{|V_{REF}| C_1}{I_{DSS}}$$

FREE RUNNING OSCILLATOR



• Adjusts $\frac{T_1}{T_2}$

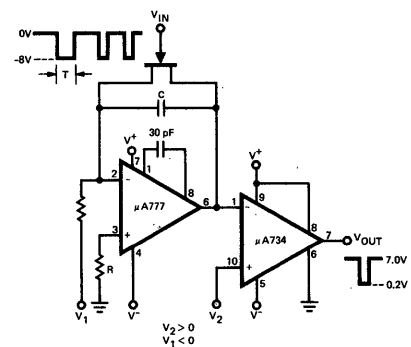
FREQUENCY DIVIDER & STAIRCASE GENERATOR



$$|V_{REF}| = 2V_D + N \left[3.5T + 2V_D - \frac{C_1 V_{IN}}{C_2} \right]$$

T In Seconds
 V_D for FJT 1000 $\approx 0.31V$

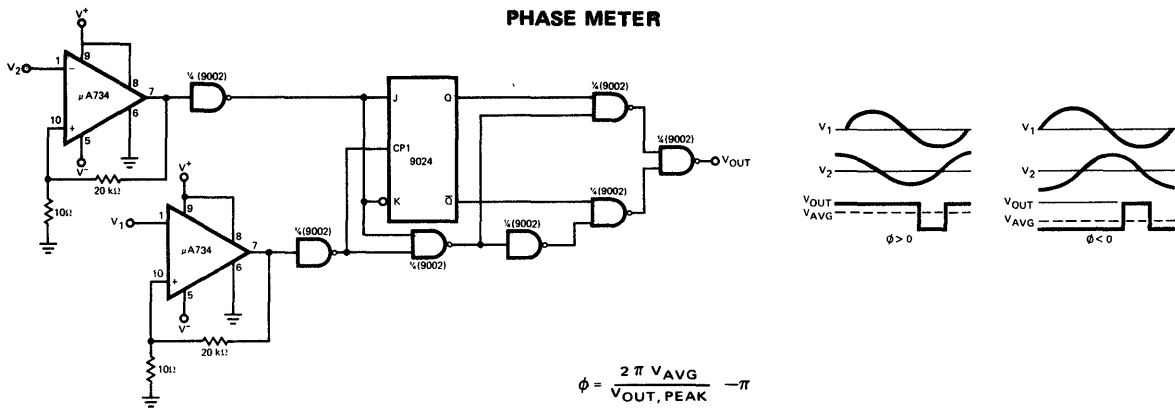
PULSE WIDTH DISCRIMINATOR



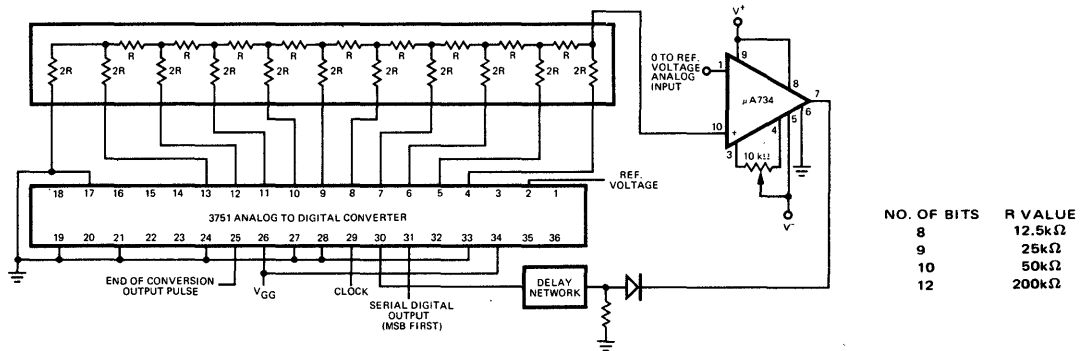
VOUT Pulse Appears

$$\text{Whenever } T > \frac{R C V_2}{|V_1|}$$

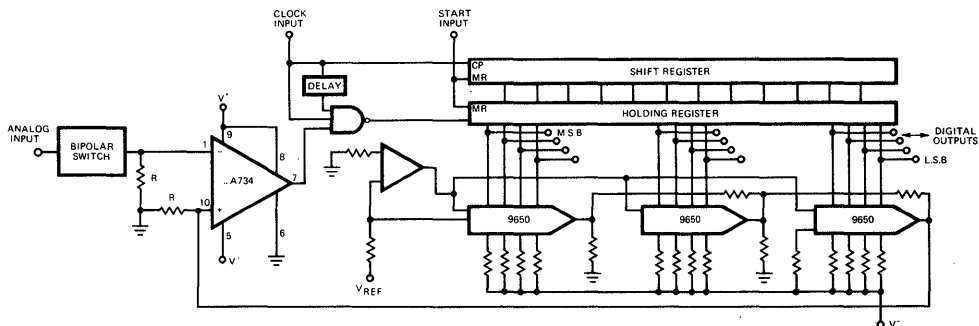
TYPICAL APPLICATIONS (Noté 2)



12-BIT A/D CONVERTER



12-BIT A/D CONVERTER



μA750

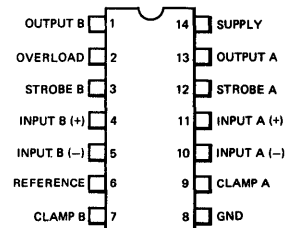
DUAL COMPARATOR SUBSYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA750 is a Dual Comparator Subsystem consisting of two independent high current comparators with input inhibit capability. A voltage reference is included in the μA750. The device is protected against short circuits and thermal overloads. Positive switching is insured by built-in hysteresis. Hysteresis expansion is available for operation in noisy environments. These advantages make the μA750 ideally suited for a wide variety of applications including environment and process systems. It is also recommended for use as a comparator for driving relays or indicator lamps.

- HIGH OUTPUT CURRENT CAPABILITY . . . 250 mA
- THERMAL AND SHORT CIRCUIT CURRENT PROTECTION
- SUBSYSTEM VOLTAGE REFERENCE
- POSITIVE SWITCHING BY MEANS OF BUILT-IN HYSTERESIS
- OUTPUT CURRENT SINKING CAPABILITY IN ADDITION TO HIGH CURRENT SOURCE
- COMPLETELY INDEPENDENT COMPARATORS
- INDEPENDENT INPUT INHIBIT CAPABILITY
- WIDE POWER SUPPLY RANGE . . . +11 V to +26 V

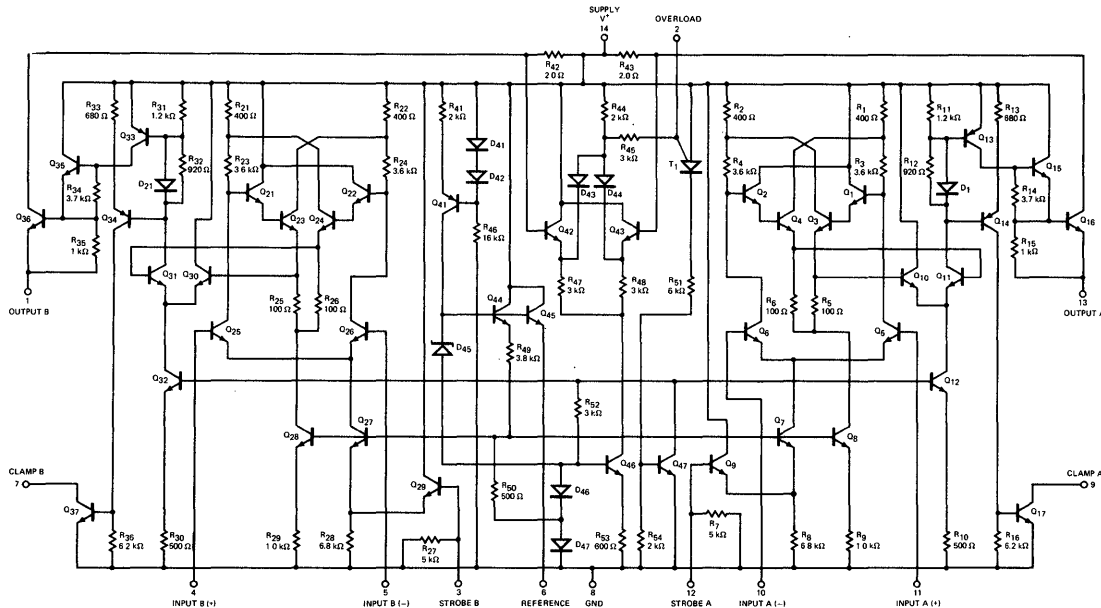
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
750C	750DC

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	26 V
Voltage Between Input Pins	± 5 V
Input Voltage Range	0 V to Supply Voltage
Voltage Range at Output Terminal (Output Off)	-5 V to Supply Voltage
Voltage at Clamp Terminal (Clamp Off)	30 V
Output Current Per Side (Note 1)	250 mA
Reference Output Current	30 mA
Clamp Sinking Current Per Side	30 mA
Power Dissipation (Note 2)	670 mW
Voltage at Strobe Input Terminal	+6 V
Current Out of Overload Terminal	10 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

ELECTRICAL CHARACTERISTICS: 750C

Each Comparator ($T_A = 25^\circ\text{C}$, $V^+ = 24\text{ V}$, $V_{\text{STROBE}} = 0$, $V_{\text{IN}(+)}$ and $V_{\text{IN}(-)}$ as defined in Figure 1, $I_{\text{REF}} = 0$, $I_{\text{CLAMP}} = 0$, $R_L = 1\text{ k}\Omega$, (Notes 3, 4) Test Circuit 1, unless otherwise specified).

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC CHARACTERISTICS:					
Positive Threshold Voltage ($V_{\text{THRESH}(+)}$)	(See Figure 1)		9.0		mV
Negative Threshold Voltage ($V_{\text{THRESH}(-)}$)	(See Figure 1)		9.0		mV
Hysteresis Voltage (V_{HYST})	(See Figure 1)		18		mV
Offset Voltage (V_{OFFSET})	(See Figure 1)		0.5		mV
Continuous Available Output Current	Device "ON" (See Figure 1)		220		mA
Total Input Bias Current			1.5		μ A
Output Voltage Below Supply Voltage	$T_J = 25^\circ\text{C}$, $I_{\text{OUT}} = 150\text{ mA}$ Device "ON" (See Figure 1)		1.7	2.1	V
Output Leakage Current	Device "OFF" (See Figure 1)			100	μ A
Clamp Saturation Voltage	Device "ON" (See Figure 1) $I_{\text{CLAMP}} = 25\text{ mA}$		0.4	0.8	V
Clamp ON Resistance			15		Ω
Strobe Activation Voltage		1.1	1.6	2.3	V
Strobe Input Resistance			5.0		k Ω
Reference Voltage	$I_{\text{REF}} = 10\text{ mA}$	7.0	7.8	8.4	V
Supply Current (Pin 14)	Device "ON", $I_{\text{OUT}} = 0$		12	18	mA
Shutdown Threshold Voltage at OVERLOAD Terminal (measured as voltage below supply voltage) (Note 4)			0.7		V
The following specifications apply for $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$					
Positive Threshold Voltage ($V_{\text{THRESH}(+)}$)	(See Figure 1)	6.0		14	mV
Negative Threshold Voltage ($V_{\text{THRESH}(-)}$)	(See Figure 1)	6.0		14	mV
Hysteresis Voltage (V_{HYST})	(See Figure 1)	12		28	mV
Offset Voltage (V_{OFFSET})	(See Figure 1)			6.0	mV
Continuous Available Output Current	Device "ON" (See Figure 1)	125			mA
Total Input Bias Current				5.0	μ A

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$, $R_L = 220\ \Omega$, $R_{\text{CLAMP}} = 2.4\text{ k}\Omega$

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time (t_r)	(See Figure 2)		55		ns
Output Fall time (t_f)	(See Figure 2)		150		ns
Turn ON Propagation Delay, Input to Output (t_{PLH})	(See Figure 2)		95		ns
Turn OFF Propagation Delay, Input to Output (t_{PHL})	(See Figure 2)		470		ns
Turn ON Strobe Release Time ($t_{\text{sr}+}$)	(See Figure 3)		115		ns
Turn OFF Strobe Release Time ($t_{\text{sr}-}$)	(See Figure 3)		525		ns

NOTES:

- Rating applies when OVERLOAD terminal is used to modify or defeat internal overload protection circuitry.
- Rating applies when used without heatsink. Junction temperature T_J must not exceed 150°C . $T_J = T_A + R_{\text{th}} \times P_{\text{DISS}}$, where $R_{\text{th}} \approx 120^\circ\text{C/W}$ is the typical thermal resistance (junction to ambient) for the package without heatsink and P_{DISS} is the power dissipation in the package.
- At least one input pin of an unused comparator section should be connected to a positive voltage between +3 V and ($V^+ - 2\text{ V}$) e.g., reference output pin (Pin 6).
- Under overload conditions the device will shut off the output sections. Resetting can be accomplished by temporarily interrupting the supply current after the overload conditions have been removed. An R-C network between the supply and overload terminal can be used to decrease the sensitivity of the overload protection network.

HYSTERESIS DEFINITIONS

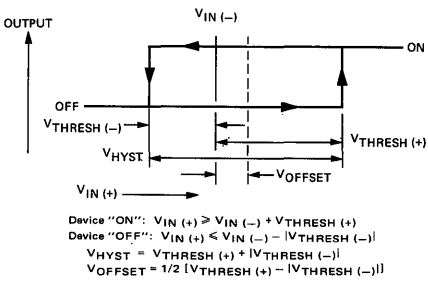


Fig. 1

SWITCHING TIMES

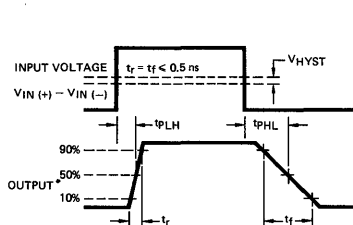


Fig. 2

STROBE RELEASE TIMES

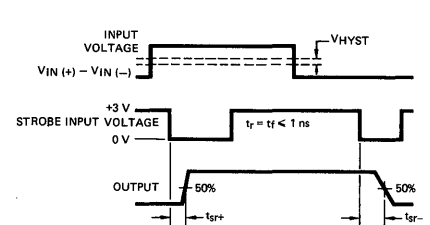
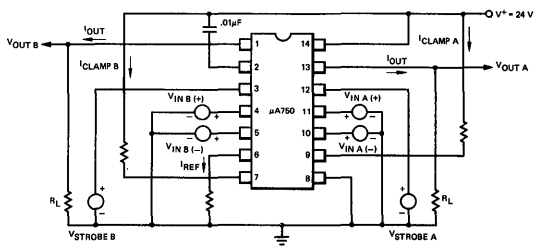
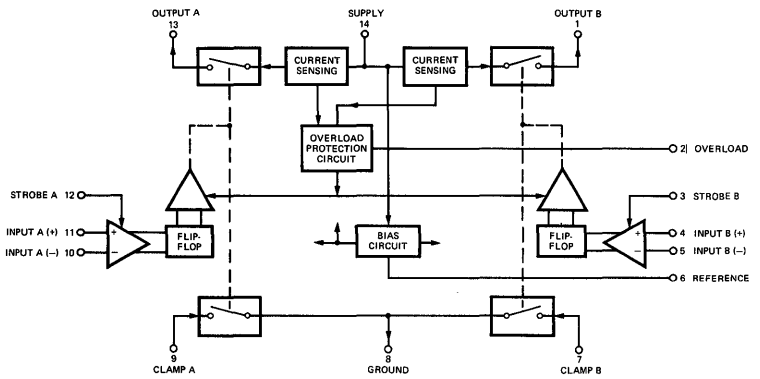


Fig. 3

TEST CIRCUIT 1

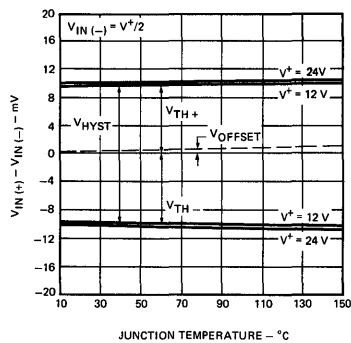


BLOCK DIAGRAM

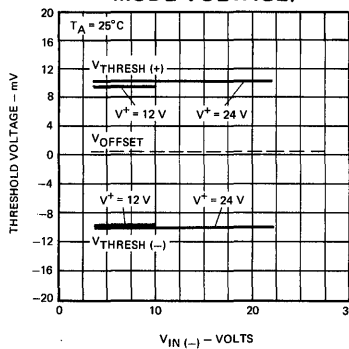


TYPICAL PERFORMANCE CURVES FOR 750C

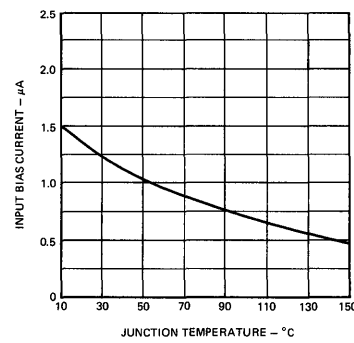
INPUT THRESHOLD AND HYSTERESIS VOLTAGE AS A FUNCTION OF TEMPERATURE



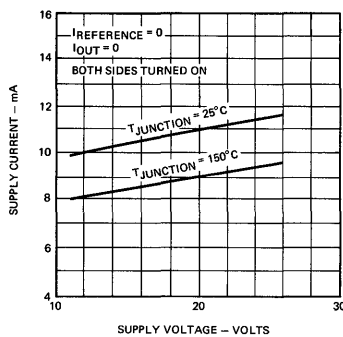
THRESHOLD VOLTAGE AS A FUNCTION OF THE VOLTAGE APPLIED TO THE INPUT (-) TERMINAL (COMMON MODE VOLTAGE)



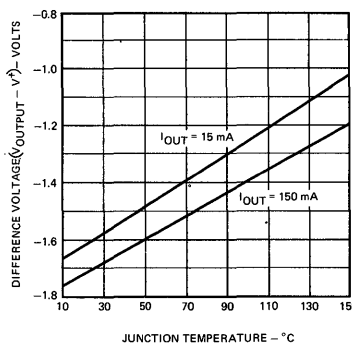
INPUT BIAS CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



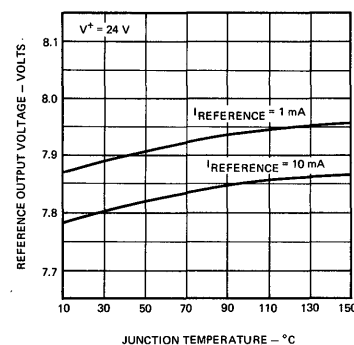
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



VOLTAGE DIFFERENCE BETWEEN OUTPUT AND SUPPLY VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE AND OUTPUT CURRENT

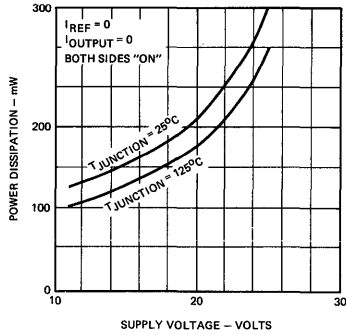


REFERENCE OUTPUT VOLTAGE AS A FUNCTION OF TEMPERATURE AND REFERENCE OUTPUT CURRENT

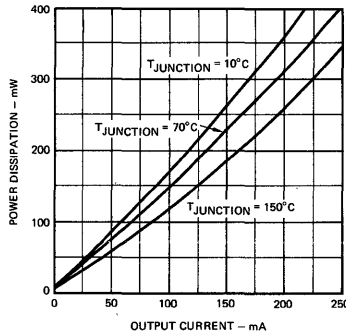


TYPICAL PERFORMANCE CURVES FOR 750C (Cont'd)

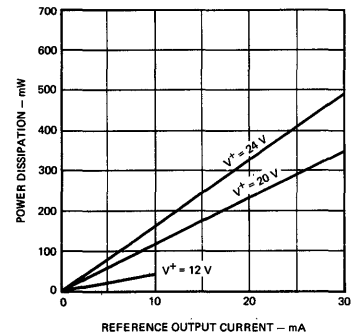
POWER DISSIPATION DUE TO BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



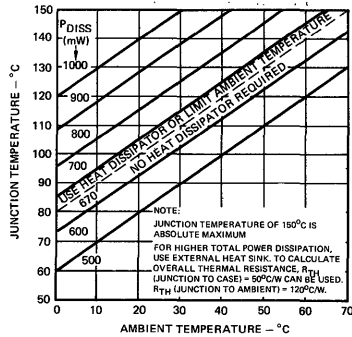
POWER DISSIPATION AS A FUNCTION OF OUTPUT CURRENT (ONE SIDE) AND JUNCTION TEMPERATURE



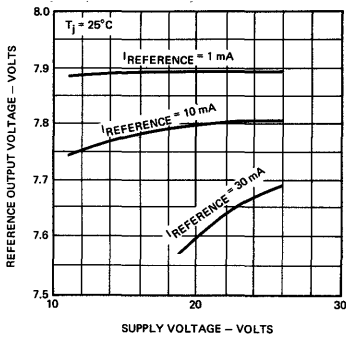
POWER DISSIPATION DUE TO REFERENCE OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



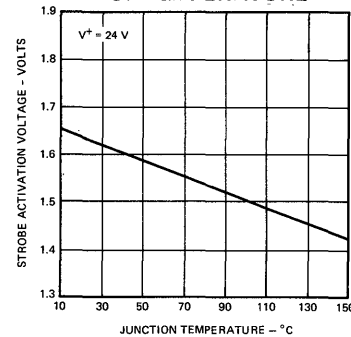
JUNCTION TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE AND POWER DISSIPATION



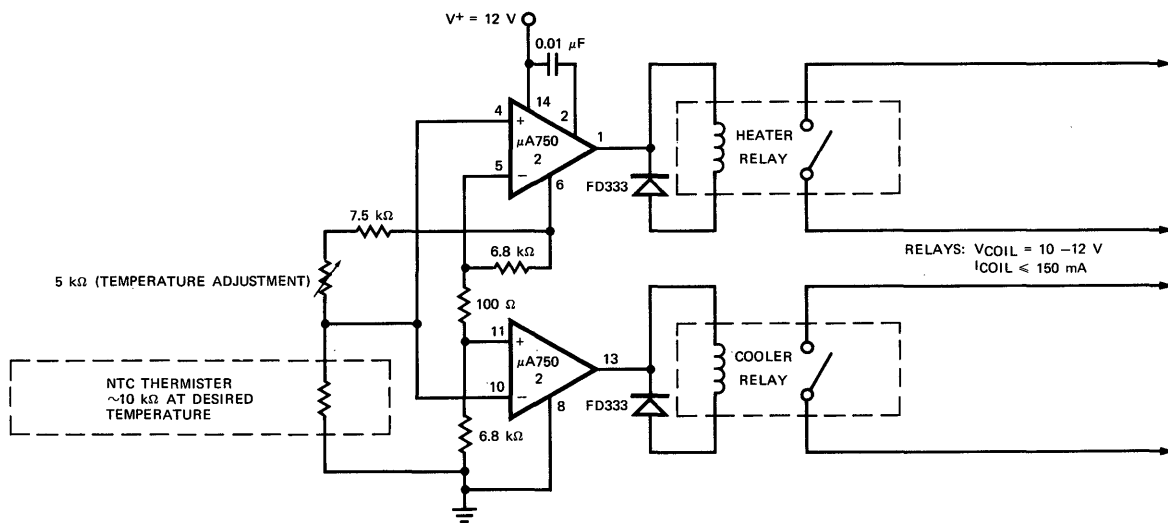
REFERENCE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND OUTPUT CURRENT



STROBE ACTIVATION VOLTAGE AS A FUNCTION OF TEMPERATURE



TYPICAL APPLICATION TEMPERATURE CONTROL SYSTEM



μA760

HIGH SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

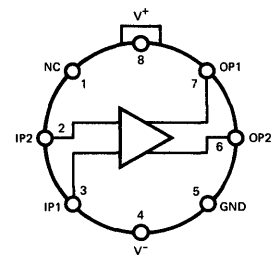
GENERAL DESCRIPTION — The μA760 is a Differential Voltage Comparator offering considerable speed improvement over the μA710 family and operation from symmetric supplies of from ±4.5 V to ±6.5 V. The μA760 can be used in high speed analog to digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The μA760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

- **GUARANTEED HIGH SPEED . . . 25 ns MAX**
- **GUARANTEED DELAY MATCHING ON BOTH OUTPUTS**
- **COMPLEMENTARY TTL COMPATIBLE OUTPUTS**
- **HIGH SENSITIVITY**
- **USES STANDARD SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+8 V
Negative Supply Voltage	-8 V
Peak Output Current	10 mA
Differential Input Voltage	±5 V
Input Voltage	$V_+ \geq V_{IN} \geq V_-$
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	
Military (760)	-55°C to 125°C
Commercial (760C)	0°C to 70°C
Storage Temperature Range	
Metal Can and DIP	-65°C to 150°C

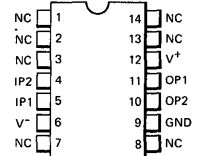
CONNECTION DIAGRAM
8-LEAD METAL CAN
 (TOP VIEW)
 PACKAGE OUTLINE 5B



ORDER INFORMATION

TYPE	PART NO.
760	760HM
760C	760HC

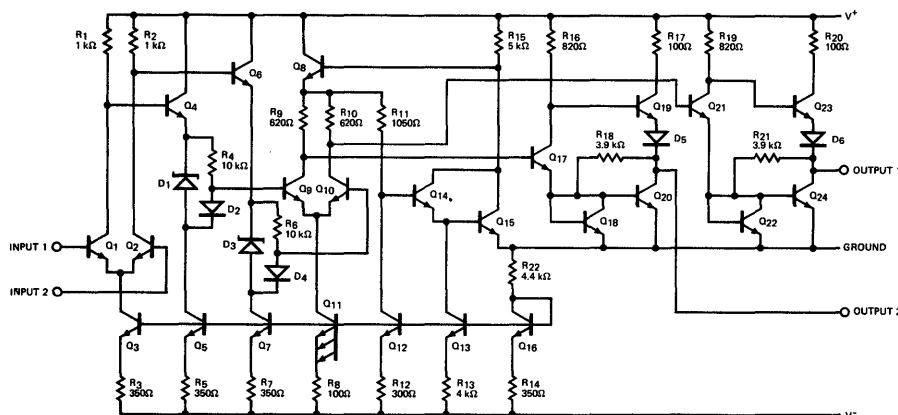
14-LEAD DIP
 (TOP VIEW)
 PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
760	760DM
760C	760DC

EQUIVALENT CIRCUIT



Notes on following page.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A760

760

ELECTRICAL CHARACTERISTICS ($V_S = \pm 4.5V$ to $\pm 6.5V$, $T_A = -55^\circ C$ to $+125^\circ C$, $T_A = 25^\circ C$ for typical figures unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, $T_A = 25^\circ C$		18	30	ns
	Note 3, $T_A = 25^\circ C$			25	ns
	Note 4		16		ns
Response Time Difference between Outputs					
$(t_{pd} \text{ of } +V_{IN1}) - (t_{pd} \text{ of } -V_{IN2})$	Note 2, $T_A = 25^\circ C$			5.0	ns
$(t_{pd} \text{ of } +V_{IN2}) - (t_{pd} \text{ of } -V_{IN1})$	Note 2, $T_A = 25^\circ C$			5.0	ns
$(t_{pd} \text{ of } +V_{IN1}) - (t_{pd} \text{ of } +V_{IN2})$	Note 2, $T_A = 25^\circ C$			7.5	ns
$(t_{pd} \text{ of } -V_{IN1}) - (t_{pd} \text{ of } -V_{IN2})$	Note 2, $T_A = 25^\circ C$			7.5	ns
Input Resistance	$f = 1 \text{ MHz}$		12		k Ω
Input Capacitance	$f = 1 \text{ MHz}$		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = -55^\circ C$ to $T_A = +125^\circ C$		3.0		$\mu V/^\circ C$
Average Temperature Coefficient of Input Offset Current	$T_A = 25^\circ C$ to $T_A = +125^\circ C$		2.0		nA/ $^\circ C$
	$T_A = 25^\circ C$ to $T_A = -55^\circ C$		7.0		nA/ $^\circ C$
Input Voltage Range	$V_S = \pm 6.5V$	± 4.0	± 4.5		V
Differential Input Voltage Range			± 5.0		V
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0 \text{ mA}$ $V_S = \pm 5.0V$	2.4	3.2		V
	$I_{OUT} = 80 \mu A$, $V_S = \pm 4.5V$	2.4	3.0		V
Output LOW Voltage (either output)	$I_{SINK} = 3.2 \text{ mA}$		0.25	0.4	V
Positive Supply Current	$V_S = \pm 6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm 6.5V$		9.0	16	mA

4

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A760

760C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 4.5V$ to $\pm 6.5V$, $T_A = 0^\circ C$ to $+70^\circ C$, $T_A = 25^\circ C$ for typical figures unless otherwise specified.)

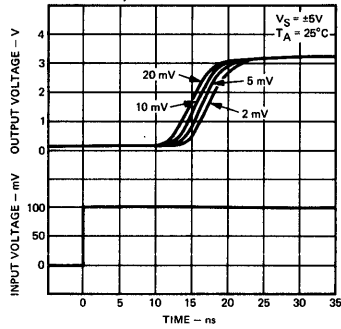
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, $T_A = 25^\circ C$		18	30	ns
	Note 3, $T_A = 25^\circ C$			25	ns
	Note 4		16		ns
Response Time Difference between Outputs	$(t_{pd} \text{ of } +V_{IN1}) - (t_{pd} \text{ of } -V_{IN2})$	Note 2, $T_A = 25^\circ C$		5.0	ns
	$(t_{pd} \text{ of } +V_{IN2}) - (t_{pd} \text{ of } -V_{IN1})$	Note 2, $T_A = 25^\circ C$		5.0	ns
	$(t_{pd} \text{ of } +V_{IN1}) - (t_{pd} \text{ of } +V_{IN2})$	Note 2, $T_A = 25^\circ C$		10	ns
	$(t_{pd} \text{ of } -V_{IN1}) - (t_{pd} \text{ of } -V_{IN2})$	Note 2, $T_A = 25^\circ C$		10	ns
Input Resistance	$f = 1 \text{ MHz}$		12		$k\Omega$
Input Capacitance	$f = 1 \text{ MHz}$		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 0^\circ C$ to $T_A = +70^\circ C$		3.0		$\mu V/^\circ C$
Average Temperature Coefficient of Input Offset Current	$T_A = 25^\circ C$ to $T_A = +70^\circ C$		5.0		$nA/^\circ C$
	$T_A = 25^\circ C$ to $T_A = 0^\circ C$		10		$nA/^\circ C$
Input Voltage Range	$V_S = \pm 6.5V$	± 4.0	± 4.5		V
Differential Input Voltage Range			± 5.0		V
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0 \text{ mA}$				
	$V_S = \pm 5.0V$	2.4	3.2		V
	$I_{OUT} = 80 \mu A$, $V_S = \pm 4.5V$	2.5	3.0		V
Output LOW Voltage (either output)	$I_{SINK} = 3.2 \text{ mA}$		0.25	0.4	V
Positive Supply Current	$V_S = \pm 6.5V$		18	34	mA
Negative Supply Current	$V_S = \pm 6.5V$		9.0	16	mA

NOTES

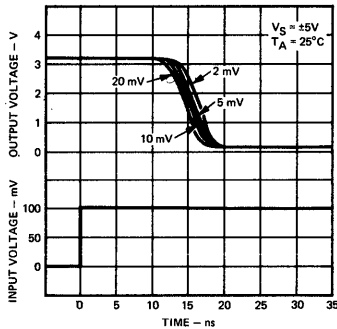
- Rating applies to ambient temperatures up to $70^\circ C$. Above $70^\circ C$ ambient derate linearly at $6.3 \text{ mW}/^\circ C$ for Metal Can and $8.3 \text{ mW}/^\circ C$ for the DIP.
- Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
- Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
- Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

TYPICAL PERFORMANCE CURVES FOR 760 AND 760C

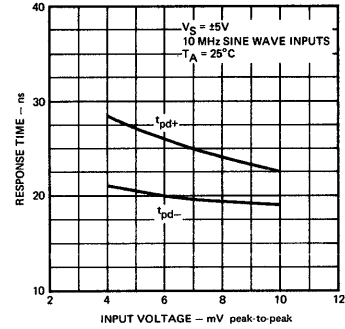
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



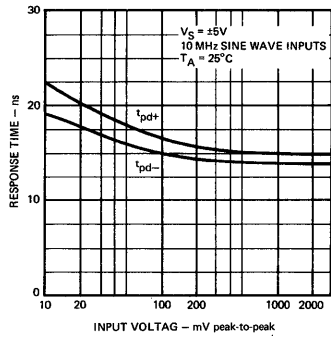
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



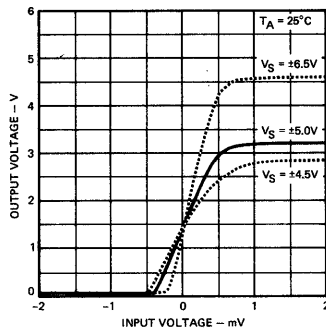
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



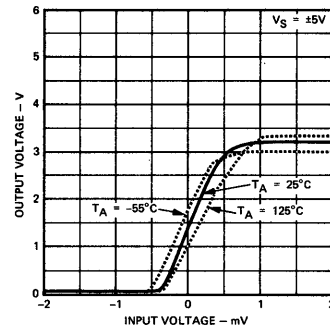
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



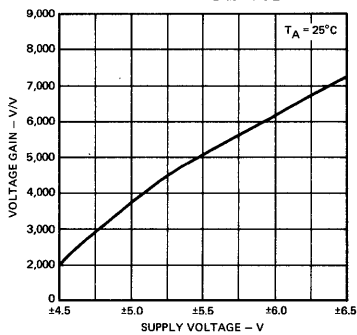
VOLTAGE TRANSFER CHARACTERISTIC



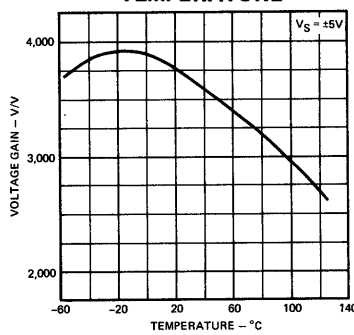
VOLTAGE TRANSFER CHARACTERISTIC



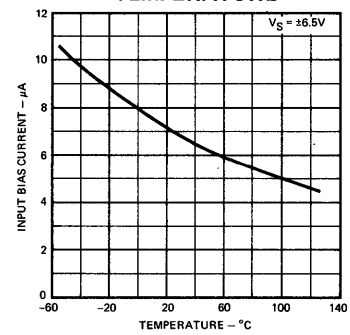
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



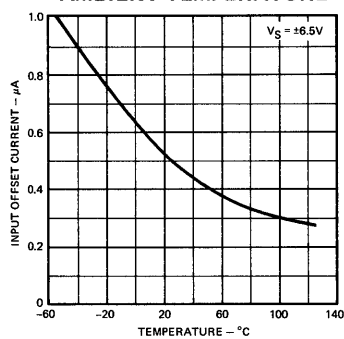
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



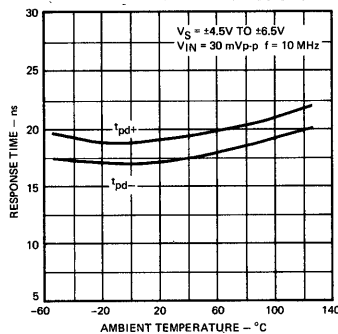
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



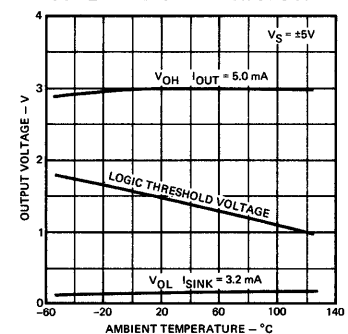
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



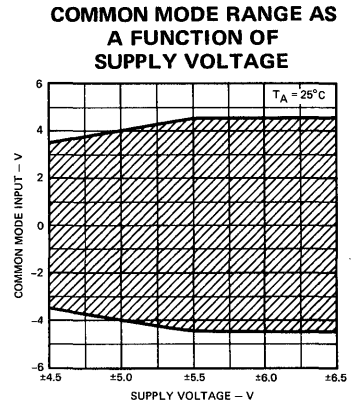
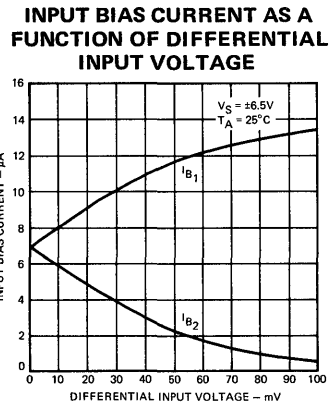
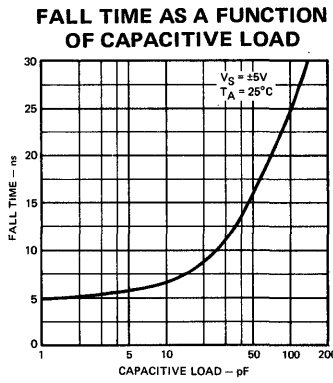
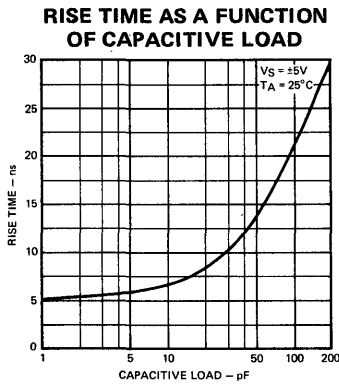
RESPONSE TIME AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



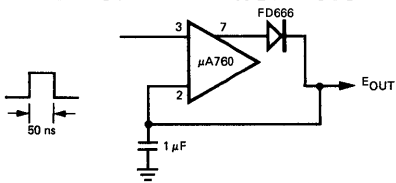
TYPICAL PERFORMANCE CURVES FOR 760 AND 760C (Cont'd)



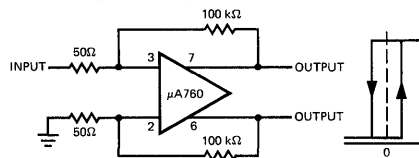
APPLICATIONS

Pin numbers shown are only for Metal Can.

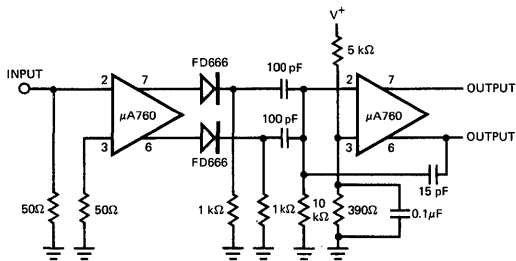
FAST POSITIVE PEAK DETECTOR



LEVEL DETECTOR WITH HYSTERESIS

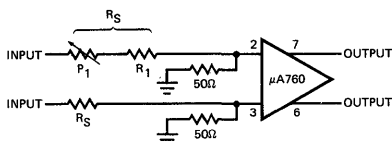


ZERO CROSSING DETECTOR



Total delay = 30 ns
Input frequency = 300 Hz to 3 MHz
Minimum input voltage = 20 mVp-p

LINE RECEIVER WITH HIGH COMMON MODE RANGE



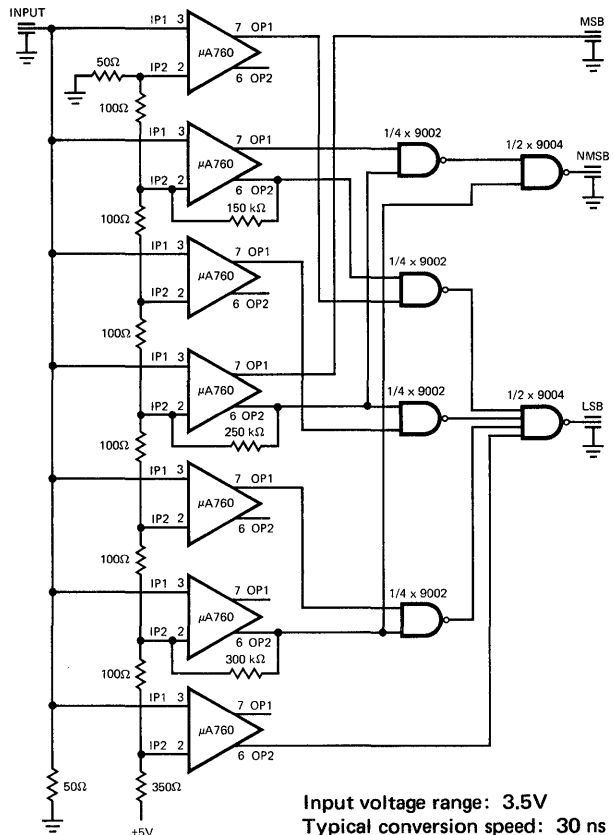
$$\text{Common mode range} = \pm 4 \times \frac{R_S}{50} \text{ V}$$

$$\text{Differential Input sensitivity} = 5 \times \frac{R_S}{50} \text{ mV}$$

P_1 must be adjusted for optimum common mode rejection.

For $R_S = 200\Omega$
Common mode range = $\pm 16\text{V}$
Sensitivity = 20 mV

HIGH SPEED 3-BIT A/D CONVERTER



Input voltage range: 3.5V
Typical conversion speed: 30 ns

111•311

VOLTAGE COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 111 and 311 are monolithic, low input current Voltage Comparators, each constructed using the Fairchild Planar* epitaxial process. The 111 series operates from the single 5 V supply used for integrated circuit logic to the standard ± 15 V operational amplifier supplies. The 111 series is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

- **LOW INPUT BIAS CURRENT . . . 60 nA**
- **LOW INPUT OFFSET CURRENT . . . 4 nA**
- **DIFFERENTIAL INPUT VOLTAGE . . . ± 30 V**
- **POWER SUPPLY VOLTAGE SINGLE 5.0 V SUPPLY TO ± 15 V**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **STROBE CAPABILITY**

ABSOLUTE MAXIMUM RATINGS

Voltage Between V_+ and V_- Terminals	36 V
Output to V_- (111)	50 V
(311)	40 V
Ground to V_-	30 V
Differential Input Voltage	± 30 V
Input Voltage (Note 1)	± 15 V
Internal Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 seconds
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Military (111)	0°C to $+70^\circ\text{C}$
Commercial (311)	

CONNECTION DIAGRAM
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B

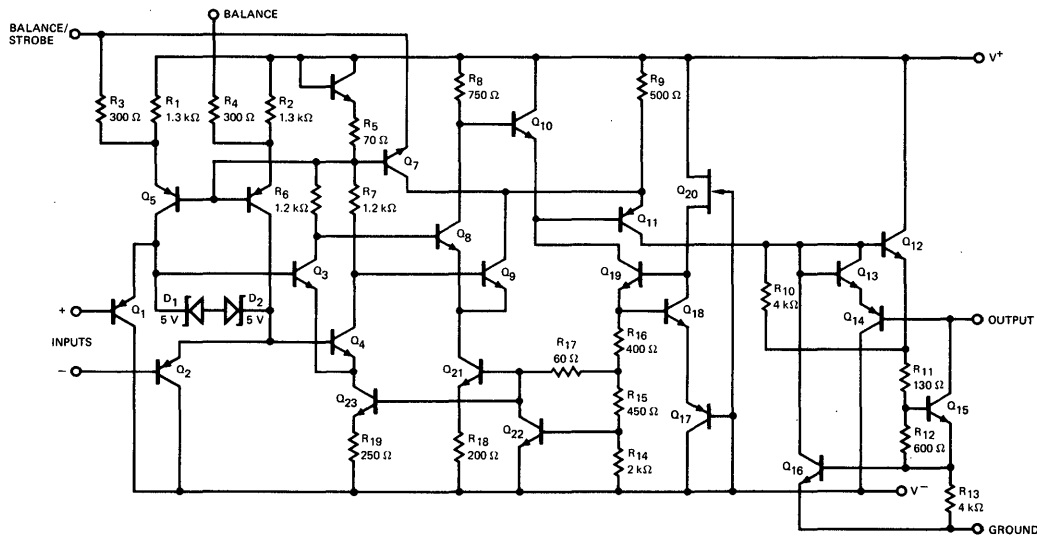
ORDER INFORMATION

TYPE	PART NO.
111	LM111H
311	LM311H

TRUTH TABLE

V_{IN}	STROBE	OUTPUT
+	H	H
+	L	L
-	H	L
-	L	L

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise specified) Note 3

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Note 4)	$T_A = 25^\circ\text{C}$, $R_S \leq 50\text{ k}\Omega$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25^\circ\text{C}$		4.0	10	nA
Input Bias Current	$T_A = 25^\circ\text{C}$		60	100	nA
Voltage Gain	$T_A = 25^\circ\text{C}$		200		V/mV
Response Time (Note 5)	$T_A = 25^\circ\text{C}$		200		ns
Saturation Voltage	$V_{IN} \leq -5\text{ mV}$, $I_{OUT} = 50\text{ mA}$ $T_A = 25^\circ\text{C}$		0.75	1.5	V
Strobe On Current	$T_A = 25^\circ\text{C}$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 35\text{ V}$ $T_A = 25^\circ\text{C}$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50\text{ k}\Omega$			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range			± 14		V
Saturation Voltage	$V^+ \geq 4.5\text{ V}$, $V^- = 0$ $V_{IN} \leq -6\text{ mV}$, $I_{SINK} \leq 8\text{ mA}$		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 35\text{ V}$		0.1	0.5	μA
Positive Supply Current	$T_A = 25^\circ\text{C}$		5.1	6.0	mA
Negative Supply Current	$T_A = 25^\circ\text{C}$		4.1	5.0	mA

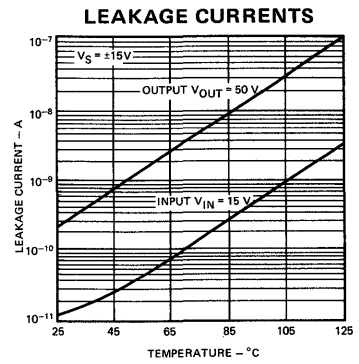
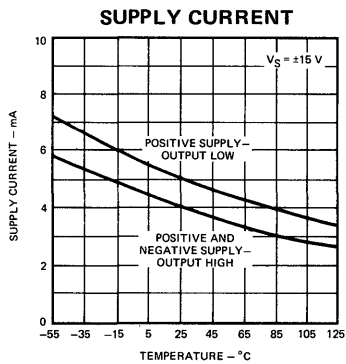
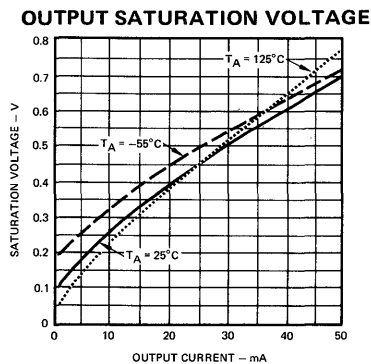
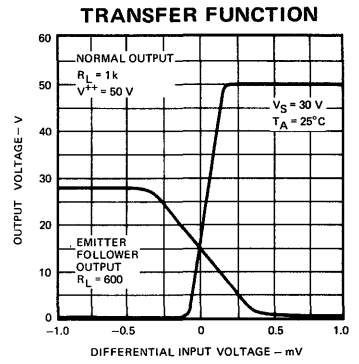
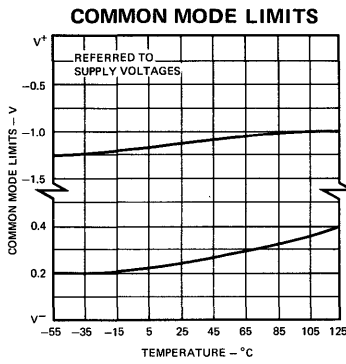
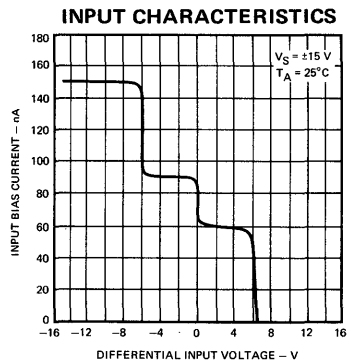
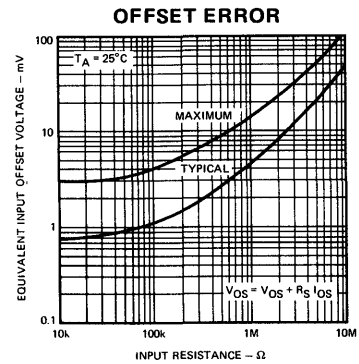
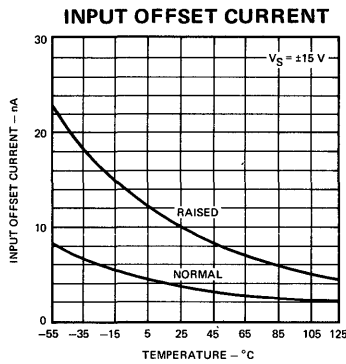
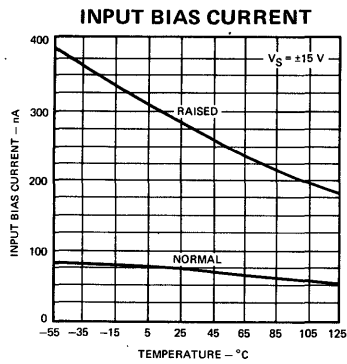
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise specified) Note 3

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Note 4)	$T_A = 25^\circ\text{C}$, $R_S \leq 50\text{ k}\Omega$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25^\circ\text{C}$		6.0	50	nA
Input Bias Current	$T_A = 25^\circ\text{C}$		100	250	nA
Voltage Gain	$T_A = 25^\circ\text{C}$		200		V/mV
Response Time (Note 5)	$T_A = 25^\circ\text{C}$		200		ns
Saturation Voltage	$V_{IN} \leq -10\text{ mV}$, $I_{OUT} = 50\text{ mA}$ $T_A = 25^\circ\text{C}$		0.75	1.5	V
Strobe On Current	$T_A = 25^\circ\text{C}$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10\text{ mV}$, $V_{OUT} = 35\text{ V}$ $T_A = 25^\circ\text{C}$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50\text{ k}\Omega$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			± 14		V
Saturation Voltage	$V^+ \geq 4.5\text{ V}$, $V^- = 0$ $V_{IN} \leq -10\text{ mV}$, $I_{SINK} \leq 8\text{ mA}$		0.23	0.4	V
Positive Supply Current	$T_A = 25^\circ\text{C}$		5.1	7.5	mA
Negative Supply Current	$T_A = 25^\circ\text{C}$		4.1	5.0	mA

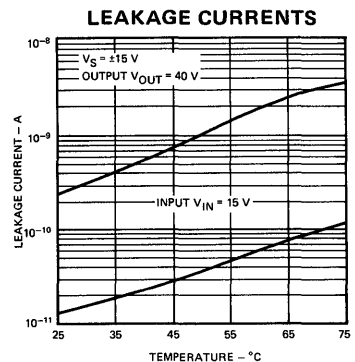
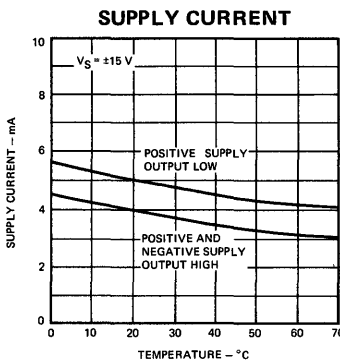
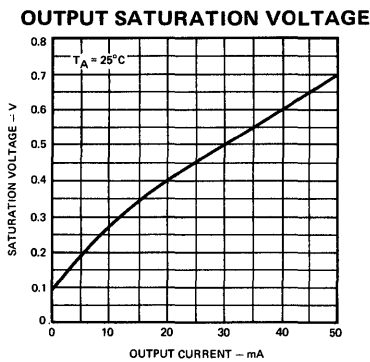
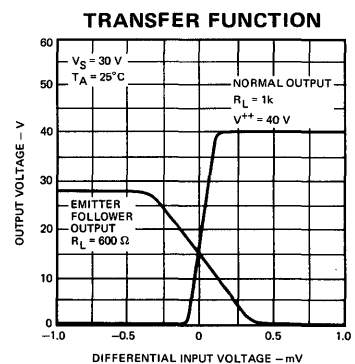
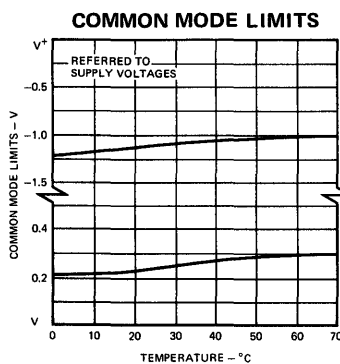
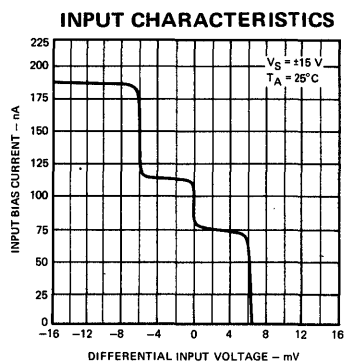
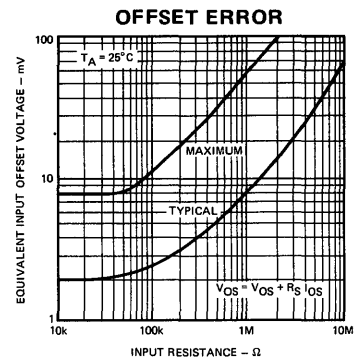
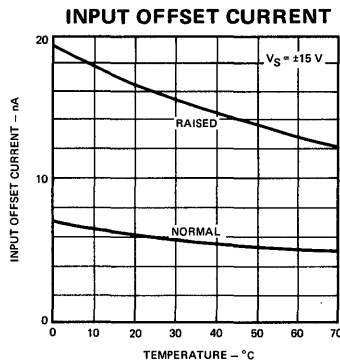
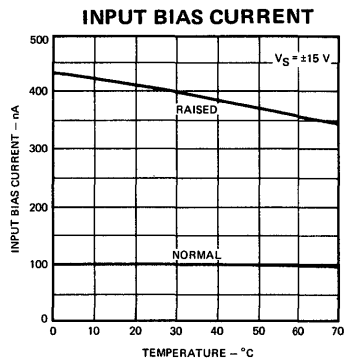
NOTES:

1. This rating applies for $\pm 15\text{ V}$ supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3\text{ mW}/^\circ\text{C}$.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to $\pm 15\text{ V}$ supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL PERFORMANCE CURVES FOR 111

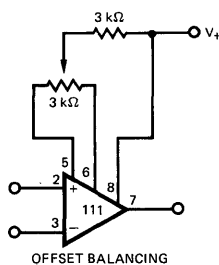


TYPICAL PERFORMANCE CURVES FOR 311

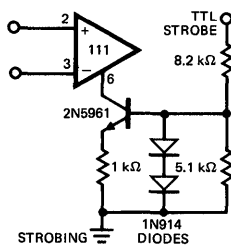


TYPICAL APPLICATIONS

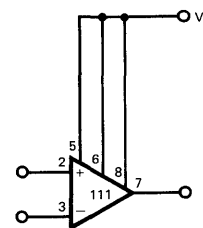
OFFSET NULL CIRCUIT



STROBE CIRCUIT



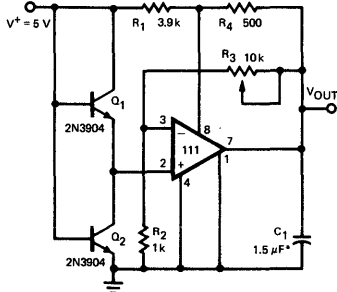
INCREASING INPUT STAGE CURRENT *



*Increases typical common mode slew rate from 7.0 V/μs to 18 V/μs

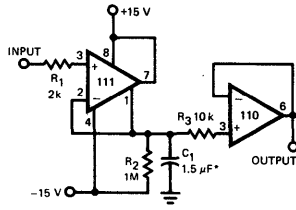
TYPICAL APPLICATIONS (Cont'd)

ADJUSTABLE LOW VOLTAGE REFERENCE SUPPLY



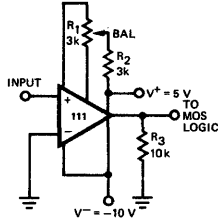
*Solid tantalum

POSITIVE PEAK DETECTOR

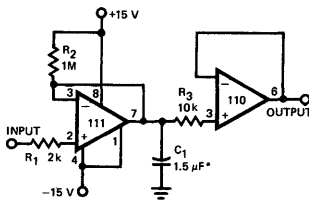


*Solid tantalum

ZERO CROSSING DETECTOR DRIVING MOS LOGIC

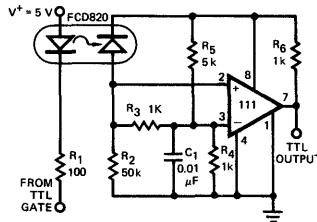


NEGATIVE PEAK DETECTOR

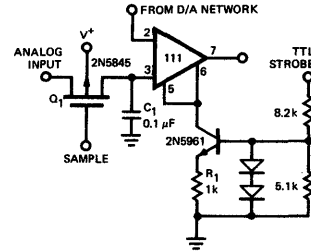


*Solid tantalum

DIGITAL TRANSMISSION ISOLATOR

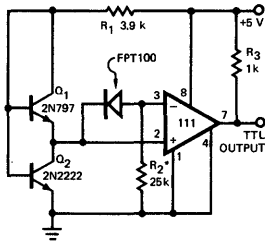


STROBING OF BOTH INPUT AND OUTPUT STAGES



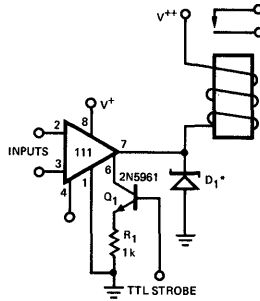
*Typical input current is 50 pA with inputs strobed off.

PRECISION PHOTODIODE COMPARATOR



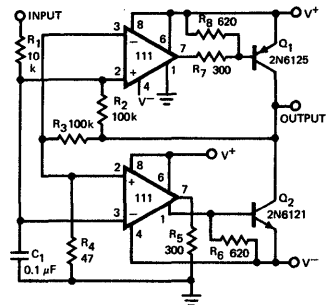
*R₂ sets the comparison level.
At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

RELAY DRIVER WITH STROBE

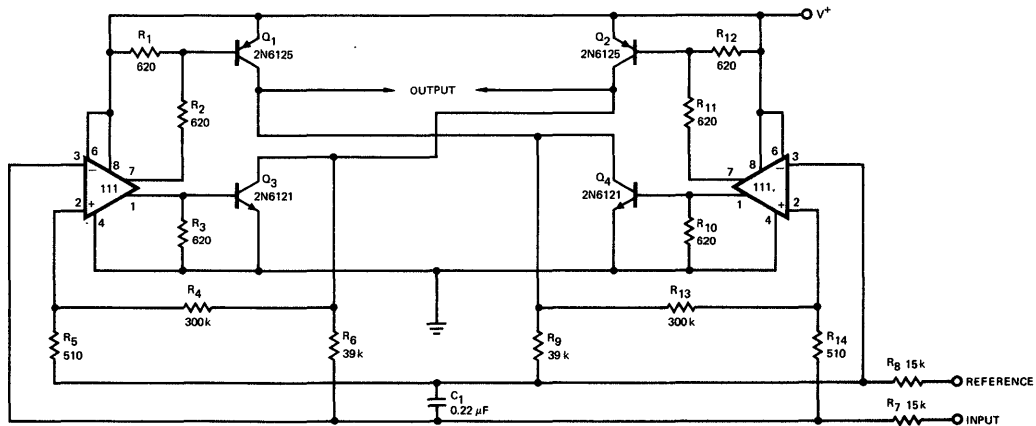


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V⁺⁺ line.

SWITCHING POWER AMPLIFIER



SWITCHING POWER AMPLIFIER



GLOSSARY

COMPARATORS

Average Temperature Coefficient of Input Offset Current — The change in input offset current over the operating temperature range divided by the operating temperature range.

Average Temperature Coefficient of Input Offset Voltage — The change in input offset voltage over the operating temperature range divided by the operating temperature range.

Common Mode Rejection Ratio — The ratio of the change of input offset voltage to the change in common mode voltage producing it.

Differential Input Voltage Range — The range of voltage applied between the input terminals for which operation within specifications is assured.

Input Bias Current — The average of the two input currents with no signal applied.

Input Capacitance — The capacitance seen looking into either input terminal with the other grounded.

Input Common Mode Voltage Range — The range of common mode input voltage over which the device will operate within specifications.

Input Offset Current — The difference between the two input currents with the output at the logic threshold voltage.

Input Offset Voltage — That voltage which must be applied to the input terminals to give the logic threshold voltage at the output.

Input Resistance — The resistance seen looking into either input terminal with the other grounded.

Input Voltage Range — The range of voltage on either input terminal over which the device will operate as specified.

Logic Threshold Voltage — The output voltage at which the logic circuitry being driven changes state. It has two values, positive and negative.

Negative Output Voltage Level — The dc output voltage in the negative direction with the input voltage equal to, or greater than, a minimum specified value.

Output Fall Time — The time taken for the output voltage to fall from 90% to 10% of its value with a step-function applied at the input.

Output Resistance — The resistance seen looking in to the output with the dc output level at the logic threshold.

Output Rise Time — The time taken for the output voltage to rise from 10% to 90% of its value with a step-function at the input.

Output Sink Current — The maximum negative current that can be delivered by the comparator.

Positive Output Voltage Level — The dc output voltage in the positive direction with the input voltage equal to, or greater than, a minimum specified value.

Response Time — The interval between the application of an input step function and the time when the output voltage crosses the logic threshold level.

Strobed Output Level — The dc output voltage, independent of input voltage, with the voltage on the strobe terminal in excess of the strobe activation voltage.

Strobe Activation Voltage — The voltage applied to the strobe terminal beyond which the device does not respond to the conditions at the input terminals.

Strobe Current — The maximum current taken by the strobe terminal during activation.

Strobe Input Resistance — The resistance between the strobe terminal and ground.

Strobe Release Time — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been activated.

Supply Voltage Rejection Ratio — The ratio of the change in input offset voltage to the change in supply voltage producing it.

Voltage Gain — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the dc output in the vicinity of the logic threshold.

LINEAR LINEAR LINEAR LINEAR LINEAR LINEAR

CONTENTS AND SECTION SELECTOR

VOLTAGE REGULATORS	5
COMPUTER / INTERFACE	6
CONSUMER	7
TRANSISTOR / DIODE ARRAYS / ANALOG SWITCHES	8
PACKAGE OUTLINES	9
ORDER INFORMATION	10
MIL-M 38510 / MIL-STD-883	11
DICE	12
INDUSTRY CROSS REFERENCE GUIDE	13
APPLICATION INFORMATION	14

INDEX

Selection Guide 5-4

DATA SHEETS

Adjustable Positive

μ A723 Precision Voltage Regulator 5-7
105 Voltage Regulator 5-30
305 Voltage Regulator 5-30
305A Voltage Regulator 5-30
376 Voltage Regulator 5-30

Fixed Positive

μ A7805 Three-Terminal Positive Voltage Regulator 5-14
 μ A7806 Three-Terminal Positive Voltage Regulator 5-14
 μ A7808 Three-Terminal Positive Voltage Regulator 5-14
 μ A7812 Three-Terminal Positive Voltage Regulator 5-14
 μ A7815 Three-Terminal Positive Voltage Regulator 5-14
 μ A7818 Three-Terminal Positive Voltage Regulator 5-14
 μ A7824 Three-Terminal Positive Voltage Regulator 5-14
 μ A78M00 Three-Terminal Positive Voltage Regulators 5-45
109 Five Volt Regulator 5-36
209 Five Volt Regulator 5-36
309 Five Volt Regulator 5-40

Adjustable Negative

μ A723 Precision Voltage Regulator 5-7
104 Negative Voltage Regulator 5-25
304 Negative Voltage Regulator 5-25

Fixed Negative

μ A78N00 Three-Terminal Negative Voltage Regulators 5-51

Fixed Positive and Negative

μ A78T00 Tracking Voltage Regulators 5-44

Precision Voltage Reference

μ A728 Precision Voltage Reference 5-44

Products to be Announced 5-43

Glossary 5-52

INTRODUCTION

Fairchild Semiconductor produces the most comprehensive line of monolithic voltage regulators available. This line includes fixed output, three-terminal regulators for a range of output voltages from 5.0 V to 30 V. Both positive and negative three-terminal voltage regulators are available, with rated output currents from 500 mA to 3.0 A.

For requirements not covered by the fixed output devices Fairchild offers a line of flexible precision regulators for all applications, including positive, negative, tracking, and switching.

The breadth of the product line, the built-in overload protection in every device, the precision, and the flexibility make Fairchild the place to go for volume deliveries of economical, easy to use, reliable voltage regulators.

SELECTION GUIDE FOR COMMERCIAL VOLTAGE REGULATORS ⁽⁴⁾

		FIXED POSITIVE μA7800 SERIES								
		μA7805	μA7806	μA7808	μA7812	μA7815	μA7818	μA7824	209	309
Input Voltage Range	Min. (V)	7.0	8.0	10	14	17	20	26	7.0	7.0
	Max. (V)	35	35	35	35	35	35	40	35	35
Output Voltage	Min. (V)	4.8	5.75	7.7	11.5	14.4	17.3	23	4.7	4.8
	Max. (V)	5.2	6.25	8.3	12.5	15.6	18.7	25	5.3	5.2
Output Current	Max. (mA)	1000	1000	1000	1000	1000	1000	1000	1000	1000
	Peak (mA)	2200	2200	2200	2200	2100	2100	2100	2200	2200
Line Regulation	Max. (%) Notes 1, 2	2.0	2.0	2.0	2.0	2.0	2.0	2.0	1.0	2.0
Load Regulation	Max. (%) Notes 1, 2	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Quiescent Current	Max. (mA) Note 2	8.0	8.0	8.0	8.0	8.0	8.0	8.0	10	10
Ripple Rejection	Min. (dB) f = 120 Hz, Notes 2,3	62	59	56	55	54	53	50	—	—
Dropout Voltage	Typ. (V) I _{OUT} = I _{Max.}	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Output Voltage Drift	Typ. (mV/°C)	-1.1	-0.8	-0.8	-1.0	-1.0	-1.0	-1.5	-0.75	-0.8
	Max. (%/°C)									
OPERATIONAL AMPLIFIERS		X	X	X	X	X	X		X	X
TTL SYSTEMS		X							X	X
MOS SYSTEMS		X			CMOS				X	X
ECL SYSTEMS										
CONSUMER			X	X				X		

SELECTION GUIDE FOR MILITARY VOLTAGE REGULATORS ⁽⁴⁾

		FIXED POSITIVE μA7800 SERIES							
		μA7805	μA7806	μA7808	μA7812	μA7815	μA7818	μA7824	109
Input Voltage Range	Min. (V)	7.0	8.0	10	14	17	20	26	7.0
	Max. (V)	35	35	35	35	35	35	40	35
Output Voltage	Min. (V)	4.8	5.75	7.7	11.5	14.4	17.3	23	4.7
	Max. (V)	5.2	6.25	8.3	12.5	15.6	18.7	25	5.3
Output Current	Max. (mA)	1000	1000	1000	1000	1000	1000	1000	1000
	Peak (mA)	2200	2200	2200	2200	2100	2100	2100	2200
Line Regulation	Max. (%) Notes 1, 2	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Load Regulation	Max. (%) Notes 1, 2	1.0	1.0	1.0	1.0	1.0	1.0	1.0	2.0
Quiescent Current	Max. (nA) Note 2	6.0	6.0	6.0	6.0	6.0	6.0	6.0	10
Ripple Rejection	Min. (dB) f = 100 Hz, Note 2	68	65	62	61	60	59	56	—
Dropout Voltage	Typ. (V) I _{OUT} = I _{Max.}	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Output Voltage Drift	Typ. (mV/°C)	-1.1	-0.8	-0.8	-1.0	-1.0	-1.0	-1.5	-0.75
	Max. (%/°C)								
OPERATIONAL AMPLIFIERS		X	X	X	X	X	X		X
TTL SYSTEMS		X							X
MOS SYSTEMS		X			CMOS				X
ECL SYSTEMS									

NOTES:

1. % V_{OUT}
2. Typical for 78MXX and 78NXX Series
3. Typical for 723
4. The 7800 is available in TO-3 and TO-220 (Commercial Grade only). 109 and 78N00 are available in TO-3. The 723, 78M00 Series, 104, 105 are available in TO-5 type package. The 376 is available in 8-Lead mini-DIP.

FIXED POSITIVE μA78M00 SERIES							ADJUSTABLE POSITIVE				ADJUSTABLE NEGATIVE		FIXED NEGATIVE		
μA78M05	μA78M06	μA78M08	μA78M12	μA78M15	μA78M20	μA78M24	μA723	305	305A	376	μA723	304	μA78N02	μA78N04	μA78N05
7.0	8.0	10	14	17	22	26	9.5	8.0	8.5	9.0	-40	-40	-4.5	-6.5	-7.5
30	30	30	35	35	40	40	40	40	50	40	-9.5	-8.0	-15	-15	-15
4.8	5.75	7.7	11.5	14.4	19.0	23	2.0	4.5	4.5	5.0	-37	-30	-1.8	-3.8	-5.1
5.2	6.25	8.3	12.5	15.6	21.0	25	37	30	40	37	-2.0	0	-2.2	-4.2	-5.3
500	500	500	500	500	500	500	150	20	45	25	150	20	2500	2500	2500
750	750	750	750	700	700	700	-	-	-	-	-	-	3000	3000	3000
1.0	1.0	1.0	1.0	1.0	1.0	1.0	0.1	0.06	0.06	0.03	0.1	0.1	1.0	1.0	0.5
1.0	1.0	1.0	1.0	1.0	1.0	1.0	0.6	0.05	0.2	0.2	0.6	0.02	1.0	1.0	0.4
4.2	4.3	4.3	4.3	4.4	4.5	4.6	4.0	2.0	2.0	2.5	4.0	5.0	10	10	10
78	75	72	71	70	69	66	74	60	-	-	74	60	60	60	60
2.0	2.0	2.0	2.0	2.0	2.0	2.0	3.0	3.0	3.0	3.0	3.0	2.0	2.0	2.0	2.0
-	-	-	-	-	-	-	0.015	1.0	1.0	-	0.015	1.0	0.5	0.5	0.25
X	X	X	X	X	X		X	X	X	X	X	X			X
X								X	X	X	X				
X			CMOS				X	X	X	X	X	X			
								X	X	X	X	X	X	X	X
					X	X	X				X				

FIXED POSITIVE μA78M00 SERIES							ADJUSTABLE POSITIVE		ADJUSTABLE NEGATIVE	
μA78M05	μA78M06	μA78M08	μA78M12	μA78M15	μA78M20	μA78M24	μA723	105	μA723	104
7.0	8.0	10	14	17	22	26	9.5	8.0	-9.5	-50
30	30	30	35	35	40	40	40	50	-40	-8.0
4.8	5.75	7.7	11.5	14.4	19.0	23	2.0	4.5	-37	-40
5.2	6.25	8.3	12.5	15.6	21.0	25	37	40	-2.0	0
500	500	500	500	500	500	500	150	20	150	20
750	750	750	750	700	700	700	-	-	-	-
1.0	1.0	1.0	1.0	1.0	1.0	1.0	0.1	0.06	0.1	1.0
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.6	0.05	0.6	0.02
4.2	4.3	4.3	4.3	4.4	4.5	4.6	3.5	2.0	3.5	5.0
78	75	72	71	70	69	66	74	60	74	60
2.0	2.0	2.0	2.0	2.0	2.0	2.0	3.0	3.0	3.0	2.0
-	-	-	-	-	-	-	0.015	1.0	0.015	1.0
X	X	X	X	X	X		X	X	X	X
X								X	X	
X			CMOS				X	X	X	X
								X	X	X

5. Thermal resistance of the package without a heat sink.

Junction to Case Junction to Ambient

TO-3	4°C/W	35°C/W
TO-220	2°C/W	50°C/W
TO-5	20°C/W	150°C/W

μA723

PRECISION VOLTAGE REGULATOR

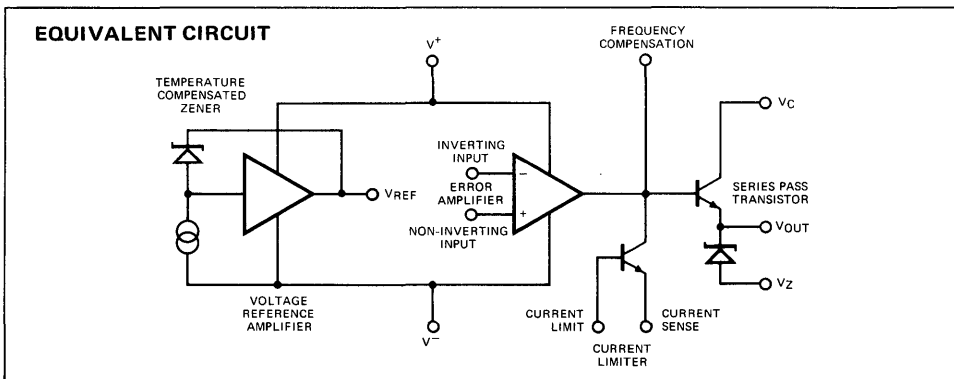
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA723 is a monolithic Voltage Regulator constructed using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- .01% LINE AND LOAD REGULATION
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS
- OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR

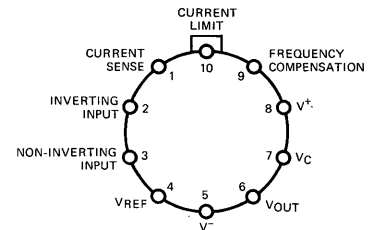
ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V_+ to V_- , (50 ms) (723)	50 V
Continuous Voltage from V_+ to V_-	40 V
Input/Output Voltage Differential	40 V
Differential Input Voltage	±5 V
Voltage Between Non-Inverting Input and V_-	+8 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	
Metal Can	800 mW
DIP	1000 mW
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (723)	-55°C to +125°C
Commercial (723C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C



Notes on following pages.

CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F

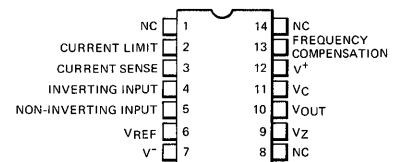


Note: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
723	723 HM
723C	723 HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
723	723 DM
723C	723 DC

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A723

723

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12V$ to $V_{IN} = 15V$		0.01	0.1	% V_{OUT}
	$V_{IN} = 12V$ to $V_{IN} = 40V$		0.02	0.2	% V_{OUT}
	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$, $V_{IN} = 12V$ to $V_{IN} = 15V$			0.3	% V_{OUT}
Load Regulation	$I_L = 1 mA$ to $I_L = 50 mA$		0.03	0.15	% V_{OUT}
	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$, $I_L = 1 mA$ to $I_L = 50 mA$			0.6	% V_{OUT}
Ripple Rejection	$f = 50 Hz$ to $10 kHz$		74		dB
	$f = 50 Hz$ to $10 kHz$, $C_{REF} = 5 \mu F$ (See Fig. 1)		86		dB
Average Temperature Coefficient of Output Voltage	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$		0.002	0.015	%/ $^{\circ}C$
Short Circuit Current Limit	$R_{SC} = 10\Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	$BW = 100 Hz$ to $10 kHz$, $C_{REF} = 0$		20		μV_{rms}
	$BW = 100 Hz$ to $10 kHz$, $C_{REF} = 5 \mu F$		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30V$		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input/Output Voltage Differential		3.0		38	V

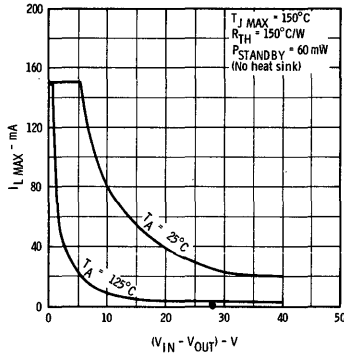
723C

ELECTRICAL CHARACTERISTICS (Note 2)

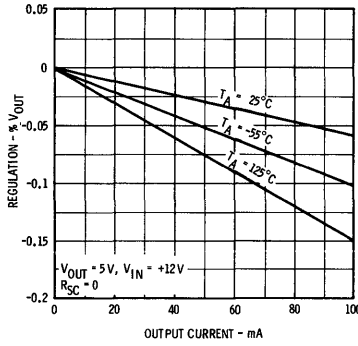
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12V$ to $V_{IN} = 15V$		0.01	0.1	% V_{OUT}
	$V_{IN} = 12V$ to $V_{IN} = 40V$		0.1	0.5	% V_{OUT}
	$0^{\circ}C \leq T_A \leq 70^{\circ}C$, $V_{IN} = 12V$ to $V_{IN} = 15V$			0.3	% V_{OUT}
Load Regulation	$I_L = 1 mA$ to $I_L = 50 mA$		0.03	0.2	% V_{OUT}
	$0^{\circ}C \leq T_A \leq 70^{\circ}C$, $I_L = 1 mA$ to $I_L = 50 mA$			0.6	% V_{OUT}
Ripple Rejection	$f = 50 Hz$ to $10 kHz$		74		dB
	$f = 50 Hz$ to $10 kHz$, $C_{REF} = 5 \mu F$ (See Fig. 1)		86		dB
Average Temperature Coefficient of Output Voltage	$0^{\circ}C \leq T_A \leq 70^{\circ}C$		0.003	0.015	%/ $^{\circ}C$
Short Circuit Current Limit	$R_{SC} = 10\Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	$BW = 100 Hz$ to $10 kHz$, $C_{REF} = 0$		20		μV_{rms}
	$BW = 100 Hz$ to $10 kHz$, $C_{REF} = 5 \mu F$		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30V$		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input/Output Voltage Differential		3.0		38	V

TYPICAL PERFORMANCE CURVES FOR 723

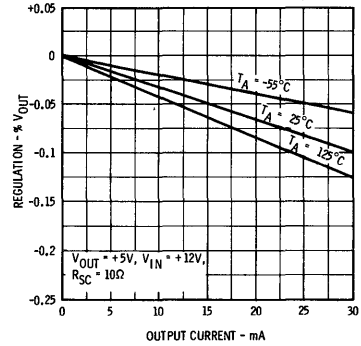
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



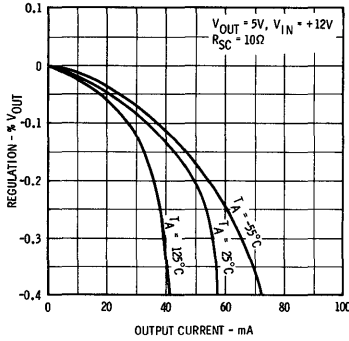
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



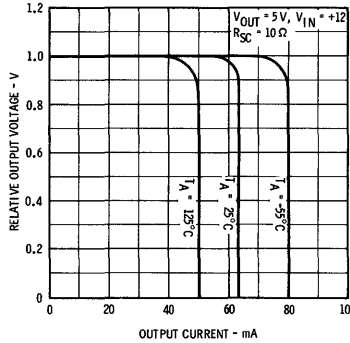
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



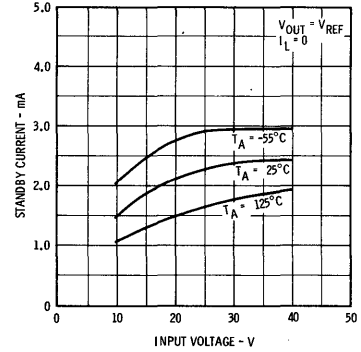
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS

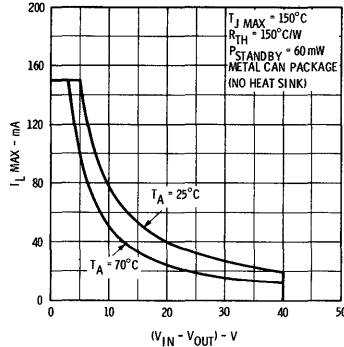


STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

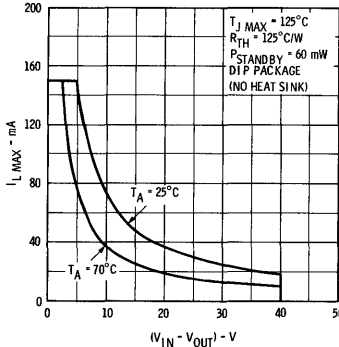


TYPICAL PERFORMANCE CURVES FOR 723C

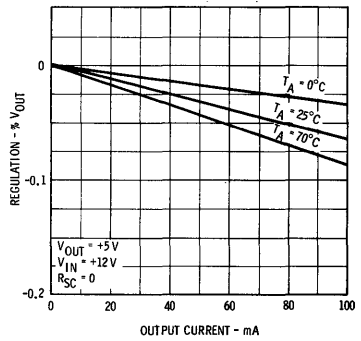
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



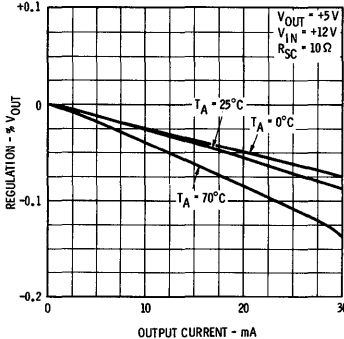
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



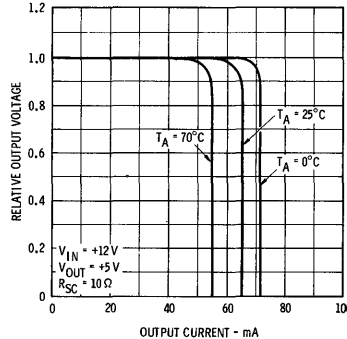
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



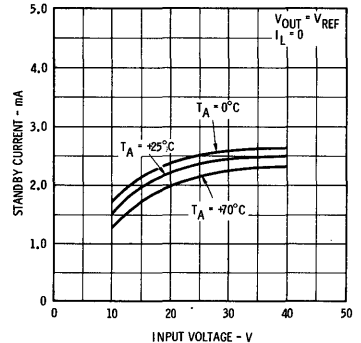
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS

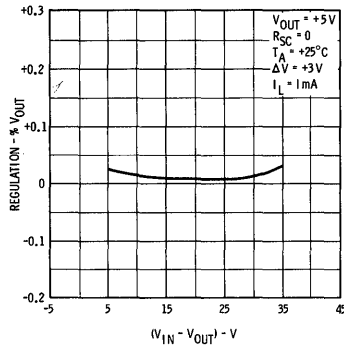


STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

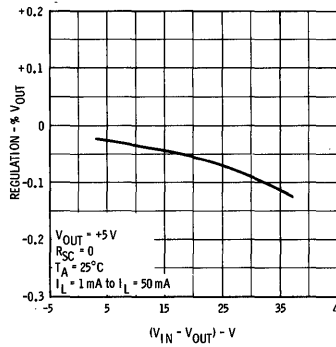


TYPICAL PERFORMANCE CURVES FOR 723 AND 723C

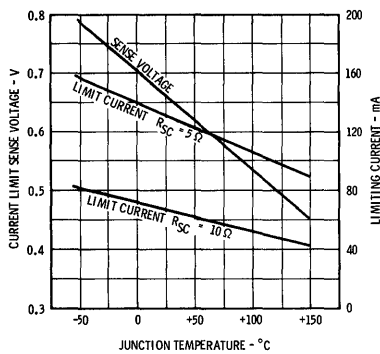
LINE REGULATION AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



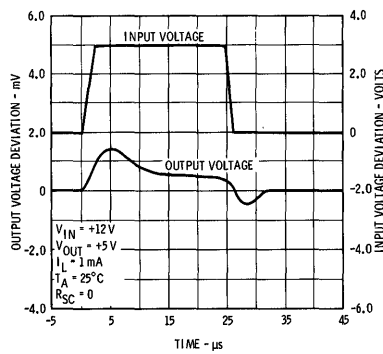
LOAD REGULATION AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



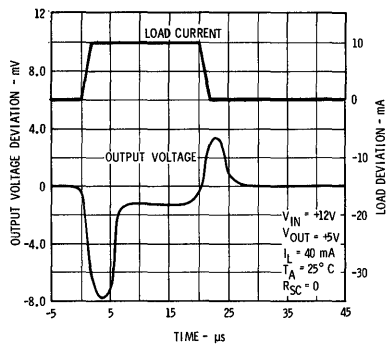
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



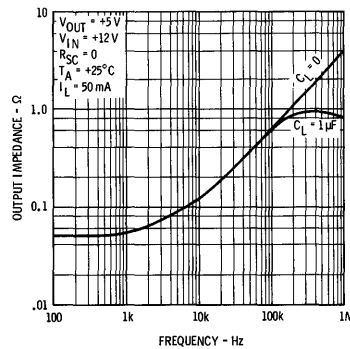
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



NOTES

1. Rating applies to ambient temperatures up to $25^\circ C$. Above $25^\circ C$ ambient derate linearly at $6.3 mW/^\circ C$ for the Metal Can, and $8.3 mW/^\circ C$ for the DIP.
2. Unless otherwise specified, $T_A = 25^\circ C$, $V_{IN} = V_+ = V_C = 12V$, $V_- = 0$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0$, $C_1 = 100 pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq 10 k\Omega$ connected as shown in Fig. 1. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.
3. L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
4. Figures in parentheses may be used if R_1/R_2 divider is placed on opposite side of error amp.
5. Replace R_1/R_2 in figures with divider shown in figure 13.
6. V^+ must be connected to a +3V or greater supply.
7. For metal can applications where V_Z is required, an external 6.2 volt zener diode should be connected in series with V_{OUT} .

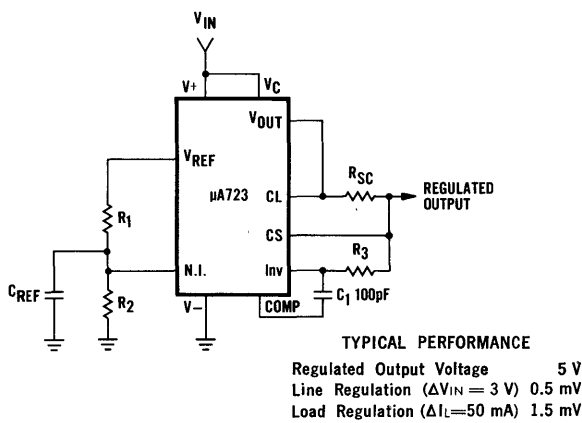
TABLE I
RESISTOR VALUES (k Ω) FOR STANDARD OUTPUT VOLTAGES

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES (Note 4)	FIXED OUTPUT $\pm 5\%$		OUTPUT ADJUSTABLE $\pm 10\%$ (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT $\pm 5\%$		5% OUTPUT ADJUSTABLE $\pm 10\%$		
		R ₁	R ₂	R ₁	P ₁	R ₂			R ₁	R ₂	R ₁	P ₁	R ₂
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	-6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	-9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	.75	1.0	2.7	-12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	-15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	-28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	-45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	-100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	-250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)] $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts [Figure 7] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]; R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)] $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Outputs from -6 to -250 volts [Figures 3, 8, 10] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]; R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT} R_3}{R_{sc} R_4} + \frac{V_{SENSE} (R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

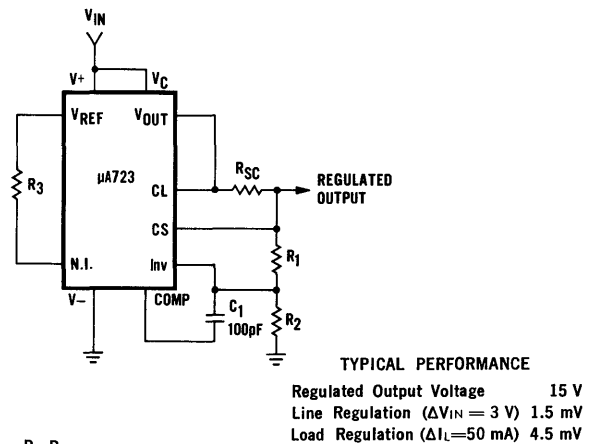
BASIC LOW VOLTAGE REGULATOR
(V_{OUT} = 2 to 7 Volts)



Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

Fig. 1

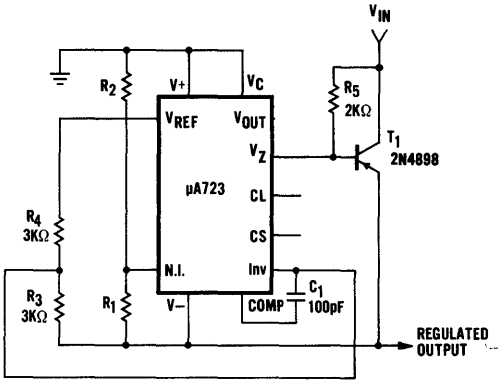
BASIC HIGH VOLTAGE REGULATOR
(V_{OUT} = 7 to 37 Volts)



Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.
 R₃ may be eliminated for minimum component count.

Fig. 2

NEGATIVE VOLTAGE REGULATOR

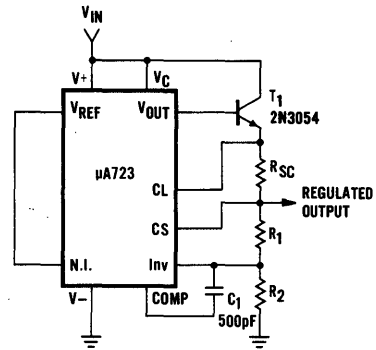


TYPICAL PERFORMANCE
 Regulated Output Voltage -15 V
 Line Regulation ($\Delta V_{IN} = 3$ V) 1 mV
 Load Regulation ($\Delta I_L = 100$ mA) 2 mV

Note 7

Fig. 3

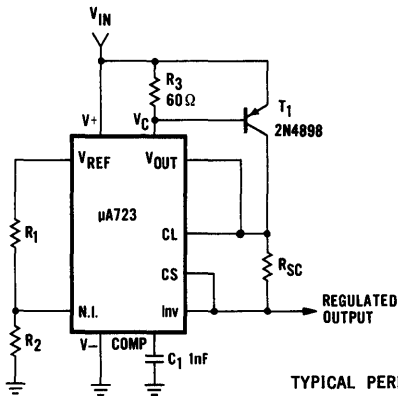
**POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)**



TYPICAL PERFORMANCE
 Regulated Output Voltage +15 V
 Line Regulation ($\Delta V_{IN} = 3$ V) 1.5 mV
 Load Regulation ($\Delta I_L = 1$ A) 15 mV

Fig. 4

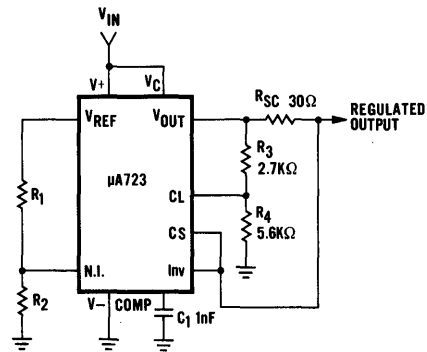
**POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)**



TYPICAL PERFORMANCE
 Regulated Output Voltage +5 V
 Line Regulation ($\Delta V_{IN} = 3$ V) 0.5 mV
 Load Regulation ($\Delta I_L = 1$ A) 5 mV

Fig. 5

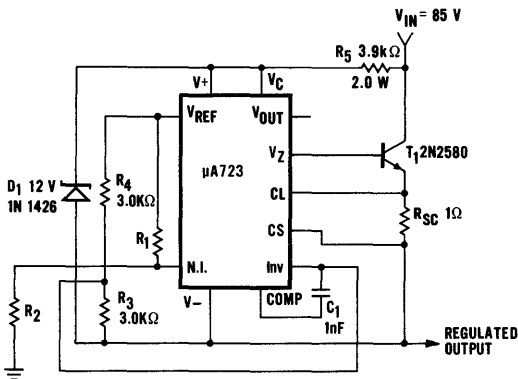
FOLDBACK CURRENT LIMITING



TYPICAL PERFORMANCE
 Regulated Output Voltage +5 V
 Line Regulation ($\Delta V_{IN} = 3$ V) 0.5 mV
 Load Regulation ($\Delta I_L = 10$ mA) 1 mV
 Short Circuit Current 20 mA

Fig. 6

POSITIVE FLOATING REGULATOR

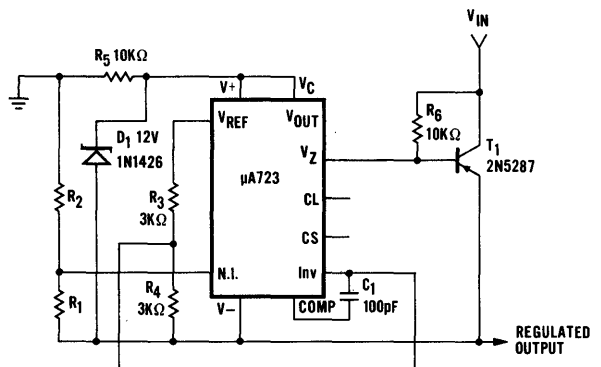


TYPICAL PERFORMANCE
 Regulated Output Voltage +50 V
 Line Regulation ($\Delta V_{IN} = 20$ V) 15 mV
 Load Regulation ($\Delta I_L = 50$ mA) 20 mV

Note 7

Fig. 7

NEGATIVE FLOATING REGULATOR

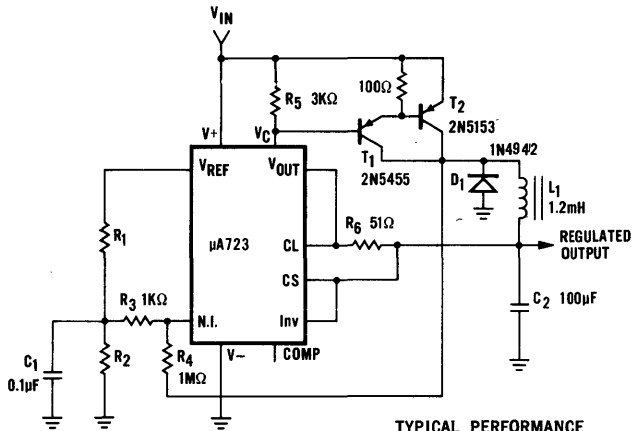


TYPICAL PERFORMANCE
 Regulated Output Voltage -100 V
 Line Regulation ($\Delta V_{IN} = 20$ V) 30 mV
 Load Regulation ($\Delta I_L = 100$ mA) 20 mV

Note 7

Fig. 8

POSITIVE SWITCHING REGULATOR

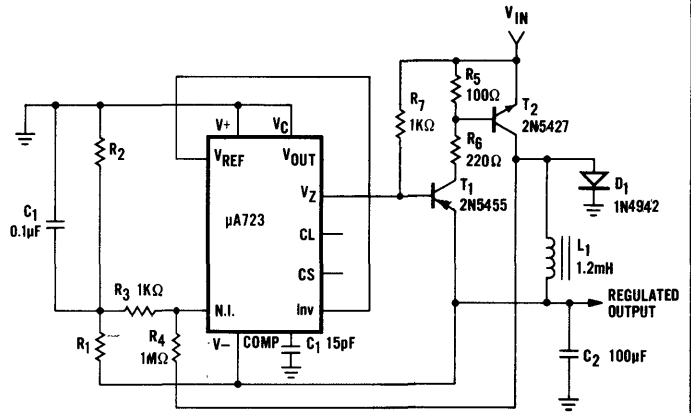


TYPICAL PERFORMANCE
 Regulated Output Voltage +5 V
 Line Regulation ($\Delta V_{IN} = 30$ V) 10 mV
 Load Regulation ($\Delta I_L = 2$ A) 80 mV

Note 3

Fig. 9

NEGATIVE SWITCHING REGULATOR

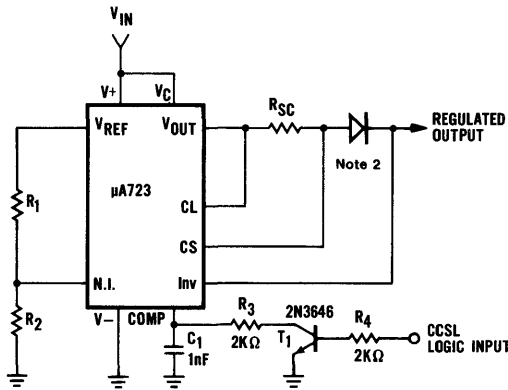


TYPICAL PERFORMANCE
 Regulated Output Voltage -15 V
 Line Regulation ($\Delta V_{IN} = 20$ V) 8 mV
 Load Regulation ($\Delta I_L = 2$ A) 6 mV

Notes 3, 7

Fig. 10

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

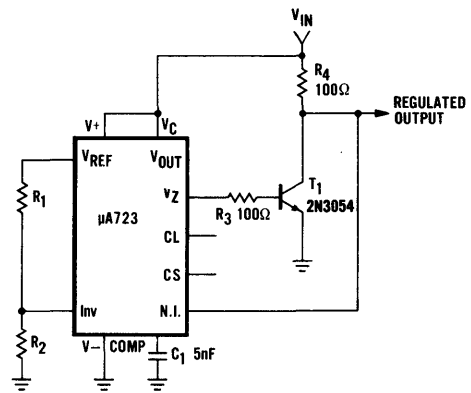


Note 1: Current limit transistor may be used for shutdown if current limiting is not required.
 2: Add if $V_{out} > 10V$

TYPICAL PERFORMANCE
 Regulated Output Voltage +5 V
 Line Regulation ($\Delta V_{IN} = 3$ V) 0.5 mV
 Load Regulation ($\Delta I_L = 50$ mA) 1.5 mV

Fig. 11

SHUNT REGULATOR



TYPICAL PERFORMANCE
 Regulated Output Voltage +5 V
 Line Regulation ($\Delta V_{IN} = 10$ V) 0.5 mV
 Load Regulation ($\Delta I_L = 100$ mA) 1.5 mV

Note 7

Fig. 12

OUTPUT VOLTAGE ADJUST

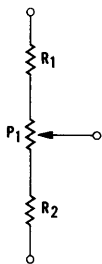
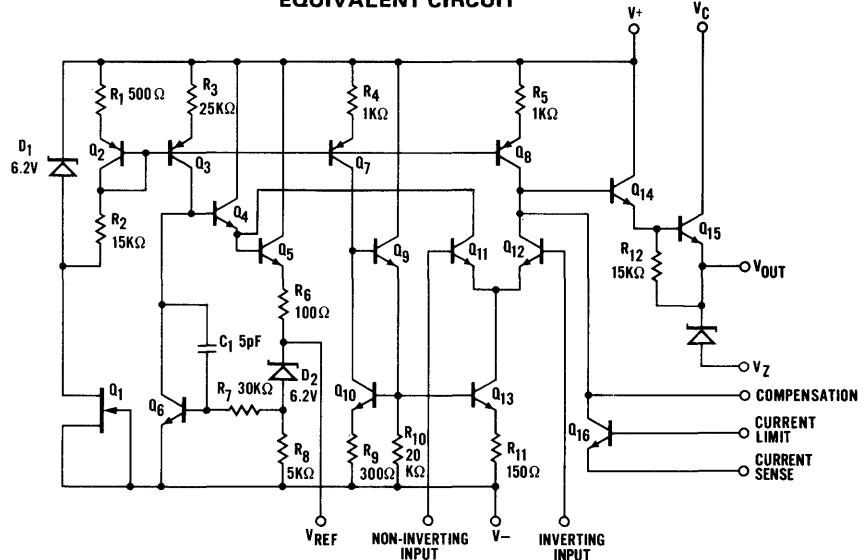


Fig. 13

EQUIVALENT CIRCUIT



μA7800 SERIES

THREE - TERMINAL POSITIVE VOLTAGE REGULATORS

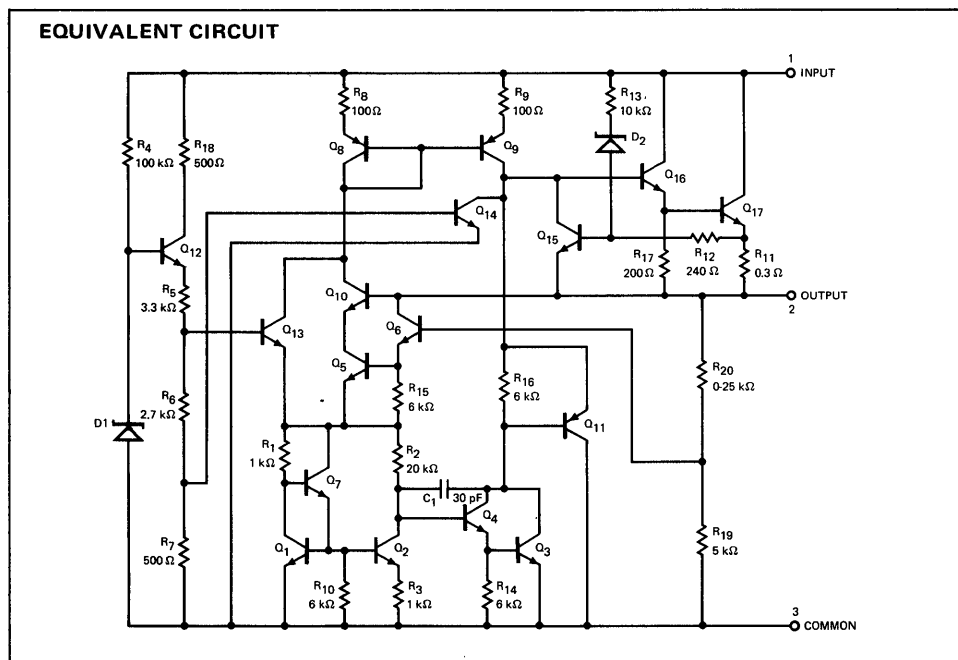
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA7800 series of monolithic Three-Terminal Positive Voltage Regulators is constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

- OUTPUT CURRENT IN EXCESS OF 1 AMP
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE-AREA COMPENSATION
- AVAILABLE IN THE TO-220 AND THE TO-3 PACKAGE
- OUTPUT VOLTAGES OF 5, 6, 8, 12, 15, 18, AND 24 VOLTS

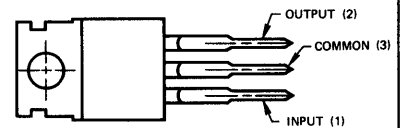
ABSOLUTE MAXIMUM RATINGS

Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range (Note 2)	7800 -55°C to +150°C
	7800C 0°C to +125°C
Lead Temperature (Soldering, 60 second time limit) TO-3 Package	300°C
(Soldering, 10 second time limit) TO-220 Package	230°C



Notes on following pages.

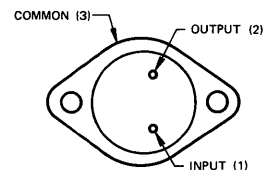
CONNECTION DIAGRAMS
TO-220 PACKAGE
 (TOP VIEW)
 PACKAGE OUTLINE GH



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	7805C	7805UC
6 V	7806C	7806UC
8 V	7808C	7808UC
12 V	7812C	7812UC
15 V	7815C	7815UC
18 V	7818C	7818UC
24 V	7824C	7824UC

TO-3 PACKAGE
 (TOP VIEW)
 PACKAGE OUTLINE GJ



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	7805	7805KM
6 V	7806	7806KM
8 V	7808	7808KM
12 V	7812	7812KM
15 V	7815	7815KM
18 V	7818	7818KM
24 V	7824	7824KM
5 V	7805C	7805KC
6 V	7806C	7806KC
8 V	7808C	7808KC
12 V	7812C	7812KC
15 V	7815C	7815KC
18 V	7818C	7818KC
24 V	7824C	7824KC

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A7800 SERIES

7805

ELECTRICAL CHARACTERISTICS ($V_{IN} = 10\text{ V}$, $I_{OUT} = 500\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Output Voltage	$T_J = 25^{\circ}\text{C}$	4.8	5.0	5.2	V	
Line Regulation	$T_J = 25^{\circ}\text{C}$	$7\text{ V} \leq V_{IN} \leq 25\text{ V}$		3	50	mV
		$8\text{ V} \leq V_{IN} \leq 12\text{ V}$		1	25	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		15	50	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		5	25	mV
Output Voltage	$8.0\text{ V} \leq V_{IN} \leq 20\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	4.65		5.35	V	
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.2	6.0	mA	
Quiescent Current Change	with line	$8\text{ V} \leq V_{IN} \leq 25\text{ V}$		0.8	mA	
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA	
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		40		μV	
Long Term Stability				20	mV	
Ripple Rejection	$f = 120\text{ Hz}$, $8\text{ V} \leq V_{IN} \leq 18\text{ V}$	68	78		dB	
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$		2.0		V	
Output Resistance	$f = 1\text{ kHz}$		17		$\text{m}\Omega$	
Short Circuit Current	$T_J = 25^{\circ}\text{C}$		750		mA	
Peak Output Current	$T_J = 25^{\circ}\text{C}$		2.2		A	
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$		-1.1		$\text{mV}/^{\circ}\text{C}$	

7805C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 10\text{ V}$, $I_{OUT} = 500\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Output Voltage	$T_J = 25^{\circ}\text{C}$	4.8	5.0	5.2	V	
Line Regulation	$T_J = 25^{\circ}\text{C}$	$7\text{ V} \leq V_{IN} \leq 25\text{ V}$		3	100	mV
		$8\text{ V} \leq V_{IN} \leq 12\text{ V}$		1	50	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		15	100	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		5	50	mV
Output Voltage	$7\text{ V} \leq V_{IN} \leq 20\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	4.75		5.25	V	
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.2	8.0	mA	
Quiescent Current Change	with line	$7\text{ V} \leq V_{IN} \leq 25\text{ V}$		1.3	mA	
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA	
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		40		μV	
Long Term Stability				20	mV	
Ripple Rejection	$f = 120\text{ Hz}$, $8\text{ V} \leq V_{IN} \leq 18\text{ V}$	62	78		dB	
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$		2.0		V	
Output Resistance	$f = 1\text{ kHz}$		17		$\text{m}\Omega$	
Short Circuit Current	$T_J = 25^{\circ}\text{C}$		750		mA	
Peak Output Current	$T_J = 25^{\circ}\text{C}$		2.2		A	
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		-1.1		$\text{mV}/^{\circ}\text{C}$	

NOTE 1: Thermal resistance of the packages (without a heat sink)

Junction to Case

TO-3 Package $4^{\circ}\text{C}/\text{W}$
TO-220 Package $2^{\circ}\text{C}/\text{W}$

Junction to Ambient

TO-3 Package $35^{\circ}\text{C}/\text{W}$
TO-220 Package $50^{\circ}\text{C}/\text{W}$

NOTE 2: Operating Ambient Temperature Range

7800 -55°C to $+125^{\circ}\text{C}$
7800C 0°C to 85°C

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A7800 SERIES

7806

ELECTRICAL CHARACTERISTICS ($V_{IN} = 11\text{ V}$, $I_{OUT} = 500\text{ mA}$, $-55^\circ\text{ C} \leq T_J \leq 150^\circ\text{ C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^\circ\text{ C}$	5.75	6.0	6.25	V
Line Regulation	$T_J = 25^\circ\text{ C}$	$8\text{ V} \leq V_{IN} \leq 25\text{ V}$	5	60	mV
		$9\text{ V} \leq V_{IN} \leq 13\text{ V}$	1.5	30	mV
Load Regulation	$T_J = 25^\circ\text{ C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$	14	60	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$	4	30	mV
Output Voltage	$9\text{ V} \leq V_{IN} \leq 21\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	5.65		6.35	V
Quiescent Current	$T_J = 25^\circ\text{ C}$		4.3	6.0	mA
Quiescent Current Change	with line	$9\text{ V} \leq V_{IN} \leq 25\text{ V}$		0.8	mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA
Output Noise Voltage	$T_A = 25^\circ\text{ C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		45		μV
Long Term Stability				24	mV
Ripple Rejection	$f = 120\text{ Hz}$, $9\text{ V} \leq V_{IN} \leq 19\text{ V}$	65	75		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^\circ\text{ C}$		2.0		V
Output Resistance	$f = 1\text{ kHz}$		19		$\text{m}\Omega$
Short Circuit Current	$T_J = 25^\circ\text{ C}$		550		mA
Peak Output Current	$T_J = 25^\circ\text{ C}$		2.2		A
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^\circ\text{ C} \leq T_J \leq 150^\circ\text{ C}$		-0.8		$\text{mV}/^\circ\text{ C}$

7806C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 11\text{ V}$, $I_{OUT} = 500\text{ mA}$, $0^\circ\text{ C} \leq T_J \leq 125^\circ\text{ C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^\circ\text{ C}$	5.75	6.0	6.25	V
Line Regulation	$T_J = 25^\circ\text{ C}$	$8\text{ V} \leq V_{IN} \leq 25\text{ V}$	5	120	mV
		$9\text{ V} \leq V_{IN} \leq 13\text{ V}$	1.5	60	mV
Load Regulation	$T_J = 25^\circ\text{ C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$	14	120	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$	4	60	mV
Output Voltage	$8\text{ V} \leq V_{IN} \leq 25\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	5.7		6.3	V
Quiescent Current	$T_J = 25^\circ\text{ C}$		4.3	8.0	mA
Quiescent Current Change	with line	$8\text{ V} \leq V_{IN} \leq 25\text{ V}$		1.3	mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA
Output Noise Voltage	$T_A = 25^\circ\text{ C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		45		μV
Long Term Stability				24	mV
Ripple Rejection	$f = 120\text{ Hz}$, $9\text{ V} \leq V_{IN} \leq 19\text{ V}$	59	75		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^\circ\text{ C}$		2.0		V
Output Resistance	$f = 1\text{ kHz}$		19		$\text{m}\Omega$
Short Circuit Current	$T_J = 25^\circ\text{ C}$		550		mA
Peak Output Current	$T_J = 25^\circ\text{ C}$		2.2		A
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^\circ\text{ C} \leq T_J \leq 125^\circ\text{ C}$		-0.8		$\text{mV}/^\circ\text{ C}$

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A7800 SERIES

7808

ELECTRICAL CHARACTERISTICS ($V_{IN} = 14\text{ V}$, $I_{OUT} = 500\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$	7.7	8.0	8.3	V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$10.5\text{ V} \leq V_{IN} \leq 25\text{ V}$	6.0	80	mV
		$11\text{ V} \leq V_{IN} \leq 17\text{ V}$	2.0	40	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$	12	80	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$	4.0	40	mV
Output Voltage	$11.5\text{ V} \leq V_{IN} \leq 23\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	7.6		8.4	V
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.3	6.0	mA
Quiescent Current Change	with line	$11.5\text{ V} \leq V_{IN} \leq 25\text{ V}$		0.8	mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $19\text{ Hz} \leq f \leq 100\text{ kHz}$		52		μV
Long Term Stability				32	mV
Ripple Rejection	$f = 120\text{ Hz}$, $11.5\text{ V} \leq V_{IN} \leq 21.5\text{ V}$	62	72		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$		2.0		V
Output Resistance	$f = 1\text{ kHz}$		16		$\text{m}\Omega$
Short Circuit Current	$T_J = 25^{\circ}\text{C}$		450		mA
Peak Output Current	$T_J = 25^{\circ}\text{C}$		2.2		A
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$		-0.8		$\text{mV}/^{\circ}\text{C}$

7808C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 14\text{ V}$, $I_{OUT} = 500\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$	7.7	8.0	8.3	V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$10.5\text{ V} \leq V_{IN} \leq 25\text{ V}$	6.0	160	mV
		$11\text{ V} \leq V_{IN} \leq 17\text{ V}$	2.0	80	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$	12	160	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$	4.0	80	mV
Output Voltage	$10.5\text{ V} \leq V_{IN} \leq 23\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	7.6		8.4	V
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.3	8.0	mA
Quiescent Current Change	with line	$10.5\text{ V} \leq V_{IN} \leq 25\text{ V}$		1.0	mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		52		μV
Long Term Stability				32	mV
Ripple Rejection	$f = 120\text{ Hz}$, $11.5\text{ V} \leq V_{IN} \leq 21.5\text{ V}$	56	72		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$		2.0		V
Output Resistance	$f = 1\text{ kHz}$		16		$\text{m}\Omega$
Short Circuit Current	$T_J = 25^{\circ}\text{C}$		450		mA
Peak Output Current	$T_J = 25^{\circ}\text{C}$		2.2		A
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		-0.8		$\text{mV}/^{\circ}\text{C}$

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A7800 SERIES

7812

ELECTRICAL CHARACTERISTICS ($V_{IN} = 19\text{ V}$, $I_{OUT} = 500\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$		11.5	12.0	12.5	V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$14.5\text{ V} \leq V_{IN} \leq 30\text{ V}$		10	120	mV
		$16\text{ V} \leq V_{IN} \leq 22\text{ V}$		3.0	60	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		12	120	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		4.0	60	mV
Output Voltage	$15.5\text{ V} \leq V_{IN} \leq 27\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$		11.4		12.6	V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.3	6.0	mA
Quiescent Current Change	with line	$15\text{ V} \leq V_{IN} \leq 30\text{ V}$			0.8	mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$			0.5	mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$			75		μV
Long Term Stability					48	mV
Ripple Rejection	$f = 120\text{ Hz}$, $15\text{ V} \leq V_{IN} \leq 25\text{ V}$		61	71		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$			2.0		V
Output Resistance	$f = 1\text{ kHz}$			18		$\text{m}\Omega$
Short Circuit Current	$T_J = 25^{\circ}\text{C}$			350		mA
Peak Output Current	$T_J = 25^{\circ}\text{C}$			2.2		A
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$			-1.0		$\text{mV}/^{\circ}\text{C}$

7812C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 19\text{ V}$, $I_{OUT} = 500\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$		11.5	12.0	12.5	V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$14.5\text{ V} \leq V_{IN} \leq 30\text{ V}$		10	240	mV
		$16\text{ V} \leq V_{IN} \leq 22\text{ V}$		3.0	120	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		12	240	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		4.0	120	mV
Output Voltage	$14.5\text{ V} \leq V_{IN} \leq 27\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$		11.4		12.6	V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.3	8.0	mA
Quiescent Current Change	with line	$14.5\text{ V} \leq V_{IN} \leq 30\text{ V}$			1.0	mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$			0.5	mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$			75		μV
Long Term Stability					48	mV
Ripple Rejection	$f = 120\text{ Hz}$, $15\text{ V} \leq V_{IN} \leq 25\text{ V}$		55	71		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$			2.0		V
Output Resistance	$f = 1\text{ kHz}$			18		$\text{m}\Omega$
Short Circuit Current	$T_J = 25^{\circ}\text{C}$			350		mA
Peak Output Current	$T_J = 25^{\circ}\text{C}$			2.2		A
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$			-1.0		$\text{mV}/^{\circ}\text{C}$

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A7800 SERIES

7815

ELECTRICAL CHARACTERISTICS ($V_{IN} = 23\text{ V}$, $I_{OUT} = 500\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Output Voltage	$T_J = 25^{\circ}\text{C}$	14.4	15.0	15.6	V	
Line Regulation	$T_J = 25^{\circ}\text{C}$	$17.5\text{ V} \leq V_{IN} \leq 30\text{ V}$		11	150	mV
		$20\text{ V} \leq V_{IN} \leq 26\text{ V}$		3	75	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		12	150	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		4	75	mV
Output Voltage	$18.5\text{ V} \leq V_{IN} \leq 30\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	14.25		15.75	V	
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.4	6.0	mA	
Quiescent Current Change	with line	$18.5\text{ V} \leq V_{IN} \leq 30\text{ V}$		0.8	mA	
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA	
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		90		μV	
Long Term Stability				60	mV	
Ripple Rejection	$f = 120\text{ Hz}$, $18.5\text{ V} \leq V_{IN} \leq 28.5\text{ V}$	60	70		dB	
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$		2.0		V	
Output Resistance	$f = 1\text{ kHz}$		19		$\text{m}\Omega$	
Short Circuit Current	$T_J = 25^{\circ}\text{C}$		230		mA	
Peak Output Current	$T_J = 25^{\circ}\text{C}$		2.1		A	
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$		-1.0		$\text{mV}/^{\circ}\text{C}$	

7815C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 23\text{ V}$, $I_{OUT} = 500\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Output Voltage	$T_J = 25^{\circ}\text{C}$	14.4	15.0	15.6	V	
Line Regulation	$T_J = 25^{\circ}\text{C}$	$17.5\text{ V} \leq V_{IN} \leq 30\text{ V}$		11	300	mV
		$20\text{ V} \leq V_{IN} \leq 26\text{ V}$		3	150	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		12	150	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		4	75	mV
Output Voltage	$17.5\text{ V} \leq V_{IN} \leq 30\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	14.25		15.75	V	
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.4	8.0	mA	
Quiescent Current Change	with line	$17.5\text{ V} \leq V_{IN} \leq 30\text{ V}$		1.0	mA	
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA	
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		90		μV	
Long Term Stability				60	mV	
Ripple Rejection	$f = 120\text{ Hz}$, $18.5\text{ V} \leq V_{IN} \leq 28.5\text{ V}$	54	70		dB	
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$		2.0		V	
Output Resistance	$f = 1\text{ kHz}$		19		$\text{m}\Omega$	
Short Circuit Current	$T_J = 25^{\circ}\text{C}$		230		mA	
Peak Output Current	$T_J = 25^{\circ}\text{C}$		2.1		A	
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		-1.0		$\text{mV}/^{\circ}\text{C}$	

5

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A7800 SERIES

7818

ELECTRICAL CHARACTERISTICS ($V_{IN} = 27\text{ V}$, $I_{OUT} = 500\text{ mA}$, $-55^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Output Voltage	$T_J = 25^{\circ}\text{C}$	17.3	18.0	18.7	V	
Line Regulation	$T_J = 25^{\circ}\text{C}$	$21\text{ V} \leq V_{IN} \leq 33\text{ V}$		15	180	mV
		$24\text{ V} \leq V_{IN} \leq 30\text{ V}$		5.0	90	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		12	180	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		4.0	90	mV
Output Voltage	$22\text{ V} \leq V_{IN} \leq 33\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	17.1		18.9	V	
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.5	6.0	mA	
Quiescent Current Change	with line	$22\text{ V} \leq V_{IN} \leq 33\text{ V}$		0.8	mA	
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA	
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		110		μV	
Long Term Stability				72	mV	
Ripple Rejection	$f = 120\text{ Hz}$, $22\text{ V} \leq V_{IN} \leq 32\text{ V}$	59	69		dB	
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$		2.0		V	
Output Resistance	$f = 1\text{ kHz}$		22		$\text{m}\Omega$	
Short Circuit Current	$T_J = 25^{\circ}\text{C}$		200		mA	
Peak Output Current	$T_J = 25^{\circ}\text{C}$		2.1		A	
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$		-1.0		$\text{mV}/^{\circ}\text{C}$	

7818C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 27\text{ V}$, $I_{OUT} = 500\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Output Voltage	$T_J = 25^{\circ}\text{C}$	17.3	18.0	18.7	V	
Line Regulation	$T_J = 25^{\circ}\text{C}$	$21\text{ V} \leq V_{IN} \leq 33\text{ V}$		15	360	mV
		$24\text{ V} \leq V_{IN} \leq 30\text{ V}$		5.0	180	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		12	360	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		4.0	180	mV
Output Voltage	$21\text{ V} \leq V_{IN} \leq 33\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$	17.1		18.9	V	
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.5	8.0	mA	
Quiescent Current Change	with line	$21\text{ V} \leq V_{IN} \leq 33\text{ V}$		1.0	mA	
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA	
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		110		μV	
Long Term Stability				72	mV	
Ripple Rejection	$f = 120\text{ Hz}$, $22 \leq V_{IN} \leq 32\text{ V}$	53	69		dB	
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$		2.0		V	
Output Resistance	$f = 1\text{ kHz}$		22		$\text{m}\Omega$	
Short Circuit Current	$T_J = 25^{\circ}\text{C}$		200		mA	
Peak Output Current	$T_J = 25^{\circ}\text{C}$		2.1		A	
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		-1.0		$\text{mV}/^{\circ}\text{C}$	

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A7800 SERIES

7824

ELECTRICAL CHARACTERISTICS ($V_{IN} = 33\text{ V}$, $I_{OUT} = 500\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$		23.0	24.0	25.0	V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$27\text{ V} \leq V_{IN} \leq 38\text{ V}$		18	240	mV
		$30\text{ V} \leq V_{IN} \leq 36\text{ V}$		6	120	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		12	240	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		4	120	mV
Output Voltage	$28\text{ V} \leq V_{IN} \leq 38\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$		22.8		25.2	V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.6	6.0	mA
Quiescent Current Change	with line	$28\text{ V} \leq V_{IN} \leq 38\text{ V}$			0.8	mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$			0.5	mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$			170		μV
Long Term Stability					96	mV
Ripple Rejection	$f = 120\text{ Hz}$, $28\text{ V} \leq V_{IN} \leq 38\text{ V}$		56	66		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$			2.0		V
Output Resistance	$f = 1\text{ kHz}$			28		$\text{m}\Omega$
Short Circuit Current	$T_J = 25^{\circ}\text{C}$			150		mA
Peak Output Current	$T_J = 25^{\circ}\text{C}$			2.1		A
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$			-1.5		$\text{mV}/^{\circ}\text{C}$

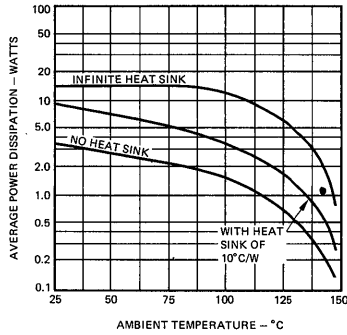
7824C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 33\text{ V}$, $I_{OUT} = 500\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, unless otherwise specified)

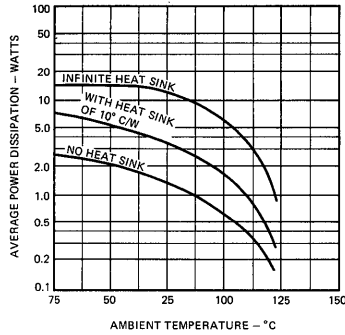
PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$		23.0	24.0	25.0	V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$27\text{ V} \leq V_{IN} \leq 38\text{ V}$		18	480	mV
		$30\text{ V} \leq V_{IN} \leq 36\text{ V}$		6	240	mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		12	480	mV
		$250\text{ mA} \leq I_{OUT} \leq 750\text{ mA}$		4	240	mV
Output Voltage	$27\text{ V} \leq V_{IN} \leq 38\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 15\text{ W}$		22.8		25.2	V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.6	8.0	mA
Quiescent Current Change	with line	$27\text{ V} \leq V_{IN} \leq 38\text{ V}$			1.0	mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$			0.5	mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$			170		μV
Long Term Stability					96	mV
Ripple Rejection	$f = 120\text{ Hz}$, $28\text{ V} \leq V_{IN} \leq 38\text{ V}$		50	66		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$			2.0		V
Output Resistance	$f = 1\text{ kHz}$			28		$\text{m}\Omega$
Short Circuit Current	$T_J = 25^{\circ}\text{C}$			150		mA
Peak Output Current	$T_J = 25^{\circ}\text{C}$			2.1		A
Average Temperature Coefficient of Output Voltage	$I_{OUT} = 5\text{ mA}$, $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$			-1.5		$\text{mV}/^{\circ}\text{C}$

TYPICAL PERFORMANCE CURVES FOR 7800 SERIES

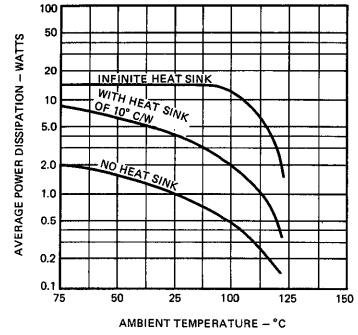
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 7800)



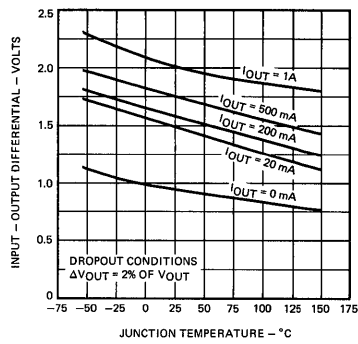
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 7800C)



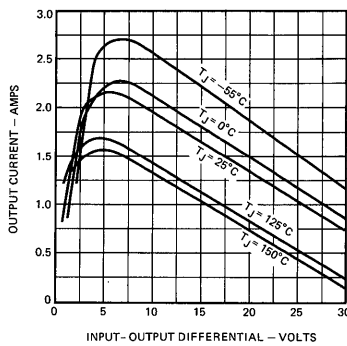
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 7800C)



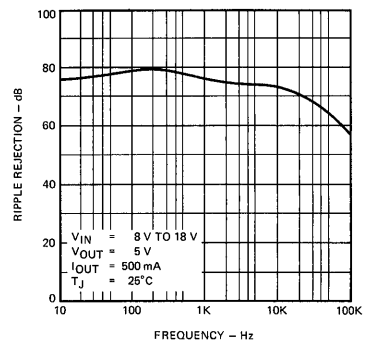
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



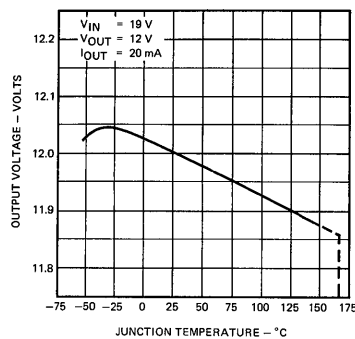
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



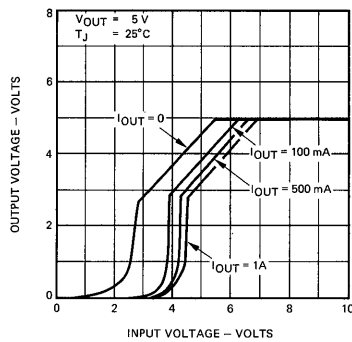
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



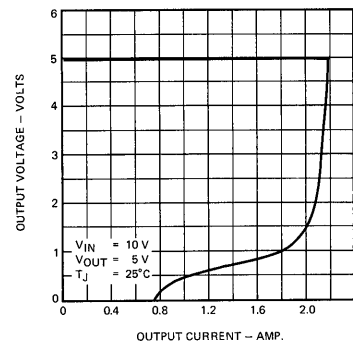
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



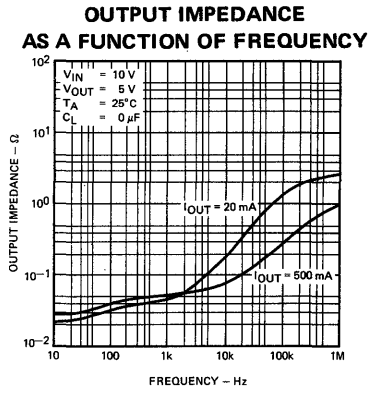
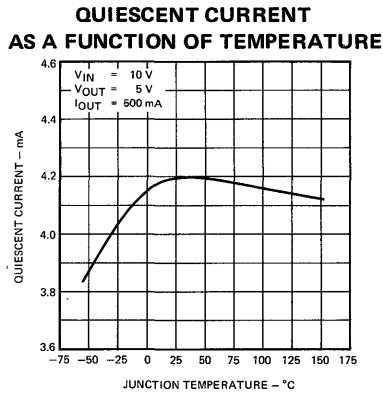
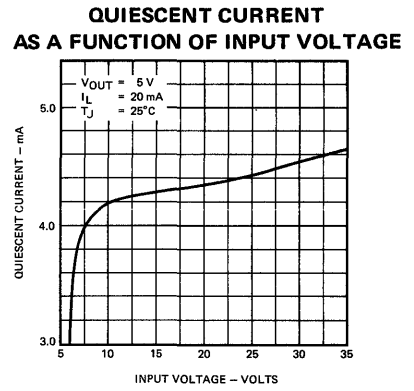
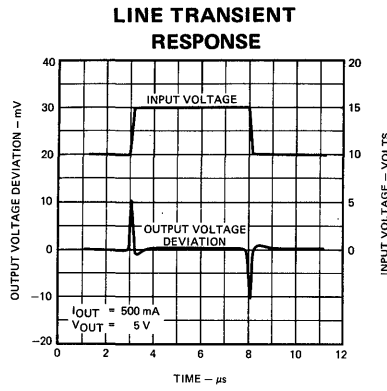
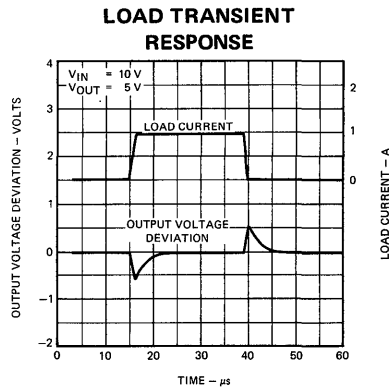
DROPOUT CHARACTERISTICS



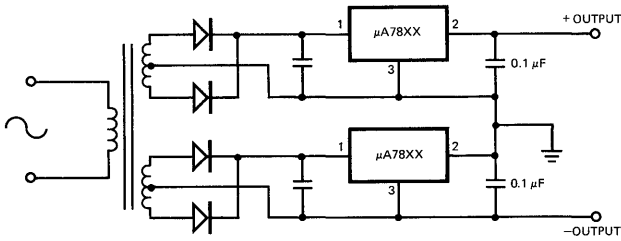
CURRENT LIMITING CHARACTERISTICS



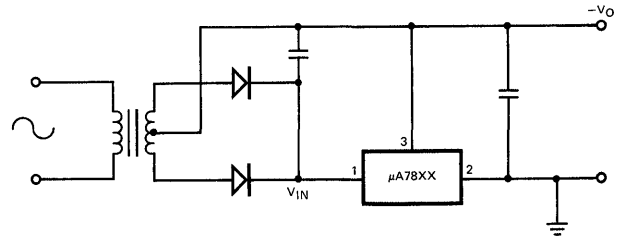
TYPICAL PERFORMANCE CURVES FOR 7800 SERIES (cont'd)



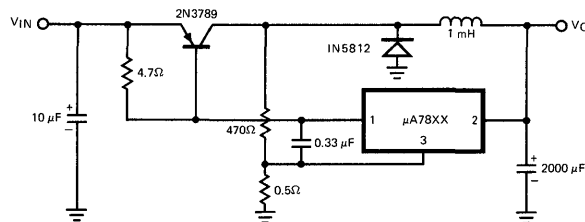
APPLICATIONS



POSITIVE AND NEGATIVE REGULATOR

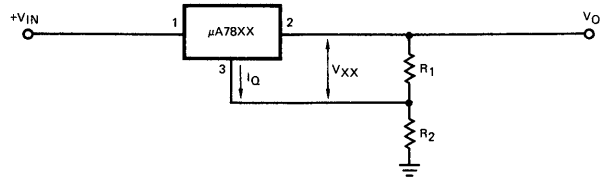
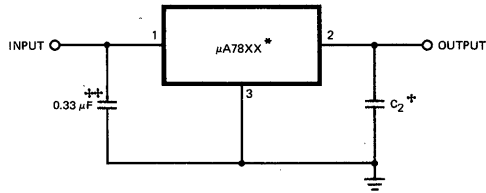


NEGATIVE OUTPUT VOLTAGE CIRCUIT



SWITCHING REGULATOR

APPLICATIONS (Cont'd)

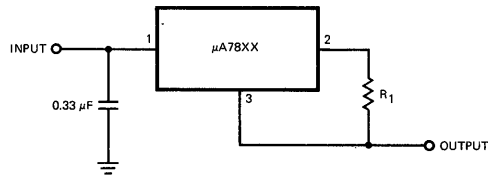


$$V_0 = V_{XX} \left(1 + \frac{R_2}{R_1}\right) + I_Q R_2$$

NOTES:

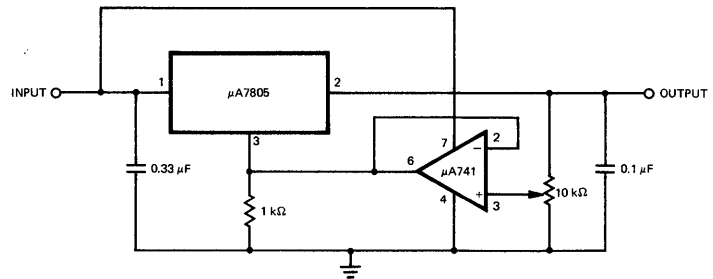
- * To specify an output voltage, substitute voltage value for "XX".
- + Although no output capacitor is needed for stability, it does improve transient response.
- ++ Required if regulator is located an appreciable distance from power supply filter.

FIXED OUTPUT REGULATOR

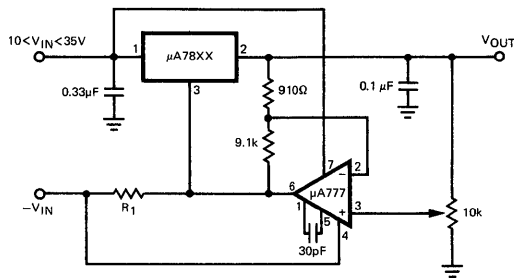


$$\text{Output Current} = \frac{V_{OUT}}{R_1}$$

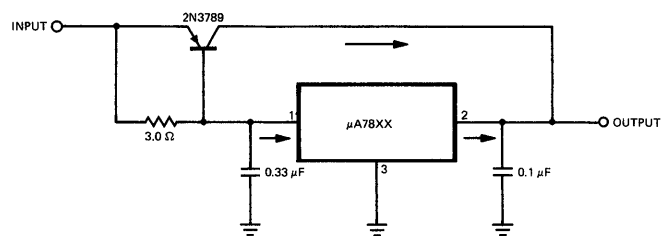
CIRCUIT FOR INCREASING OUTPUT VOLTAGE



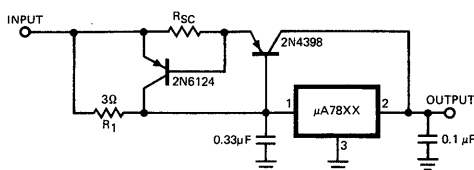
CURRENT REGULATOR



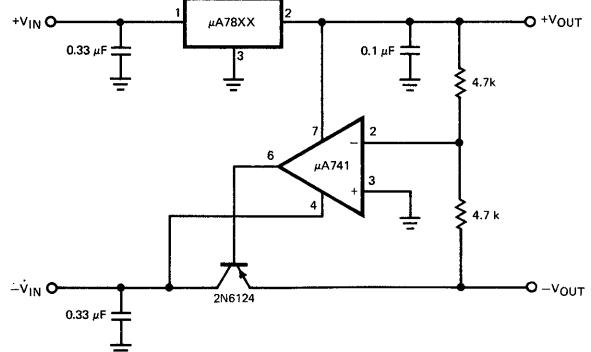
ADJUSTABLE OUTPUT REGULATOR, 7 to 30 VOLTS



VARIABLE OUTPUT VOLTAGE, 0.5 to 7 VOLTS



HIGH CURRENT VOLTAGE REGULATOR



HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED

± TRACKING VOLTAGE REGULATOR

104•304

NEGATIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

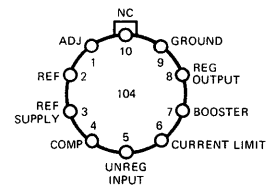
GENERAL DESCRIPTION — The 104 family of Precision Negative Voltage Regulators is constructed using the Fairchild Planar* epitaxial process. This device can be programmed by a single external resistor to supply any voltage from 0 V to 30 V from a single unregulated supply. When used with a separate floating bias supply, the 104/304 can provide 0.01% regulation with the output voltage limited only by the breakdown of external pass transistors. The 104 and 304 provide complementary operation with the 105 positive regulator family. Although primarily designed as a linear series regulator, the 104 family can be used as a current regulator, switching regulator, or in control applications. Without external pass elements, the device can supply currents up to 25 mA; with external pass transistors, the output current is limited only by the capacity of the pass transistors. External resistors establish the output voltage and either constant or fold-back current limiting.

- 1 mV REGULATION WITH FULL LOAD
- 0.01%/V LINE REGULATION
- 0.2 mV/V RIPPLE REJECTION
- 0.3% TEMPERATURE STABILITY OVER FULL TEMPERATURE RANGE

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
104	50 V
304	40 V
Input/Output Voltage Differential	
104	50 V
304	40 V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Military grade (104)	-55°C to +125°C
Commercial grade (304)	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

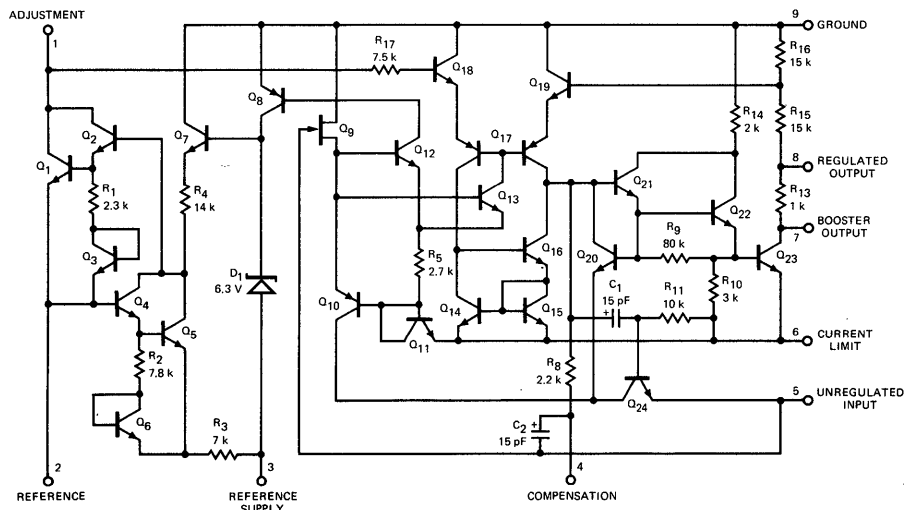
CONNECTION DIAGRAM
10-LEAD METAL CAN
 (TOP VIEW)
PACKAGE OUTLINE 5F



Note: Pin 5 connected to case.

ORDER INFORMATION	
TYPE	PART NO.
104	LM104H
304	LM304H

EQUIVALENT CIRCUIT



104

ELECTRICAL CHARACTERISTICS ($V_{IN} = -50\text{ V to } -8.0\text{ V}$, $T_A = -55^\circ\text{C to } 125^\circ\text{C}$, unless otherwise specified), Note 2.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		-50		-8.0	V
Output Voltage Range		-40		-0.015	V
Output/Input Voltage Differential (Note 3)	$I_{OUT} = 20\text{ mA}$	2.0		50	V
	$I_{OUT} = 5\text{ mA}$	0.5		50	V
Load Regulation (Note 4)	$0 \leq I_{OUT} \leq 20\text{ mA}$, $R_{SC} = 15\ \Omega$		1.0	5.0	mV
Line Regulation (Note 5)	$V_{OUT} \leq -5\text{ V}$, $\Delta V_{IN} = 0.1\text{ V}_{IN}$		0.056	0.1	%
Ripple Rejection	$C_{19} = 10\ \mu\text{F}$, $f = 120\text{ Hz}$, $V_{IN} \geq -15\text{ V}$		0.2	0.5	mV/V
	$-7\text{ V} \geq V_{IN} \geq -15\text{ V}$		0.5	1.0	mV/V
Output Voltage Scale Factor	$R_{23} = 2.4\text{ k}\Omega$	1.8	2.0	2.2	V/k Ω
Temperature Stability	$V_{OUT} \leq -1\text{ V}$, $-55\text{ C} \leq T_A \leq 125^\circ\text{C}$		0.3	1.0	%
Output Noise Voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$, $V_{OUT} \leq -5\text{ V}$, $C_{19} = 0$		0.007		%
	$C_{19} = 10\ \mu\text{F}$		15		μV
Standby Current Drain	$I_L = 5\text{ mA}$, $V_{OUT} = 0$		1.7	2.5	mA
	$V_{OUT} = -40\text{ V}$		3.6	5.0	mA
Long Term Stability	$V_{OUT} \leq -1\text{ V}$		0.1	1.0	%

304

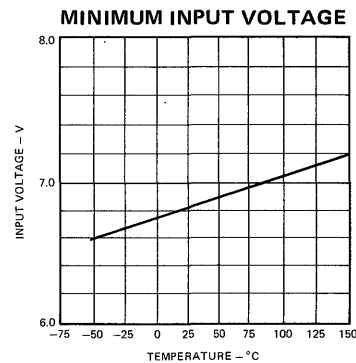
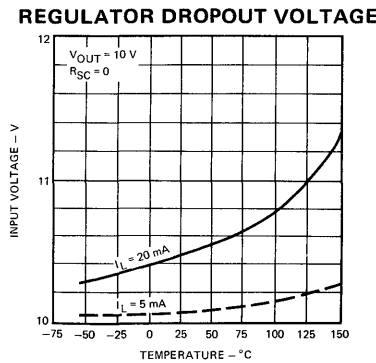
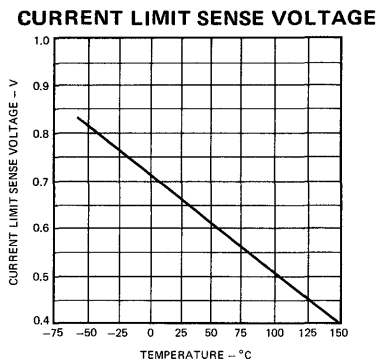
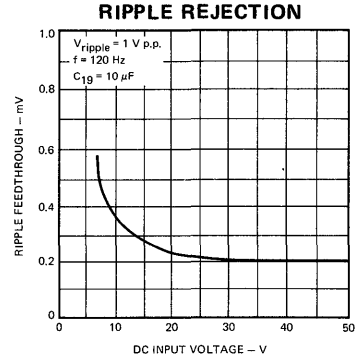
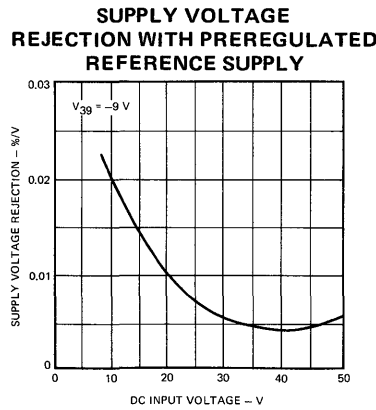
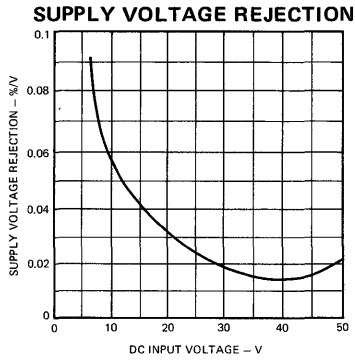
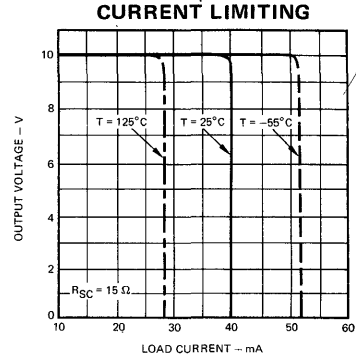
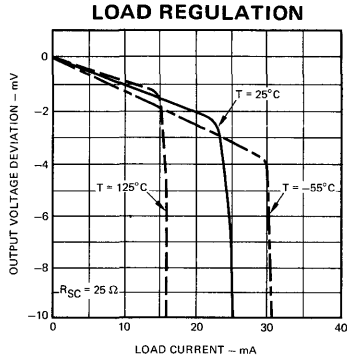
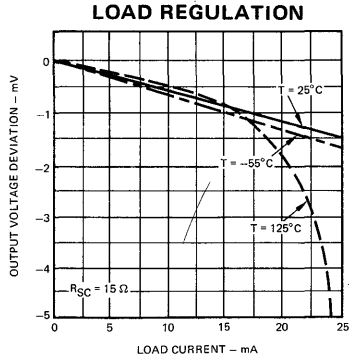
ELECTRICAL CHARACTERISTICS ($V_{IN} = -40\text{ V to } -8.0\text{ V}$, $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, unless otherwise specified), Note 2.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		-40		-8.0	V
Output Voltage Range		-30		-0.035	V
Output/Input Voltage Differential (Note 3)	$I_{OUT} = 20\text{ mA}$	2.0		40	V
	$I_{OUT} = 5\text{ mA}$	0.5		40	V
Load Regulation (Note 4)	$0 \leq I_{OUT} \leq 20\text{ mA}$, $R_{SC} = 15\ \Omega$		1.0	5.0	mV
Line Regulation (Note 5)	$V_{OUT} \leq -5\text{ V}$, $\Delta V_{IN} = 0.1\text{ V}_{IN}$		0.056	0.1	%
Ripple Rejection	$C_{19} = 10\ \mu\text{F}$, $f = 120\text{ Hz}$, $V_{IN} < -15\text{ V}$		0.2	0.5	mV/V
	$-7\text{ V} \geq V_{IN} \geq -15\text{ V}$		0.5	1.0	mV/V
Output Voltage Scale Factor	$R_{23} = 2.4\text{ k}\Omega$	1.8	2.0	2.2	V/k Ω
Temperature Stability	$V_{OUT} \leq -1\text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.3	1.0	%
Output Noise Voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$, $V_{OUT} \leq -5\text{ V}$, $C_{19} = 0$		0.007		%
	$C_{19} = 10\ \mu\text{F}$		15		μV
Standby Current Drain	$I_L = 5\text{ mA}$, $V_{OUT} = 0$		1.7	2.5	mA
	$V_{OUT} = -30\text{ V}$		3.6	5.0	mA
Long Term Stability	$V_{OUT} \leq -1\text{ V}$		0.1	1.0	%

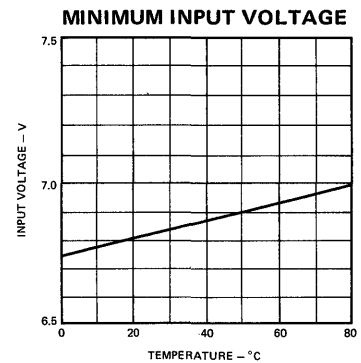
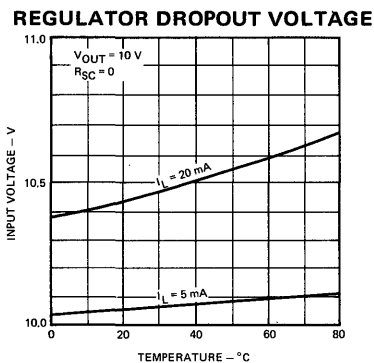
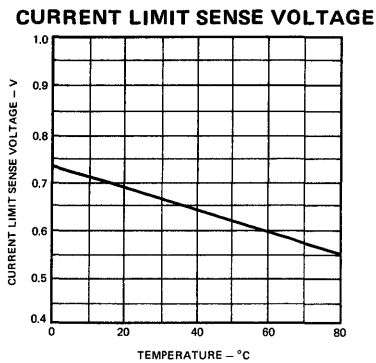
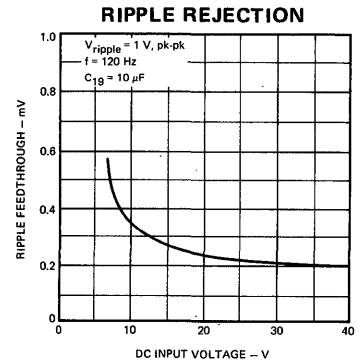
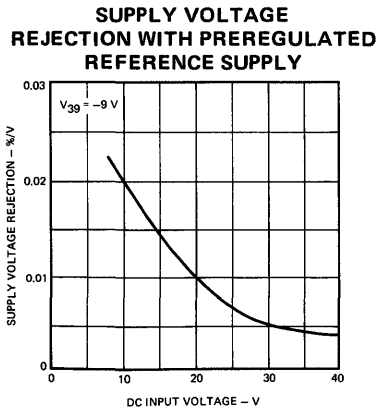
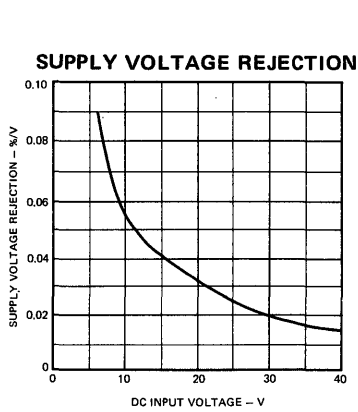
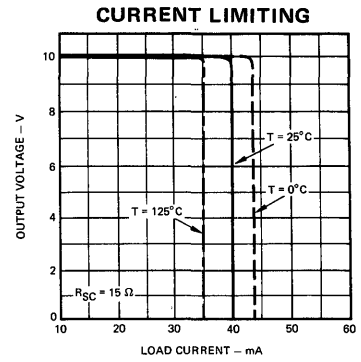
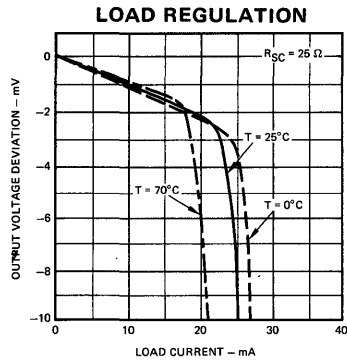
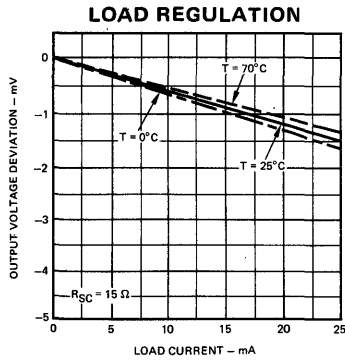
NOTES:

- Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3\text{ mW}/^\circ\text{C}$.
- The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
- When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1 V .
- The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
- With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0 V and -5 V , a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

TYPICAL PERFORMANCE CURVES FOR 104

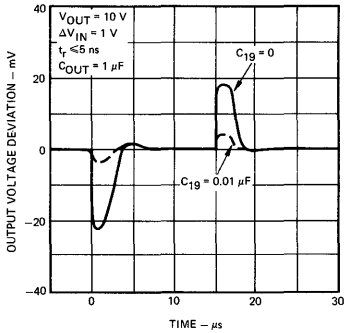


TYPICAL PERFORMANCE CURVES FOR 304

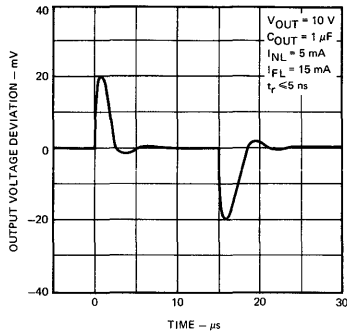


TYPICAL PERFORMANCE CURVES FOR 104 AND 304

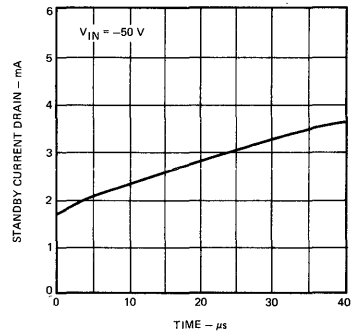
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE

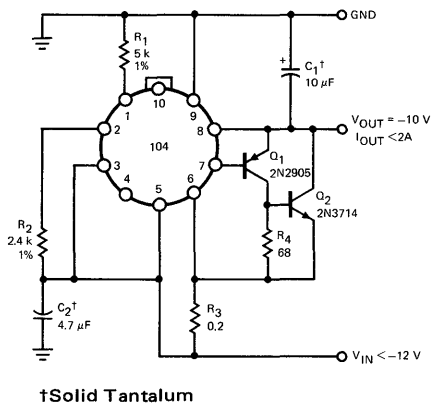


STANDBY CURRENT DRAIN



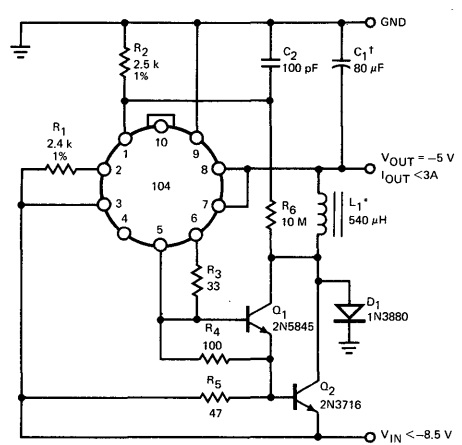
TYPICAL APPLICATIONS

HIGH CURRENT REGULATOR



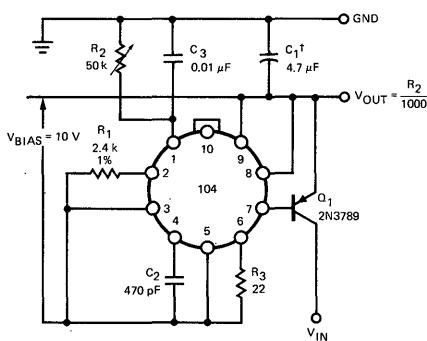
†Solid Tantalum

SWITCHING REGULATOR



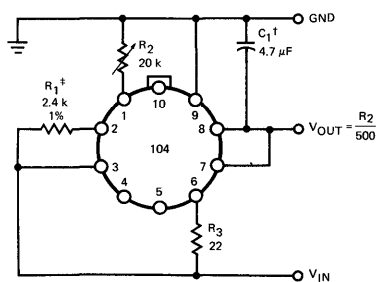
†Solid Tantalum
*60 Turns #20
on Arnold
Engineering
A930157-2
Molybdenum
Permalloy Core.

OPERATING WITH SEPARATE BIAS SUPPLY



†Solid Tantalum

BASIC REGULATOR CIRCUIT



†Solid Tantalum
‡Trim R_1 for exact
scale factor

105•305•305A•376

VOLTAGE REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

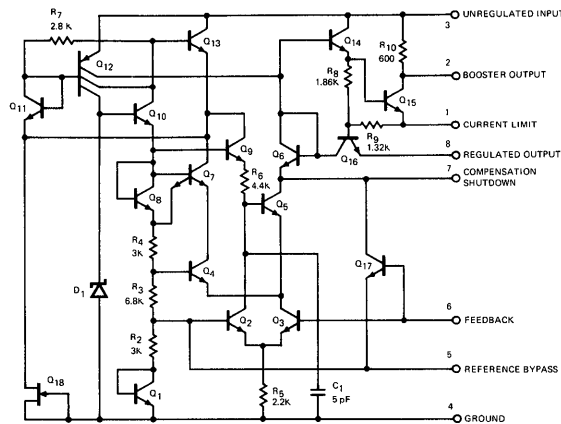
GENERAL DESCRIPTION — The 105/305/305A/376 are monolithic Positive Voltage Regulators constructed using the Fairchild Planar* epitaxial process. Applications for these devices include both linear and switching regulator circuits with output voltages greater than 4.5 V. These devices will not oscillate when confronted with varying resistive and reactive loads and will start reliably regardless of the load within the ratings of the circuit. They also feature fast response to both load and line transients. Used independently, the 105/305/305A will supply 45 mA and the 376, 25 mA. The 105 is specified for the military temperature range (-55°C to $+125^{\circ}\text{C}$) and the 305/376/305A are specified for 0°C to $+70^{\circ}\text{C}$ operation. The 105/305/305A are in an 8-lead TO-5 package and the 376 is available in the space and cost saving mini DIP.

- **LOW STANDBY CURRENT DRAIN**
- **ADJUSTABLE OUTPUT VOLTAGE FROM 4.5 V TO 40 V**
- **HIGH OUTPUT CURRENTS EXCEEDING 10A WITH EXTERNAL COMPONENTS**
- **LOAD REGULATION BETTER THAN 0.1%, FULL LOAD WITH CURRENT LIMITING**
- **DC LINE REGULATION GUARANTEED AT 0.03%/V**
- **RIPPLE REJECTION OF 0.01%/V**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
105, 305A	50 V
305, 376	40 V
Input/Output Voltage Differential	40 V
Internal Power Dissipation (Note 1)	
105, 305, 305A	500 mW
376	450 mW
Operating Temperature Range	
Military (105)	-55°C to $+125^{\circ}\text{C}$
Commercial (305, 305A, 376)	0°C to $+70^{\circ}\text{C}$
Storage Temperature Range	
Metal Can	-65°C to $+150^{\circ}\text{C}$
Mini DIP	-55°C to $+125^{\circ}\text{C}$
Lead Temperature	
Metal Can (Soldering, 60 seconds)	300°C
Mini DIP (Soldering, 10 seconds)	260°C

EQUIVALENT CIRCUIT

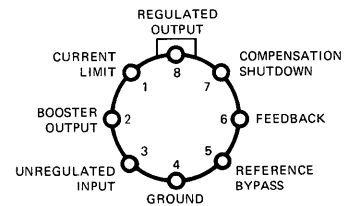


PIN CONNECTIONS SHOWN ARE FOR METAL CAN

CONNECTION DIAGRAMS

8-LEAD METAL CAN (TOP VIEW)

PACKAGE OUTLINE 5B

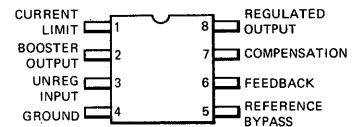


ORDER INFORMATION

TYPE	PART NO.
105	LM105H
305	LM305H
305A	LM305AH

8-LEAD MINI DIP (TOP VIEW)

PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
376	LM376N

Notes on following pages.

*Planar is a patented Fairchild process.

105

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified) Note 2

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input Voltage Range			8.5		50	V
Output Voltage Range			4.5		40	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_O \leq 12\text{ mA}$	$R_{SC} = 10\Omega, T_A = 25^\circ\text{C}$		0.02	0.05	%
		$R_{SC} = 10\Omega, T_A = 125^\circ\text{C}$		0.03	0.1	%
		$R_{SC} = 10\Omega, T_A = -55^\circ\text{C}$		0.03	0.1	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5\text{ V}$			0.025	0.06	%/V
	$V_{IN} - V_{OUT} > 5\text{ V}$			0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\ \mu\text{F}, f = 120\text{ Hz}$			0.003	0.01	%/V
Temperature Stability	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			0.3	1.0	%
Feedback Sense Voltage			1.63	1.7	1.81	V
Output Noise Voltage	$10\text{ Hz} < f \leq 10\text{ kHz}$	$C_{REF} = 0$		0.005		%
		$C_{REF} > 0.1\ \mu\text{F}$		0.002		%
Current Limit Sense Voltage	$R_{SC} = 10\Omega, T_A = 25^\circ\text{C}, V_{OUT} = 0\text{ V}$		225	300	315	mV
Standby Current Drain	$V_{IN} = 50\text{ V}$			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

305

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified) Note 2

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input Voltage Range			8.5		40	V
Output Voltage Range			4.5		30	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_O \leq 12\text{ mA}$	$R_{SC} = 10\Omega, T_A = 25^\circ\text{C}$		0.02	0.05	%
		$R_{SC} = 15\Omega, T_A = 70^\circ\text{C}$		0.03	0.1	%
		$R_{SC} = 10\Omega, T_A = 0^\circ\text{C}$		0.03	0.1	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5\text{ V}$			0.025	0.06	%/V
	$V_{IN} - V_{OUT} > 5\text{ V}$			0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\ \mu\text{F}, f = 120\text{ Hz}$			0.003	0.01	%/V
Temperature Stability	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$			0.3	1.0	%
Feedback Sense Voltage			1.63	1.7	1.81	V
Output Noise Voltage	$10\text{ Hz} < f \leq 10\text{ kHz}$	$C_{REF} = 0$		0.005		%
		$C_{REF} > 0.1\ \mu\text{F}$		0.002		%
Current Limit Sense Voltage	$R_{SC} = 10\Omega, T_A = 25^\circ\text{C}, V_{OUT} = 0\text{ V}$		225	300	315	mV
Standby Current Drain	$V_{IN} = 40\text{ V}$			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

NOTES

1. Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3\text{ mW}/^\circ\text{C}$ for the metal can and $5.6\text{ mW}/^\circ\text{C}$ for the mini Dip.
2. These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of $2\text{ k}\Omega$, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. With no external pass transistor.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 105 • 305 • 305A • 376

305A

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified) Note 2

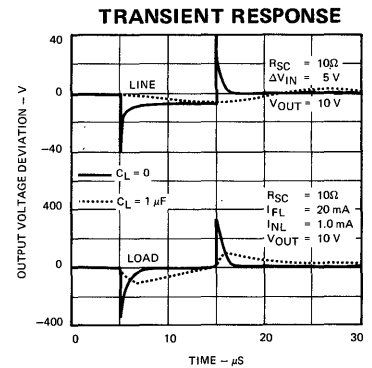
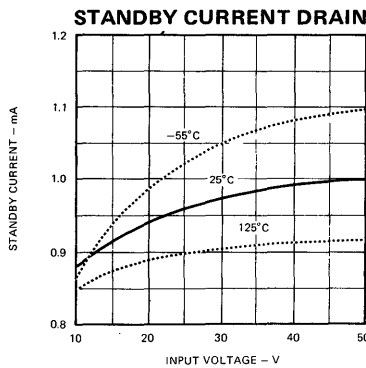
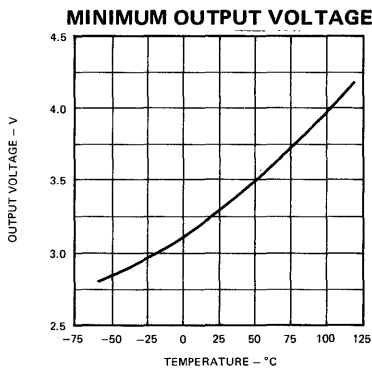
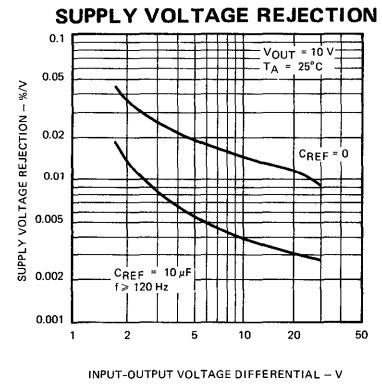
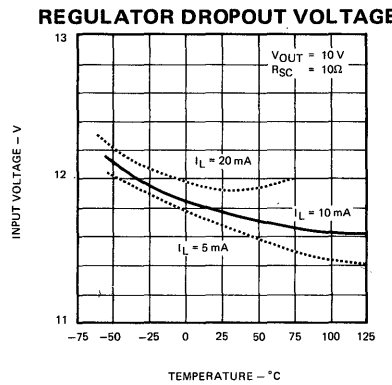
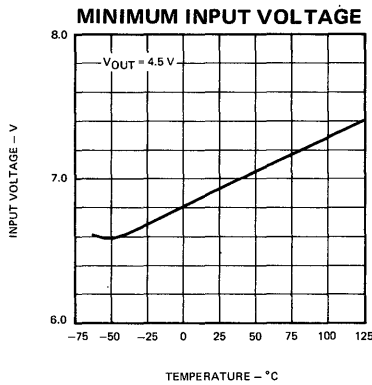
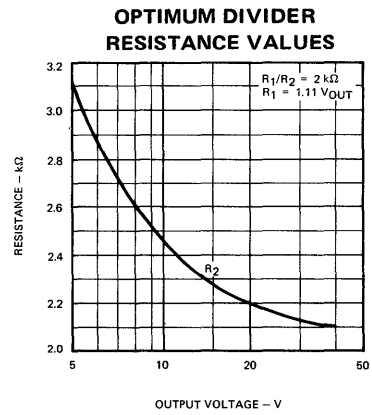
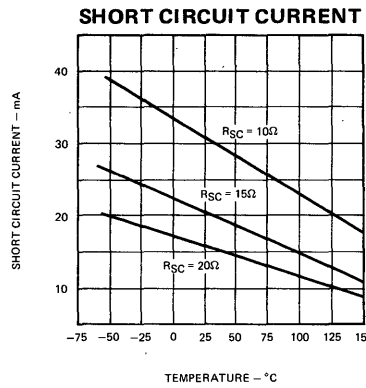
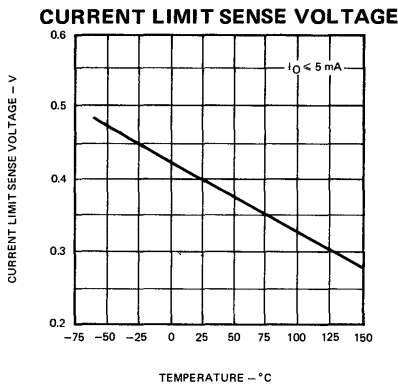
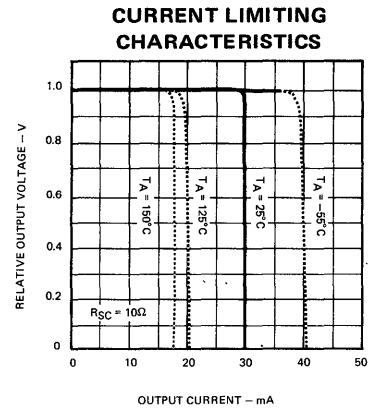
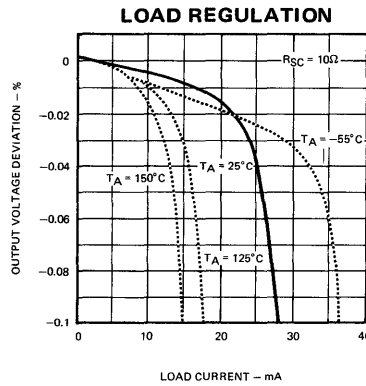
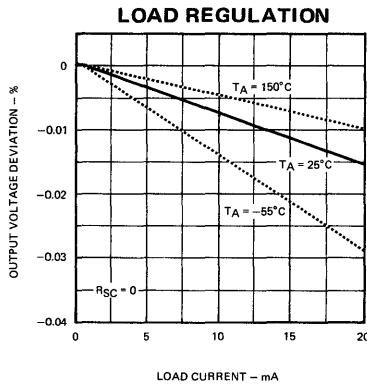
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		8.5		50	V
Output Voltage Range		4.5		40	V
Output/Input Voltage Differential		3.0		30	V
Load Regulation (Note 3)	$0 \leq I_O \leq 45 \text{ mA}$	$R_{SC} = 0\Omega, T_A = 25^\circ\text{C}$	0.02	0.2	%
		$R_{SC} = 0\Omega, T_A = 70^\circ\text{C}$	0.03	0.4	%
		$R_{SC} = 0\Omega, T_A = 0^\circ\text{C}$	0.03	0.4	%
Line Regulation		$V_{IN} - V_{OUT} \leq 5 \text{ V}$	0.025	0.06	%/V
		$V_{IN} - V_{OUT} > 5 \text{ V}$	0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10 \mu\text{F}, f = 120 \text{ Hz}$	0.003			%/V
Temperature Stability	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.3	1.0	%
Feedback Sense Voltage		1.55	1.7	1.85	V
Output Noise Voltage	$10 \text{ Hz} \leq f \leq 10 \text{ kHz}$	$C_{REF} = 0$	0.005		%
		$C_{REF} > 0.1 \mu\text{F}$	0.002		%
Current Limit Sense Voltage (Note 4)	$R_{SC} = 10\Omega, T_A = 25^\circ\text{C}, V_{OUT} = 0 \text{ V}$	225	300	375	mV
Standby Current Drain	$V_{IN} = 50 \text{ V}$		0.8	2.0	mA
Long Term Stability			0.1	1.0	%

376

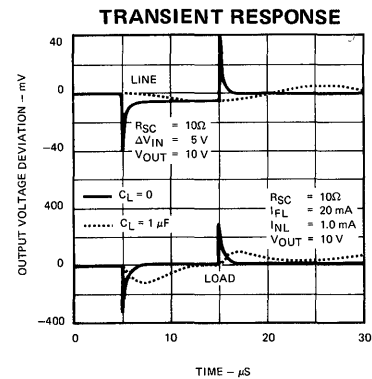
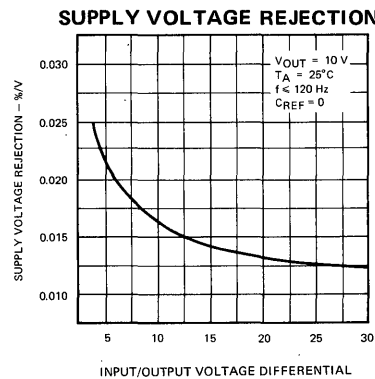
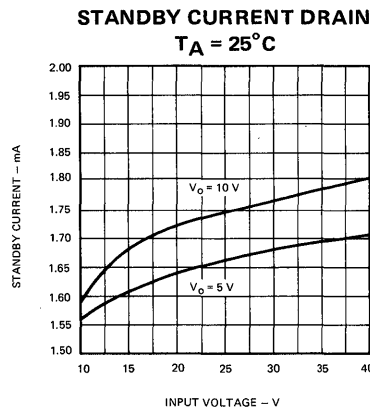
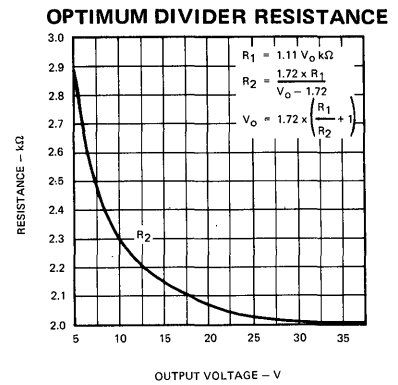
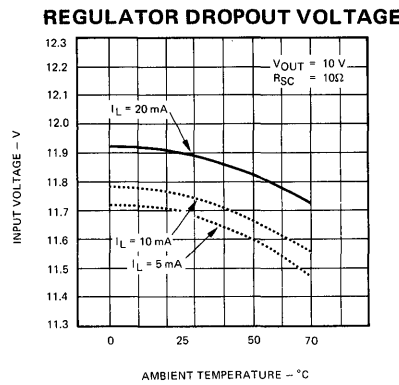
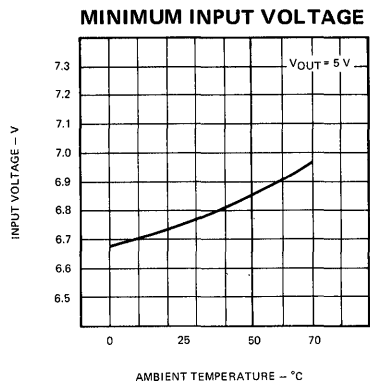
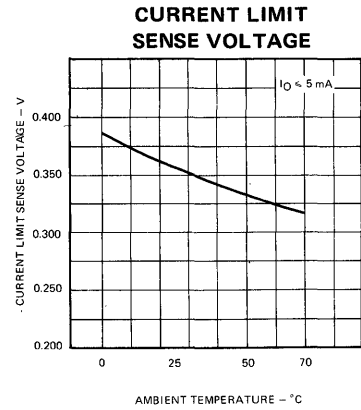
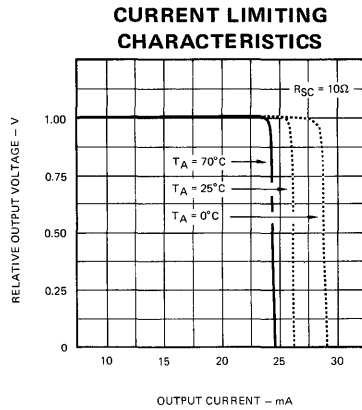
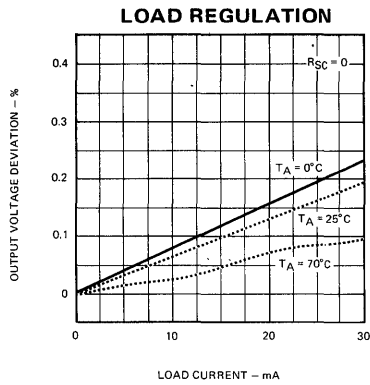
ELECTRICAL CHARACTERISTICS $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		9.0		40	V
Output Voltage Range		5.0		37	V
Output/Input Voltage Differential		3.0		30	V
Load Regulation	$0 \leq I_O \leq 25 \text{ mA}$	$R_{SC} = 0\Omega, T_A = 25^\circ\text{C}$		0.2	%
		$R_{SC} = 0\Omega, T_A = 70^\circ\text{C}$		0.5	%
		$R_{SC} = 0\Omega, T_A = 0^\circ\text{C}$		0.5	%
Line Regulation		$T_A = 25^\circ\text{C}$		0.03	%/V
				0.1	%/V
Ripple Rejection	$f = 120 \text{ Hz}, T_A = 25^\circ\text{C}$			0.1	%/V
Standby Current Drain	$V_{IN} = 30 \text{ V}, T_A = 25^\circ\text{C}$			2.5	mA
Reference Voltage		1.60	1.72	1.80	V
Current Limit Sense Voltage			0.360		V

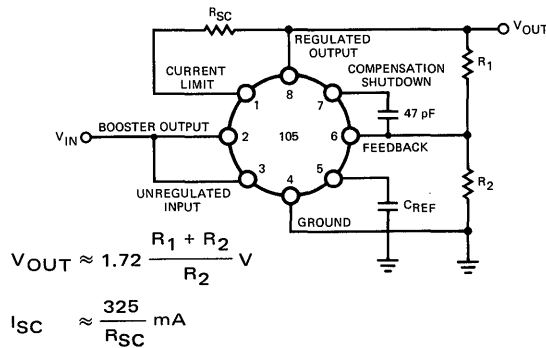
TYPICAL PERFORMANCE CURVES FOR 105/305/305A



TYPICAL PERFORMANCE CURVES FOR 376

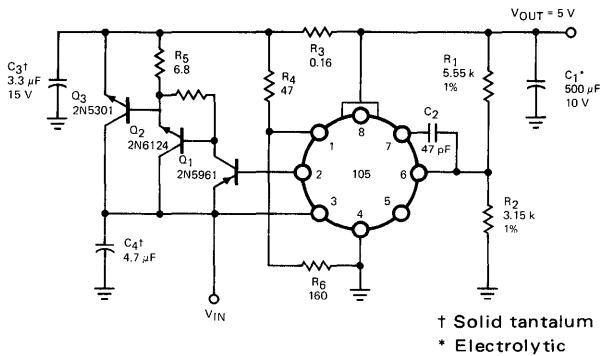


BASIC POSITIVE REGULATOR WITH CURRENT LIMITING



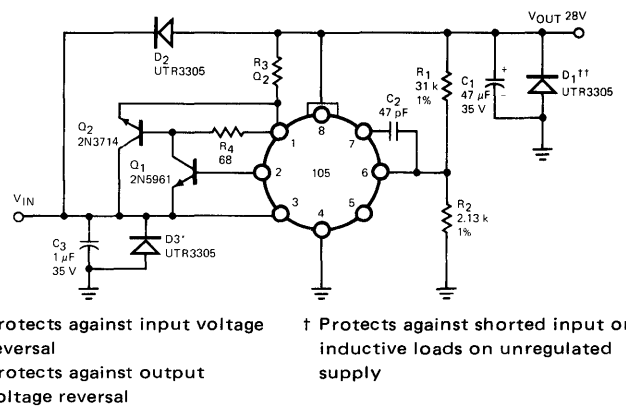
TYPICAL APPLICATIONS

10A REGULATOR WITH FOLDBACK CURRENT LIMITING



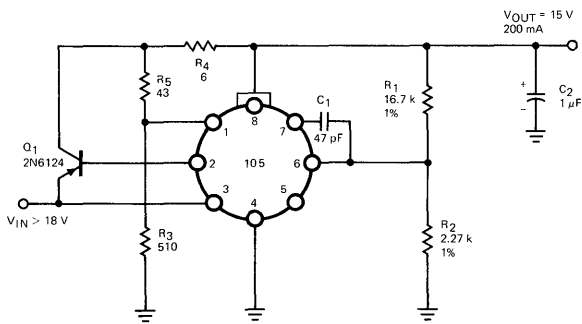
† Solid tantalum
* Electrolytic

1.0A REGULATOR WITH PROTECTIVE DIODES

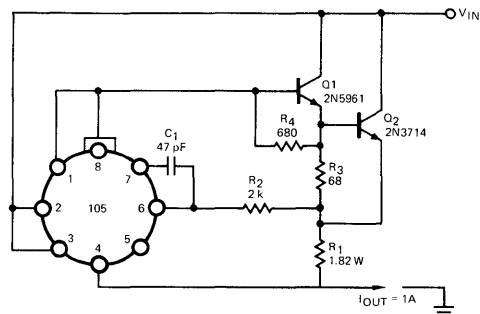


* Protects against input voltage reversal
† Protects against shorted input or inductive loads on unregulated supply
†† Protects against output voltage reversal

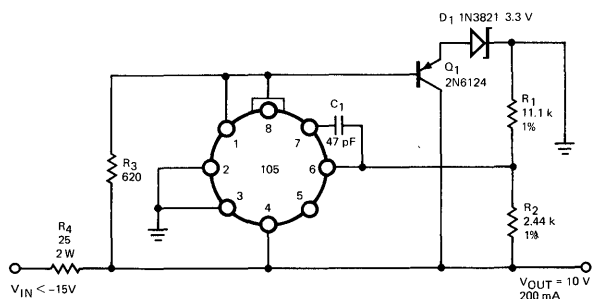
LINEAR REGULATOR WITH FOLDBACK CURRENT LIMITING



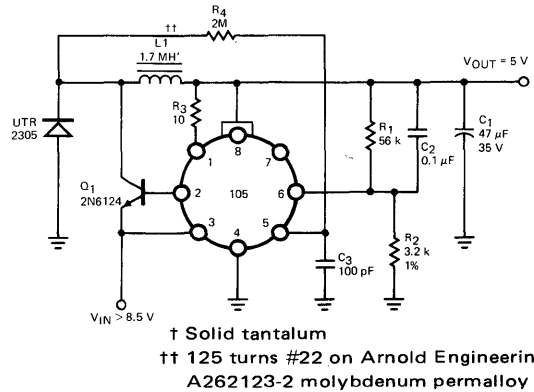
CURRENT REGULATOR



SHUNT REGULATOR



SWITCHING REGULATOR



† Solid tantalum
†† 125 turns #22 on Arnold Engineering A262123-2 molybdenum permalloy core.

109 • 209

FIVE VOLT REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

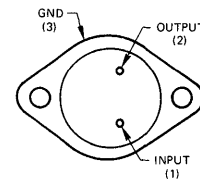
GENERAL DESCRIPTION — The 109 and 209 are complete Five Volt Regulators constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially indestructible. They are intended for use as local regulators, eliminating noise and distribution problems associated with single point regulation. If adequate heat sinking is provided, they can provide over 1A output current. The 109 and 209 are intended primarily for use with TTL and DTL logic and are completely specified under worst case conditions to match the power supply requirements of these logic families. In addition to use as a fixed 5 V regulator, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

- OUTPUT CURRENT IN EXCESS OF 1 AMP
- SPECIFIED TO MATCH WORST CASE TTL AND DTL REQUIREMENTS
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- OUTPUT TRANSISTOR SAFE-AREA COMPENSATION

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	-65° C to +150° C
Operating Junction Temperature Range	
109	-55° C to +150° C
209	-25° C to +150° C
Lead Temperature (Soldering, 60 seconds)	300° C

CONNECTION DIAGRAM
TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ

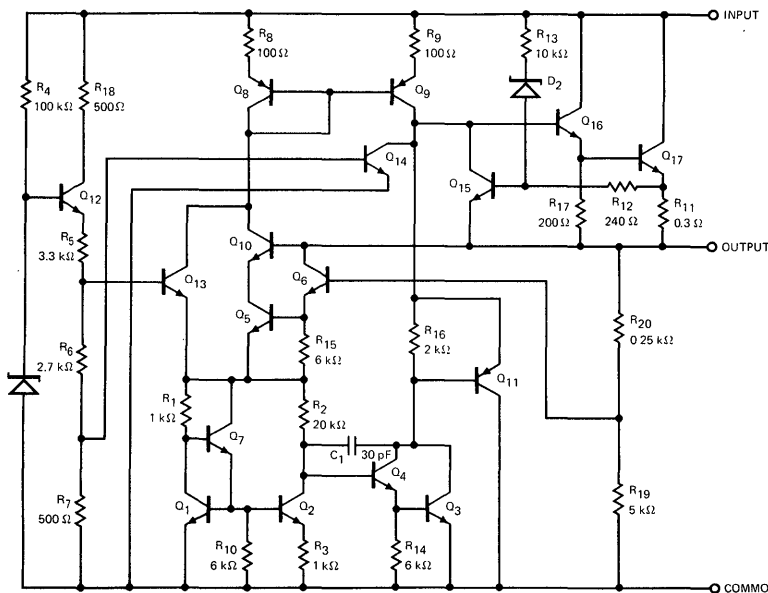


Case is connected to ground.

ORDER INFORMATION

TYPE	PART NO.
109	LM109K
209	LM209K

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

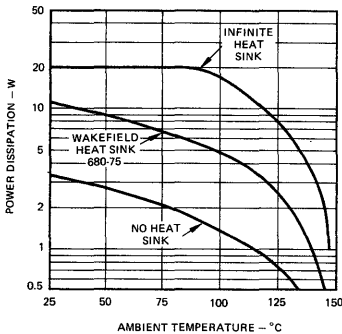
ELECTRICAL CHARACTERISTICS ($T_J = -55^\circ\text{C}$ to $+150^\circ\text{C}$ for 109, -25°C to $+150^\circ\text{C}$ for 209, $V_{IN} = 10\text{ V}$, $I_{OUT} = 0.5\text{ A}$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$	4.7	5.05	5.3	V
Line Regulation	$T_J = 25^\circ\text{C}$, $7\text{ V} \leq V_{IN} \leq 25\text{ V}$		4	50	mV
Load Regulation	$T_J = 25^\circ\text{C}$, $5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		15	100	mV
Output Voltage	$8\text{ V} \leq V_{IN} \leq 20\text{ V}$, $5\text{ mA} \leq I_{OUT} \leq 1\text{ A}$, $P \leq 15\text{ W}$	4.6		5.4	V
Quiescent Current	$7\text{ V} \leq V_{IN} \leq 25\text{ V}$			10	mA
		$T_J = 25^\circ\text{C}$		4.2	mA
Quiescent Current Change	with Line	$8\text{ V} \leq V_{IN} \leq 25\text{ V}$		0.8	mA
	with Load	$5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$		0.5	mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		40		μV
Long Term Stability				10	mV
Thermal Resistance Junction to Case (Note 1)			3.0		$^\circ\text{C/W}$

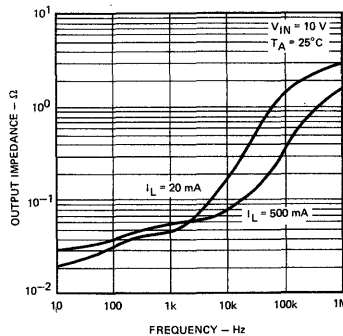
NOTE 1: Without a heat sink, the thermal resistance is approximately 35°C/W . With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

TYPICAL PERFORMANCE CURVES FOR 109 AND 209

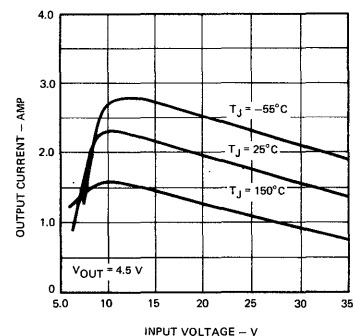
MAXIMUM AVERAGE POWER DISSIPATION



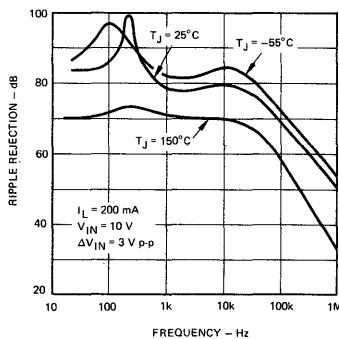
OUTPUT IMPEDANCE



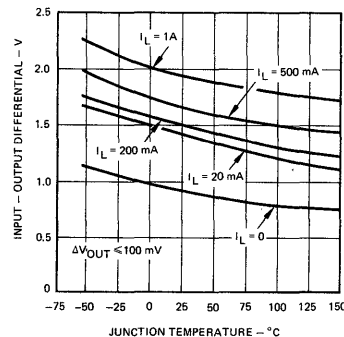
PEAK OUTPUT CURRENT



RIPPLE REJECTION

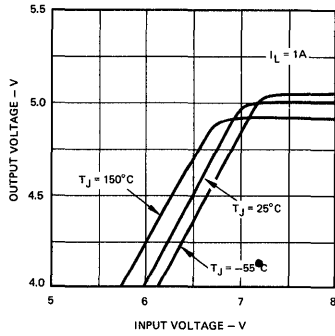


DROPOUT VOLTAGE

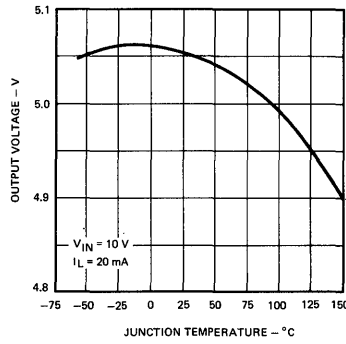


TYPICAL PERFORMANCE CURVES FOR 109 AND 209 (Cont'd)

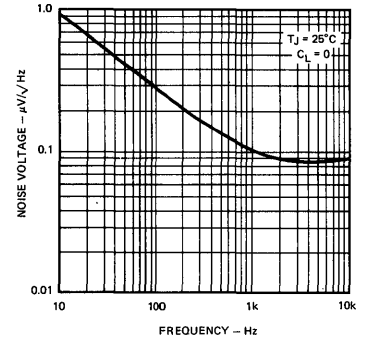
DROPOUT CHARACTERISTIC



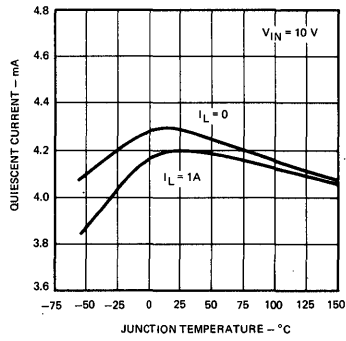
OUTPUT VOLTAGE



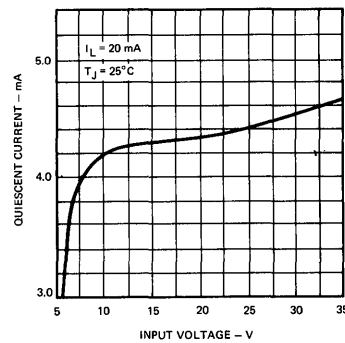
OUTPUT NOISE VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

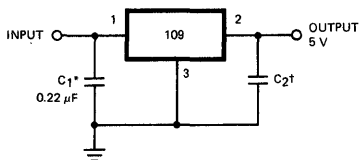


QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



APPLICATIONS

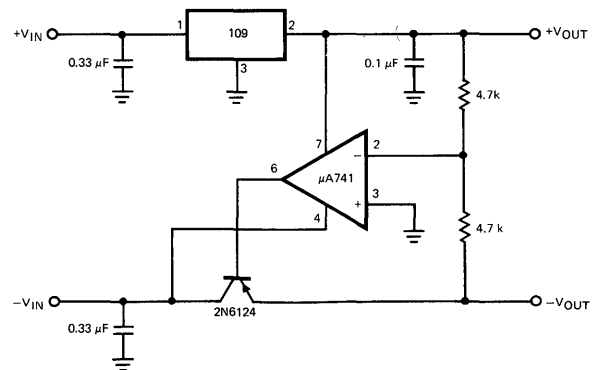
FIXED 5 V REGULATOR



NOTES:

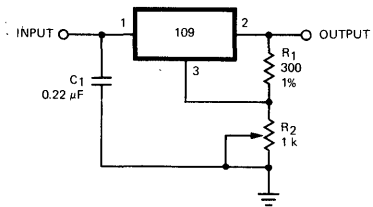
- *Required if regulator is located an appreciable distance from power supply filter.
- †Although no output capacitor is needed for stability, it does improve transient response.

TRACKING VOLTAGE REGULATOR

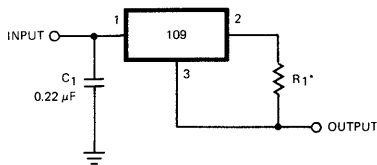


APPLICATIONS (Cont'd)

ADJUSTABLE OUTPUT REGULATOR

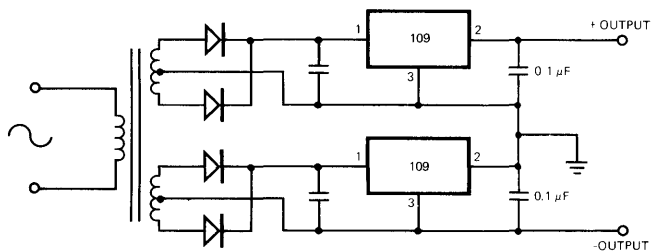


CURRENT REGULATOR



NOTE: * Determines output current.

POSITIVE AND NEGATIVE REGULATOR



309

FIVE VOLT REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

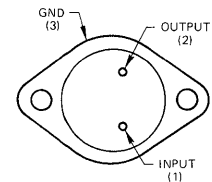
GENERAL DESCRIPTION — The 309 is a monolithic 5 Volt Regulator constructed using the Fairchild Planar* epitaxial process. This regulator employs internal current limiting, thermal shutdown and safe-area compensation making it essentially indestructible. The 309 is intended for use as a local regulator, eliminating noise and distribution problems associated with single point regulation. If adequate heat sinking is provided, it can provide over 1A output current. The 309 is intended primarily for use with TTL and DTL logic and is completely specified under worst case conditions to match the power supply requirements of these logic families. In addition to use as a fixed 5 volt regulator, this device can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

- **OUTPUT CURRENT IN EXCESS OF 1 AMP**
- **SPECIFIED TO MATCH WORST CASE TTL AND DTL REQUIREMENTS**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	0°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

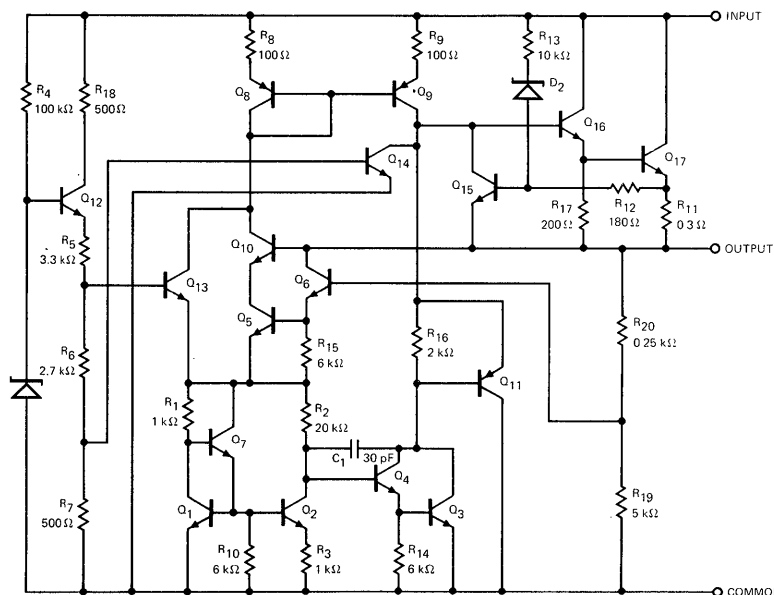
CONNECTION DIAGRAM
TO-3 PACKAGE
 (TOP VIEW)
 PACKAGE OUTLINE GJ



Case is connected to ground.

ORDER INFORMATION
TYPE PART NO.
309 LM309K

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (Note 1)

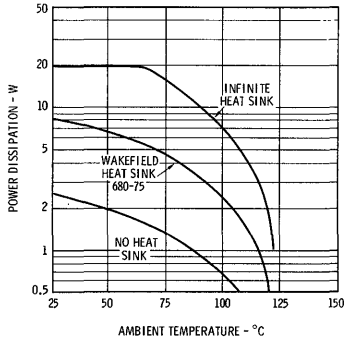
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$	4.8	5.05	5.2	V
Line Regulation	$T_J = 25^\circ\text{C}$ $7\text{ V} \leq V_{IN} \leq 25\text{ V}$		4.0	50	mV
Load Regulation	$T_J = 25^\circ\text{C}$ $5\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		50	100	mV
Output Voltage	$7\text{ V} \leq V_{IN} \leq 25\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 1.0\text{ A}$ $P \leq 20\text{ W}$	4.75		5.25	V
Quiescent Current	$7\text{ V} \leq V_{IN} \leq 25\text{ V}$		5.2	10	mA
Quiescent Current Change	with Line			0.5	mA
	with Load			0.8	mA
Output Noise Voltage	$T_A = 25^\circ\text{C}$ $10\text{ Hz} \leq f \leq 100\text{ kHz}$		40		μV
Long Term Stability				20	mV
Thermal Resistance Junction to Case (Note 2)			3.0		$^\circ\text{C/W}$

NOTES:

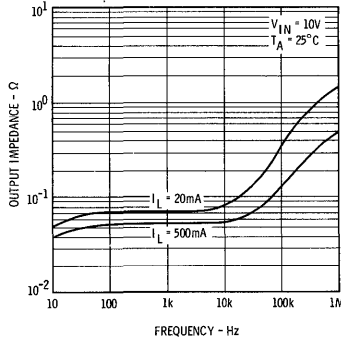
- Unless otherwise specified, these specifications apply for $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $V_{IN} = 10\text{ V}$ and $I_{OUT} = 0.5\text{ A}$.
- Without a heat sink, the thermal resistance of the TO-3 package is approximately 35°C/W . With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

TYPICAL PERFORMANCE CURVES

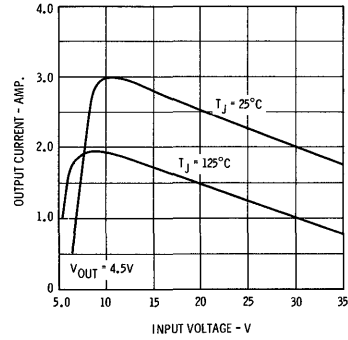
MAXIMUM AVERAGE POWER DISSIPATION



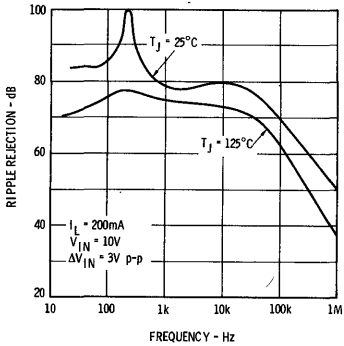
OUTPUT IMPEDANCE



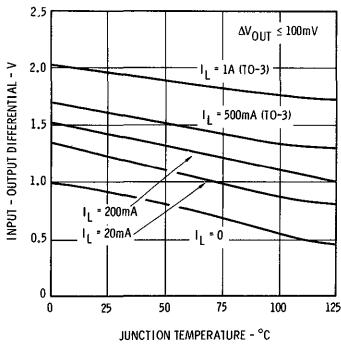
PEAK OUTPUT CURRENT



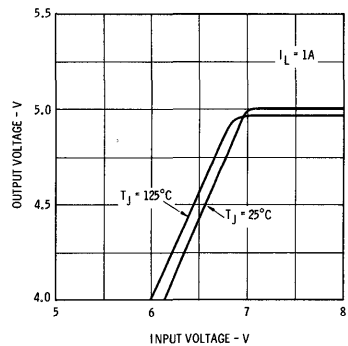
RIPPLE REJECTION



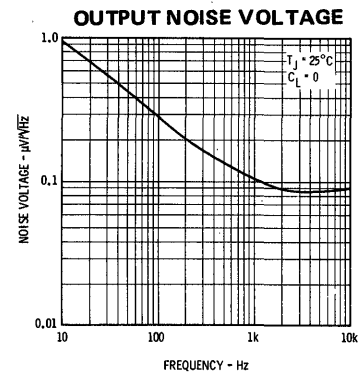
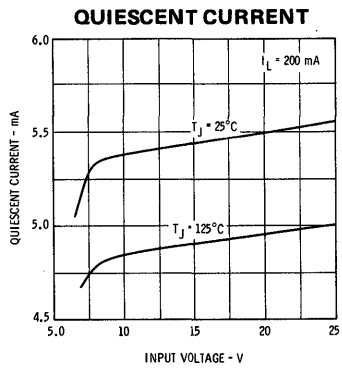
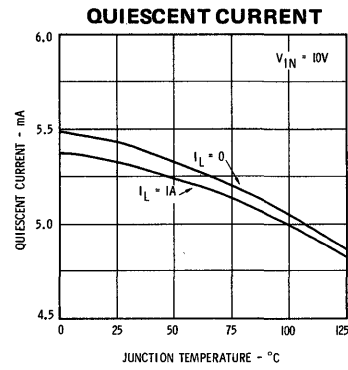
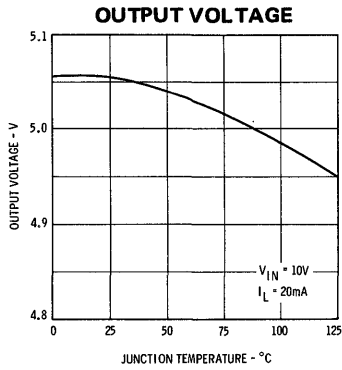
DROPOUT VOLTAGE



DROPOUT CHARACTERISTIC

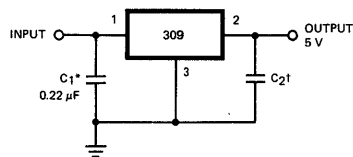


TYPICAL PERFORMANCE CURVES (Cont'd)



APPLICATIONS

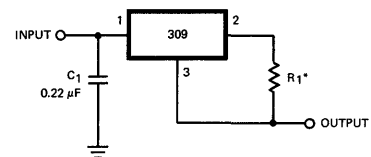
FIXED 5 V REGULATOR



NOTES:

- * Required if regulator is located an appreciable distance from power supply filter.
- † Although no output capacitor is needed for stability, it does improve transient response.

CURRENT REGULATOR



NOTES:

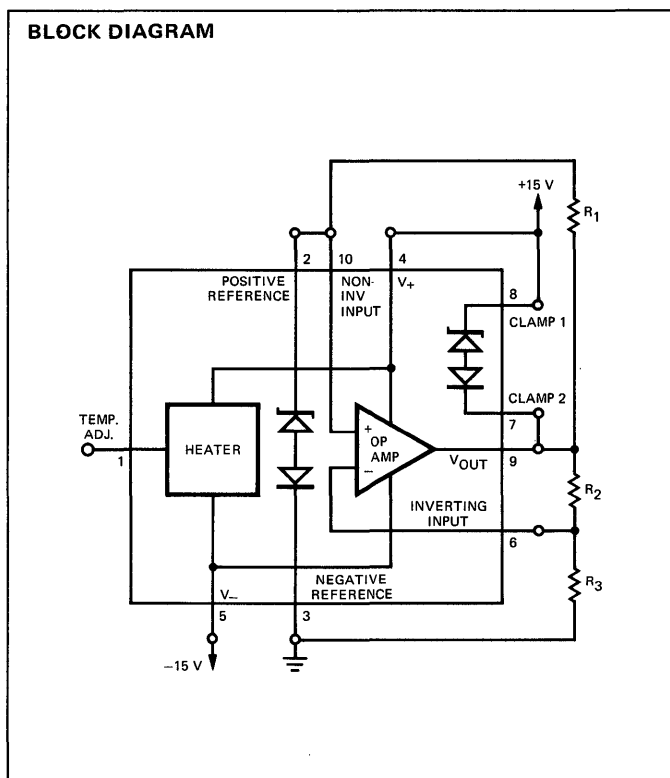
- * Determines output current.

μA728

PRECISION VOLTAGE REFERENCE

GENERAL DESCRIPTION — The μA728 is a Precision Voltage Reference with excellent output voltage temperature coefficient and long term stability. The device includes a zener diode reference, a buffer amplifier and a heater circuit to maintain constant chip temperature. The μA728 offers unmatched performance in applications such as A/D and D/A converters, precision voltage and current sources, digital voltmeters and programmable power supplies.

- 1 ppm/°C TYPICAL TEMPERATURE COEFFICIENT
- 10 ppm/1000 HOURS TYPICAL LONG-TERM STABILITY
- LOW DRIFT AMPLIFIER
- LOW OUTPUT IMPEDANCE
- POSITIVE OR NEGATIVE OPERATION
- LATCH-UP PREVENTION PROVIDED
- ADJUSTABLE CHIP TEMPERATURE



μA78T00

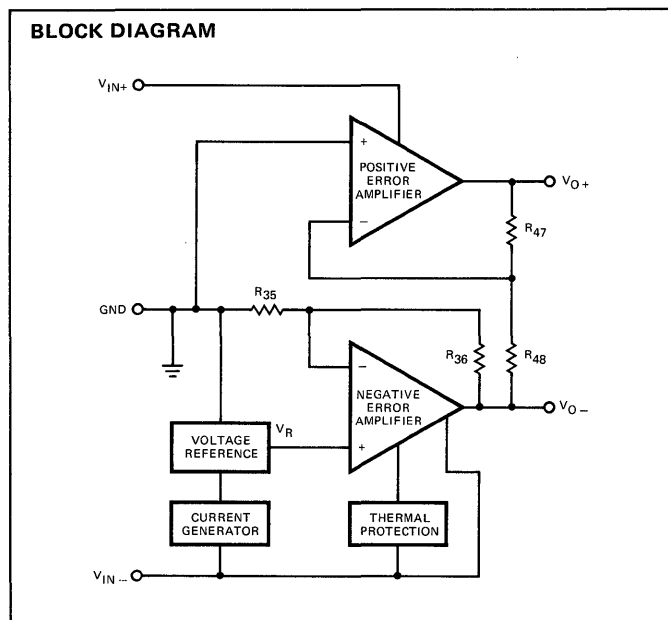
TRACKING VOLTAGE REGULATOR

GENERAL DESCRIPTION — The μA78T00 is a family of dual polarity Tracking Regulators which provide balanced positive and negative, regulated output voltages at currents up to 150 mA over the temperature range. Output current can be easily boosted by the addition of external pass transistors. Initial output voltage accuracy for prime grade devices is ±2%. In addition, the voltage can be adjusted over a ±10% range with the use of external components. The output current is internally limited for device protection. This, in conjunction with thermal shutdown circuitry, maintains chip temperature at a safe level. Internal compensation is included to maintain frequency stability.

The μA78T00 series is available in the following output voltages.

DEVICE TYPE	OUTPUT VOLTAGES
78T05	+ 5 V, - 5 V
78T06	+12 V, - 6 V
78T12	+12 V, -12 V
78T15	+15 V, -15 V
78T17	+ 5 V, -12 V
78T18	+18 V, -18 V

- EXCELLENT OUTPUT VOLTAGE REGULATION (±1%)
- INTERNAL AND EXTERNAL CURRENT LIMITING
- INTERNAL THERMAL SHUTDOWN
- FIXED OUTPUT VOLTAGES
- INTERNAL FREQUENCY COMPENSATION
- AVAILABLE IN 10-LEAD METAL CAN (PACKAGE OUTLINE 9J) AND 14-LEAD POWER DIP (PACKAGE OUTLINE 9J)
- MILITARY (-55°C to +125°C) AND COMMERCIAL (0°C TO 70°C) OPERATING TEMPERATURE RANGE



μA78M00 SERIES

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

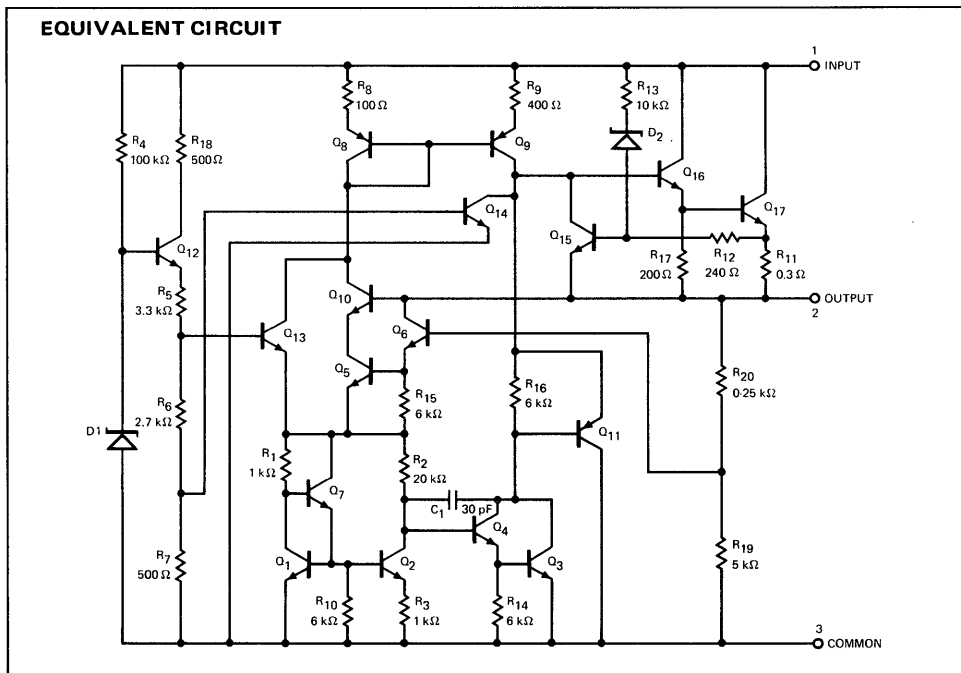
GENERAL DESCRIPTION — The μA78M00 series of Three-Terminal Medium Current Positive Voltage Regulators are constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 500 mA output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

- **OUTPUT CURRENT UP TO 0.5 AMP**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**

ABSOLUTE MAXIMUM RATINGS

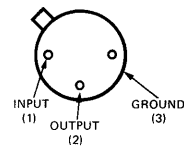
Input Voltage	
(5 V, 6 V, 8 V)	30 V
(12 V, 15 V)	35 V
(20 V, 24 V)	40 V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	-65°C to +200°C
Operating Junction Temperature Range (Note 2)	
Military (78M00)	-55°C to +175°C
Commercial (78M00C)	0°C to +175°C
Lead Temperature (Soldering, 60 second time limit)	300°C

EQUIVALENT CIRCUIT



Notes on following pages.

CONNECTION DIAGRAM
TO-5 TYPE PACKAGE
(TOP VIEW)
PACKAGE OUTLINE CS



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	78M05	78M05HM
6 V	78M06	78M06HM
8 V	78M08	78M08HM
12 V	78M12	78M12HM
15 V	78M15	78M15HM
20 V	78M20	78M20HM
24 V	78M24	78M24HM
5 V	78M05C	78M05HC
6 V	78M06C	78M06HC
8 V	78M08C	78M08HC
12 V	78M12C	78M12HC
15 V	78M15C	78M15HC
20 V	78M20C	78M20HC
24 V	78M24C	78M24HC

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A78M00 SERIES

78M05 AND 78M05C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 10\text{ V}$, $I_{OUT} = 200\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M05 and $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M05C, unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$			5.0		V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$7\text{ V} \leq V_{IN} \leq 20\text{ V}$		3.0		mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		25		mV
Output Voltage	$8.0\text{ V} \leq V_{IN} \leq 20\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$			5.0		V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.2		mA
Quiescent Current Change	with line	$8\text{ V} \leq V_{IN} \leq 25\text{ V}$		0.2		mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		0.1		mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$			40		μV
Ripple Rejection	$f = 120\text{ Hz}$, $8\text{ V} \leq V_{IN} \leq 18\text{ V}$			78		dB
Dropout Voltage	$T_J = 25^{\circ}\text{C}$, $I_{OUT} = 0.5\text{ A}$			2.0		V
Peak Output Current	$T_J = 25^{\circ}\text{C}$			750		mA

78M06 AND 78M06C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 11\text{ V}$, $I_{OUT} = 200\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M06 and $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M06C, unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$			6.0		V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$8\text{ V} \leq V_{IN} \leq 20\text{ V}$		5.0		mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		30		mV
Output Voltage	$9\text{ V} \leq V_{IN} \leq 21\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$			6.0		V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.3		mA
Quiescent Current Change	with line	$9\text{ V} \leq V_{IN} \leq 25\text{ V}$		0.2		mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		0.1		mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$			45		μV
Ripple Rejection	$f = 120\text{ Hz}$, $9\text{ V} \leq V_{IN} \leq 19\text{ V}$			75		dB
Dropout Voltage	$T_J = 25^{\circ}\text{C}$, $I_{OUT} = 0.5\text{ A}$			2.0		V
Peak Output Current	$T_J = 25^{\circ}\text{C}$			750		mA

NOTE 1: Thermal resistance of the packages (without a heat sink)

Junction to Case 20°C/W **Junction to Ambient** 170°C/W

NOTE 2: Operating Ambient Temperature Range

78M00 -55°C to $+125^{\circ}\text{C}$

78M00C 0°C to 85°C

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A78M00 SERIES

78M08 AND 78M08C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 14$ V, $I_{OUT} = 200$ mA, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M08 and $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M08C, unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$			8.0		V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$10.5\text{ V} \leq V_{IN} \leq 25\text{ V}$		6.0		mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		40		mV
Output Voltage	$11.5\text{ V} \leq V_{IN} \leq 23\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$			8.0		V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.3		mA
Quiescent Current Change	with line	$11.5\text{ V} \leq V_{IN} \leq 25\text{ V}$		0.2		mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		0.1		mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $19\text{ Hz} \leq f \leq 100\text{ kHz}$			52		μV
Ripple Rejection	$f = 120\text{ Hz}$, $11.5\text{ V} \leq V_{IN} \leq 21.5\text{ V}$			72		dB
Dropout Voltage	$T_J = 25^{\circ}\text{C}$, $I_{OUT} = 0.5\text{ A}$			2.0		V
Peak Output Current	$T_J = 25^{\circ}\text{C}$			750		mA

78M12 AND 78M12C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 19$ V, $I_{OUT} = 200$ mA, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M12 and $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M12C, unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$			12		V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$14.5\text{ V} \leq V_{IN} \leq 30\text{ V}$		10		mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		50		mV
Output Voltage	$15.5\text{ V} \leq V_{IN} \leq 27\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$			12		V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.3		mA
Quiescent Current Change	with line	$15\text{ V} \leq V_{IN} \leq 30\text{ V}$		0.2		mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		0.1		mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$			75		μV
Ripple Rejection	$f = 120\text{ Hz}$, $15\text{ V} \leq V_{IN} \leq 25\text{ V}$			71		dB
Dropout Voltage	$T_J = 25^{\circ}\text{C}$, $I_{OUT} = 0.5\text{ A}$			2.0		V
Peak Output Current	$T_J = 25^{\circ}\text{C}$			750		mA

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A78M00 SERIES

78M15 AND 78M15C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 23\text{ V}$, $I_{OUT} = 200\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M15 and $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M15C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$		15		V
Line Regulation	$T_J = 25^{\circ}\text{C}$, $17.5\text{ V} \leq V_{IN} \leq 30\text{ V}$		11		mV
Load Regulation	$T_J = 25^{\circ}\text{C}$, $5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		60		mV
Output Voltage	$18.5\text{ V} \leq V_{IN} \leq 30\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$		15		V
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.4		mA
Quiescent Current Change	with line	$18.5\text{ V} \leq V_{IN} \leq 30\text{ V}$	0.2		mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$	0.1		mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		90		μV
Ripple Rejection	$f = 120\text{ Hz}$, $18.5\text{ V} \leq V_{IN} \leq 28.5\text{ V}$		70		dB
Dropout Voltage	$I_{OUT} = 1.0\text{ A}$, $T_J = 25^{\circ}\text{C}$, $I_{OUT} = 0.5\text{ A}$		2.0		V
Peak Output Current	$T_J = 25^{\circ}\text{C}$		700		mA

78M20 AND 78M20C

ELECTRICAL CHARACTERISTICS ($V_{IN} = 29\text{ V}$, $I_{OUT} = 200\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M20 and $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M20C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$		20		V
Line Regulation	$T_J = 25^{\circ}\text{C}$, $23\text{ V} \leq V_{IN} \leq 36\text{ V}$		15		mV
Load Regulation	$T_J = 25^{\circ}\text{C}$, $5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		80		mV
Output Voltage	$24\text{ V} \leq V_{IN} \leq 35\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$		20		V
Quiescent Current	$T_J = 25^{\circ}\text{C}$		4.5		mA
Quiescent Current Change	with line	$24\text{ V} \leq V_{IN} \leq 35\text{ V}$	0.2		mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$	0.1		mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$		110		μV
Ripple Rejection	$f = 120\text{ Hz}$, $24\text{ V} \leq V_{IN} \leq 34\text{ V}$		69		dB
Dropout Voltage	$T_J = 25^{\circ}\text{C}$, $I_{OUT} = 0.5\text{ A}$		2.0		V
Peak Output Current	$T_J = 25^{\circ}\text{C}$		700		mA

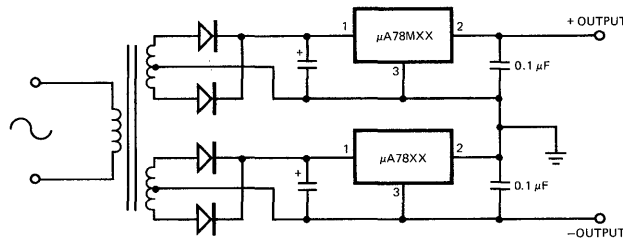
FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A78M00 SERIES

78M24 AND 78M24C

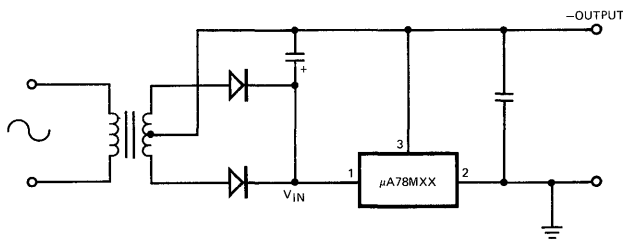
ELECTRICAL CHARACTERISTICS ($V_{IN} = 33\text{ V}$, $I_{OUT} = 200\text{ mA}$, $-55^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M24 and $0^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ for 78M24C, unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_J = 25^{\circ}\text{C}$			24		V
Line Regulation	$T_J = 25^{\circ}\text{C}$	$27\text{ V} \leq V_{IN} \leq 38\text{ V}$		18		mV
Load Regulation	$T_J = 25^{\circ}\text{C}$	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		100		mV
Output Voltage	$28\text{ V} \leq V_{IN} \leq 38\text{ V}$ $5\text{ mA} \leq I_{OUT} \leq 200\text{ mA}$			24		V
Quiescent Current	$T_J = 25^{\circ}\text{C}$			4.6		mA
Quiescent Current Change	with line	$28\text{ V} \leq V_{IN} \leq 38\text{ V}$		0.2		mA
	with load	$5\text{ mA} \leq I_{OUT} \leq 0.5\text{ A}$		0.1		mA
Output Noise Voltage	$T_A = 25^{\circ}\text{C}$, $\text{Hz} \leq f \leq 100\text{ kHz}$			170		μV
Ripple Rejection	$f = 120\text{ Hz}$, $28\text{ V} \leq V_{IN} \leq 38\text{ V}$			66		dB
Dropout Voltage	$T_J = 25^{\circ}\text{C}$, $I_{OUT} = 0.5\text{ A}$			2.0		V
Peak Output Current	$T_J = 25^{\circ}\text{C}$			700		mA

APPLICATIONS

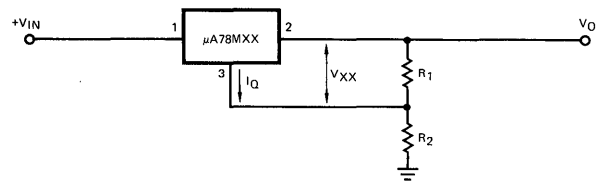
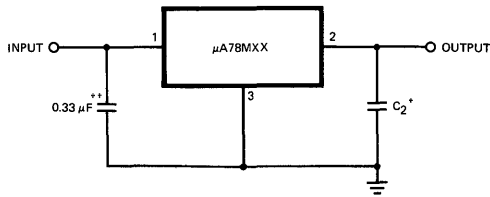


POSITIVE AND NEGATIVE REGULATOR



NEGATIVE OUTPUT VOLTAGE CIRCUIT

APPLICATIONS (Cont'd)

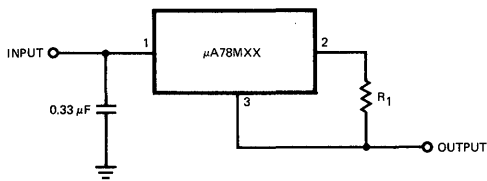


NOTES:

- * To specify an output voltage, substitute voltage value for "XX".
- + Although no output capacitor is needed for stability, it does improve transient response.
- ++ Required if regulator is located an appreciable distance from power supply filter.

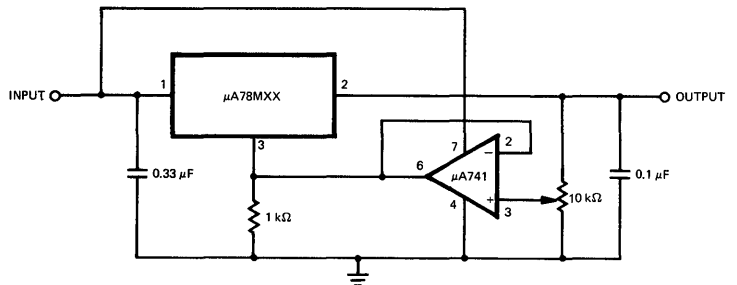
$$V_0 = V_{XX} \left(1 + \frac{R_2}{R_1}\right) + I_Q R_2$$

FIXED OUTPUT REGULATOR

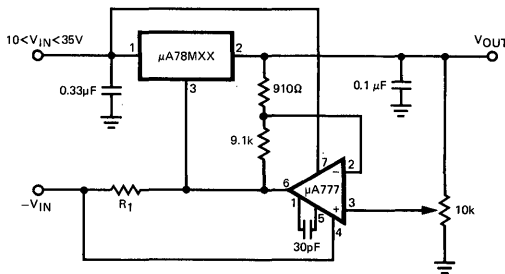


$$\text{Output Current} = \frac{V_{OUT}}{R_1}$$

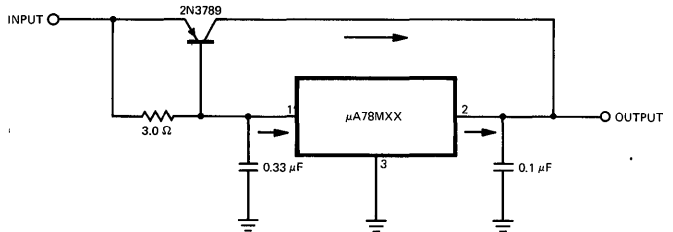
CIRCUIT FOR INCREASING OUTPUT VOLTAGE



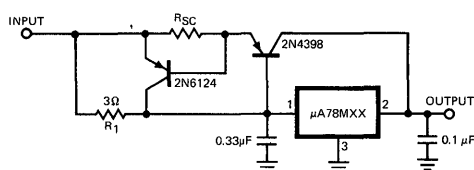
CURRENT REGULATOR



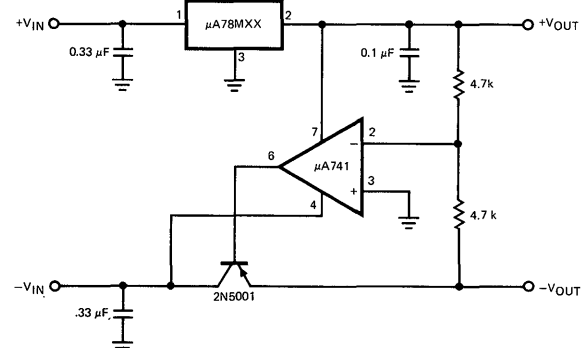
ADJUSTABLE OUTPUT REGULATOR, 7 to 30 VOLTS



VARIABLE OUTPUT VOLTAGE, 0.5 to 7 VOLTS



HIGH CURRENT VOLTAGE REGULATOR



HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED

± TRACKING VOLTAGE REGULATOR

μA78N00

THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

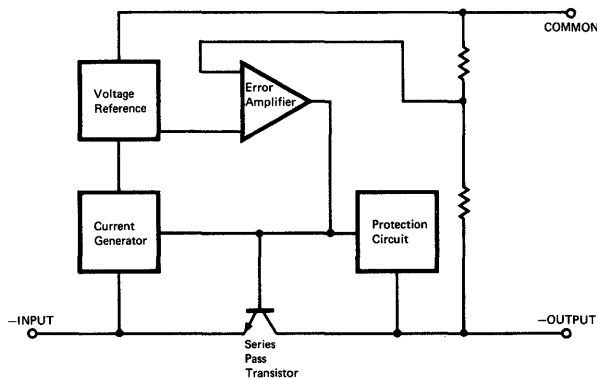
GENERAL DESCRIPTION — The μA78N00 series of monolithic three Terminal Negative Voltage Regulators is specifically designed for emitter coupled logic (ECL) circuits. Three voltages are available: -2.0 V, -4.0 V, and -5.2 V. The μA78N00 regulators are capable of providing output currents to 3A with adequate heat sinking. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation making them essentially indestructible. The output voltage is precision trimmed to typically 0.5% and has excellent tolerance to variations with line voltage, load current, and ambient temperature. The μA78N00 are intended as fixed-voltage regulators in ECL applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation.

- **OUTPUT VOLTAGE TOLERANCE TYPICALLY 0.5% WITHOUT EXTERNAL TRIMMING**
- **OUTPUT CURRENT OF UP TO 3 AMPERES**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION AND SHORT CIRCUIT PROTECTION**

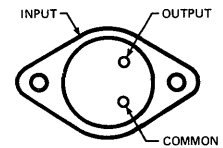
ABSOLUTE MAXIMUM RATINGS

Input Voltage	-15 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	
Military (78N00)	-55°C to $+125^{\circ}\text{C}$
Commercial (78N00C)	0°C to $+70^{\circ}\text{C}$
Lead Temperature (Soldering, 60 second time limit)	300°C

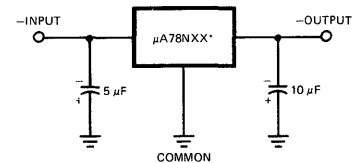
BLOCK DIAGRAM



**CONNECTION DIAGRAM
TO -3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ**



TYPICAL APPLICATION



* To specify an output voltage, substitute voltage value for "XX".

GLOSSARY

VOLTAGE REGULATORS

Average Temperature Coefficient of Output Voltage — The percentage change in output voltage for a specified change in ambient temperature.

Current Limit Sense Voltage — The voltage across the current limit terminals required to initiate current limiting.

Dropout Voltage — The input/output differential voltage at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage — The voltage measured on the feedback terminal of the regulator, with respect to ground, when the device is operating in regulation.

Input Voltage Range — The range of dc input voltage over which the regulator will operate within specifications.

Input/Output Voltage Differential — The value of difference voltage between input and output outside of which the regulator ceases to operate within specifications.

Line Regulation — The percentage change of output voltage for a specified change in input voltage.

Load Regulation — The percentage change in output voltage for a specified change in load current.

Long Term Stability — Output voltage stability under accelerated life test conditions after 1000 hours at maximum rated voltage and power dissipation.

Output Noise Voltage — The rms value of the noise voltage measured at the output with constant load current and no input ripple.

Output Resistance — The resistance seen looking into the output terminal at a specified value of load current.

Output Voltage Range — The range of regulated output voltages over which the specifications apply.

Output Voltage Scale Factor — The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

Quiescent Current — That part of the input current to the regulator that is not delivered to the load.

Reference Voltage — The output of the reference amplifier measured with respect to the negative supply.

Ripple Rejection — The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Short-Circuit Current Limit — The output current of the regulator with the output shorted to the negative supply.

Standby Current Drain — The supply current drawn by the regulator with no output load and no reference voltage load.

Temperature Stability — The percentage change in output voltage over a specified ambient temperature range.

LINEAR

CONTENTS AND SECTION SELECTOR

COMPUTER/INTERFACE

6

CONSUMER

7

TRANSISTOR/DIODE ARRAYS/ANALOG SWITCHES

8

PACKAGE OUTLINES

9

ORDER INFORMATION

10

MIL-M-38510/MIL-STD-883

11

DICE

12

INDUSTRY CROSS REFERENCE GUIDE

13

APPLICATION INFORMATION

14

INDEX

Selection Guide 6-4

DATA SHEETS

DATA TRANSMISSION

General Purpose

9614 Dual Differential Line Driver 6-23
9615 Dual Differential Line Driver 6-27
9620 Dual Differential Line Receiver 6-36
9621 Dual Line Driver 6-42
9622 Dual Line Receiver 6-48
55/75107A Dual Line Receivers 6-69
55/75108A Dual Line Receivers 6-69
55/75109 Dual Line Drivers 6-75
55/75110 Dual Line Drivers 6-75
8T13 Dual Single-Ended Line Driver 6-114
8T14 Triple Line Receiver 6-117

RS-232-C/MIL-STD-188C

9616 Triple EIA RS-232-C/MIL-STD-188C
Line Driver 6-31
9617 Triple EIA RS-232-C Line Receiver 6-34
9627 Dual EIA RS-232-C/MIL-STD-188C
Line Receiver 6-57

IBM Compatible

8T23 Dual Single-Ended Line Driver 6-120
8T24 Triple Line Receiver 6-123

DISPLAY DRIVERS

LED

9660 Seven Segment Decoder/Programmable
Current Driver 6-146
9661 Quad Programmable Current Segment Driver .. 6-146
9662 Quad LED/Lamp Digit Driver..... 6-147
9663 Hex LED/Lamp Digit Driver 6-147
75491 MOS to LED Segment and Digit Driver 6-110
75492 MOS to LED Segment and Digit Driver 6-110
9307 Seven Segment Decoder 6-18
9317B Seven Segment Decoder/Driver..... 6-19
9617C Seven Segment Decoder/Driver..... 6-19
9368 Seven Segment Decoder/Driver/Latch 6-20
9369 Seven Segment Decoder/Driver/Latch 6-21
9370 Seven Segment Decoder/Driver/Latch 6-22

MEMORY

Core Drivers

55/75325 Memory Driver..... 6-79
7524 Two Channel Core Memory Sense Amplifier 6-87
7525 Two Channel Core Memory Sense Amplifier 6-87

MOS Memory

75107A Dual Line Receiver 6-69
75108A Dual Line Receiver 6-69
SH0013 Two Phase MOS Clock Driver 6-126

GENERAL PURPOSE DRIVERS

9624 Dual TTL, MOS Interface Element 6-52
9625 Dual TTL, MOS Interface Element 6-52
75450A Dual Peripheral Driver..... 6-91
75451A Dual Peripheral Driver..... 6-91

75452	Dual Peripheral Driver	6-91
75453	Dual Peripheral Driver	6-91
75454	Dual Peripheral Driver	6-91
75460A	Dual High Voltage Peripheral Driver	6-91
75461A	Dual High Voltage Peripheral Driver	6-91
75462A	Dual High Voltage Peripheral Driver	6-91
75463A	Dual High Voltage Peripheral Driver	6-91
75464A	Dual High Voltage Peripheral Driver	6-91
SH2001	High Voltage, High Current Driver	6-131
SH2002	DTL High Power Driver	6-135
SH2200	High Voltage, High Current Driver	6-139

D/A AND A/D CONVERSION

μA722	10-Bit Current Source	6-9
9650	4-Bit Current Source	6-60
SH8090	10-Bit D/A Converter	6-143

Tape — Disc File Amplifier

μA733	Differential Video Amplifier	6-12
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Products to be Announced	6-145
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Glossary	6-148
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INTRODUCTION

Interface circuits, a major category within linear integrated circuits, perform the interface between analog and digital systems. They can be categorized by the function they perform.

- Data Transmission
- Display Driving
- Memory Driving and Sensing
- General Purpose Driving
- D/A and A/D Conversion
- Tape and Disc File Amplification

Each device category can be described as follows:

1. Data Transmission, i.e., Line Driver and Receivers
These devices adapt TTL signal levels for transmission over data transmission line and back to TTL signal levels at the receiving end of the transmission line.
2. Display Drivers, i.e., LED Drivers
These devices convert MOS and TTL signal levels to high output currents for driving LED displays.
3. Memory Driving and Sensing
These drivers convert TTL signal levels to the appropriate signal required by the memory system. The sense amplifiers convert the small output signals to TTL signal levels.
4. General Purpose Drivers, i.e., Peripheral Drivers
These devices convert TTL signal levels to high voltage and current output levels.
5. D/A and A/D Conversion and Tape and Disc File Amplifiers
These devices perform specific function as their name implies.

Interface circuits reduce overall system complexity and greatly improve system performance. Simplify your system — analog or digital — with Fairchild linear circuits interface products.

SELECTION GUIDE FOR LINE DRIVER AND RECEIVER

DATA TRANSMISSION DISTANCE	FORM OF CIRCUIT OPERATION	SUGGESTED DEVICES		CONSTRAINTS
		DRIVERS	RECEIVERS	
SIMPLEX OR HALF DUPLEX				
Short Distance, Up to 10 Ft.	Single Ended	7400 or 9000 Series		Transmission Lines Up to 10 Ft. With $\geq 93 \Omega$ Impedances
10 Ft. Up to 500 Ft.	Single Ended	9614 8T13	9615 8T14	Distance of Transmission Limited by Environmental Noise
500 Ft. and Up	Balanced Differential	9614 75109/75110	9615 75107/75108	For Use in High Noise Environments and Long Distance Data Transmission Up to 4,000 Ft.
MULTIPLEX				
Up to 500 Ft.	Single Ended	8T13	8T14	
500 Ft. and Up	Balanced Differential	75109/75110	75107/75108	
SPECIAL SPECIFICATIONS				
EIA RS232C		9616	9617 9627	Implied Maximum Cable Length is 50 Ft., Maximum Modulation Rate is 20 k Baud
MIL-STD-188		9616	9627	External Capacitor May Be Needed on 9616 to Control Rise and Fall to 5 – 15% of the Unit Interval at the Maximum System Modulation Rate
IBM 360 – I/O Interface		8T23	8T24	

SELECTION GUIDE FOR TRANSMISSION LINE DRIVERS

KEY FEATURES (Typical)	UNITS	9614	9616(1)	9621	9624(2)	75450 SERIES(3)	75109	75110	8T13(4)	8T23(4)
Supply Voltages	V	+5.0	+12 -12	+5.0 +12	+5.0 (0 to -30)	+5.0	+5.0 -5.0	+5.0 -5.0	+5.0	+5.0
Inputs TTL Compatible		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
V_{OH}	V	+3.2	+6.0	+4.3	$V_{TAP}-0.5$	+30 (max)	N/A	N/A	3.2	3.2
V_{OL}	V	+0.2	-6.0	+0.2	$V_{DD}+0.2$	+0.4	N/A	N/A	0	0
I_O (On) $V_O = 2.0$ V Nominal Supplies	mA	-85	N/A	-250	-20 ($V_O = -10$ V)	+300 (max)	+6.0	+12	-210	-210
I_{OL} (Off) $V_O = 0.4$ V Nominal Supplies	μ A	N/A	N/A	N/A	N/A	100	100	100	500	40
I_{SC}	mA	-90	+15 to -15	-420	-20	N/A	+6.0	+12	+30	+30
t_{pd}	ns	16	300	10	120	30	9.0	9.0	20	20
P_O per Channel	mW	87	83	60	20	30	180	300	160	160

NOTES FOR LINE DRIVERS/INTERFACE DRIVERS

- The 9616 is a triple EIA line driver. Each driver incorporates an internal response control circuit. The slew rate is a maximum of $30 \text{ V}/\mu\text{s}$ and a minimum of $4 \text{ V}/\mu\text{s}$ (3% of unit interval at 20 k baud). The two values for I_{SC} are the typical V_{OH} and V_{OL} short circuit currents. The t_{pd} is measured from 1.5 V on the input to the output passing through the 0 V point. The delay is caused by the internally controlled slew rate of the output. The 9616 meets the electrical interface requirements of EIA-RS-232C and the CCITT recommendation V.24. By using an external capacitor from the output to ground for wave shaping, the 9616 will also meet the low level digital interface for MIL-STD-188C.
- The 9624 dual TTL/DTL to MOS level converter is designed to operate with a V_{DD} from 0 to -30 V.
- The V_{OH} value is a maximum stand off voltage on the collector of the output device. I_O (on) is the maximum steady state current sinking capability of the output device. I_O (off) is the maximum leakage current into the output with the output device off.
- The 8T13 and 8T23 have foldback current limited outputs. V_{OL} is a typical $V_{CE(sat)}$ of the output transistor at collector currents of 100 mA ($V_{OL} = 0.25 \text{ V}$) and 300 mA ($V_{OL} = 0.5 \text{ V}$).

SELECTION GUIDE FOR TRANSMISSION LINE RECEIVERS OR SENSE AMPLIFIERS

KEY FEATURES (Typical)	UNITS	9615	9617	9620	9622	9625	9627(1)	8T14	8T24	75107	75108	7524	7525
Supply Voltages	V	+5.0	+5.0	+5.0 to +12	+5.0 to -10	+5.0 -11 to -30	+12.0 -12.0	+5.0	+5.0	+5.0 -5.0	+5.0 -5.0	+5.0 -5.0	+5.0 -5.0
Outputs TTL Compatible		Yes	Yes	Yes	Yes	Yes	Yes Wired-OR	Yes	Yes	Yes	Yes Open Collector	Yes	Yes
V _{TH}	V	±0.5	+1.5	±0.5	+1.5	-3.0/-9.0	±0.6 ±2.4	+1.5	+1.5	±0.025	±0.025	±0.04	±0.025
V _{CM}	V	±15	±25	±15	±10	N/A	±2.5	N/A	N/A	±3.0	±3.0	N/A	N/A
R _{IN}	kΩ	7.0	4.0	2.4	5.0	22	3 TO 7 or >6	18	18	16	16	2.6	2.5
P _D	mW	175	100	110	140	60	234	315	315	130	130	175	175
t _{pd}	ns	28	50	30	35	70	72	20	20	14	14	25	25
Differential Inputs		X		X	X		X			X	X	X	X
Output Enable		X			X		X			X	X		
Response Control		X	X	X									
Line Terminaator		X	X		X		X						
Wired-OR Output		X	X	X	X		X				X		
Failsafe Control			X		X								

1. 9627 Dual EIA RS-232/Mil-Std 188C Line Driver allows two levels of hysteresis and a choice of input resistances to satisfy both the EIA RS-232 and Mil-Std 188C electrical specifications.

GENERAL PURPOSE – HIGH CURRENT DRIVERS

High Current Drivers are designed with inputs TTL and/or MOS compatible and output stage capable of handline high currents. These circuits are ideal as lamp, relay, LED, and memory drivers.

6

PERIPHERAL DRIVERS – 75450 SERIES • 75460 SERIES: Peripheral Drivers are dual monolithic circuits, each circuit consisting of a TTL logic gate and a high current NPN transistor. The NPN transistors are guaranteed to sink 300 mA and hold off 30 volts even when powered down, on high voltage devices 60 volt breakdown is guaranteed.

DEVICE NUMBER	GATE FUNCTION	CIRCUIT FUNCTION	TRANSISTOR CONNECTION MODE	CURRENT CAPABILITY (TYP)
75450	NAND	N/A	External	I_O at V_{OUT} 300 mA at 0.7 V
75451	NAND	AND	Internal	300 mA at 0.7 V
75452	AND	NAND	Internal	300 mA at 0.7 V
75453	NOR	OR	Internal	300 mA at 0.7 V
75454	OR	NOR	Internal	300 mA at 0.7 V
HIGH VOLTAGE (60 V Standoff)				
75460*	NAND	N/A	External	300 mA at 0.7 V
75461*	NAND	AND	Internal	300 mA at 0.7 V
75462*	AND	NAND	Internal	300 mA at 0.7 V
75463*	NOR	OR	Internal	300 mA at 0.7 V
75464*	OR	NOR	Internal	300 mA at 0.7 V

A/D AND D/A SYSTEMS

CURRENT SOURCES

μ A722	10-Bit Current Source
9650	4-Bit Current Source

VOLTAGE REFERENCE

μ A728	Precision Voltage Reference
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D/A SUBSYSTEM

SH8090	10-Bit D/A Converter
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OPERATIONAL AMPLIFIER

μ A772	High Slew Rate Op Amp
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LED DRIVERS

SEGMENT DRIVERS: LED Segment Drivers interface MOS and TTL signals to LED's. The currents can be set for low currents for continuous operation or higher currents for multiplex operation.

DIGIT DRIVERS: LED Digit Drivers are used for multiplex operation for selection of the digit to be turned on. MOS and/or TTL signals are used to select proper digit and each has high output current capability.

SEGMENT DRIVERS

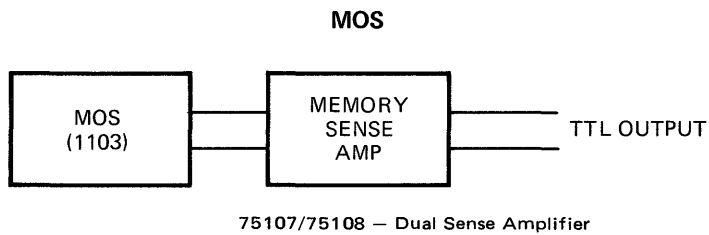
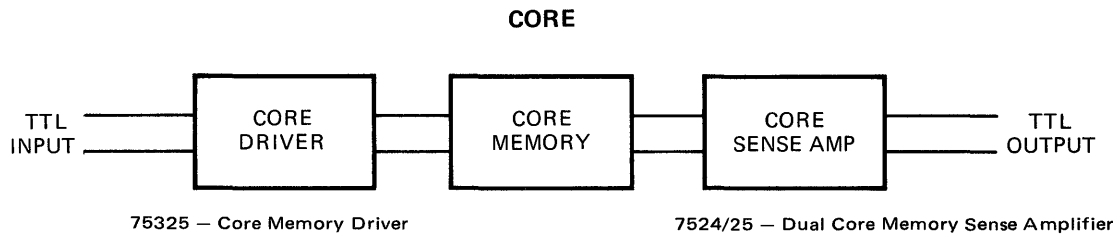
DEVICE NUMBER	INPUT COMPATIBILITY	BCD DECODER	NUMBER OF DRIVERS	MAXIMUM CURRENTS
9660*	TTL and MOS	Yes	7+ Decimal	75 mA
9661*	TTL and MOS	No	4	75 mA
75491	MOS	No	4	50 mA
9307	TTL	Yes	None	N/A
9317	TTL	Yes	7	40 mA
9368	TTL	Yes	7	17 mA
9369	TTL	Yes	7	50 mA
9370	TTL	Yes	7	25 mA

DIGIT DRIVER

DEVICE NUMBER	INPUT COMPATIBILITY	NUMBER OF DRIVERS	MAXIMUM CURRENT CAPABILITY
9662*	TTL and MOS	4	V_O at $I_O = 600$ mA = 0.75 V Max
9663*	TTL and MOS	6	V_O at $I_O = 600$ mA = 0.75 V Max
75492	MOS	4	V_O at $I_O = 250$ mA = 1.7 V Max

*New Products to be announced in 1973.

SELECTION GUIDE FOR MEMORY SYSTEMS



MOS CLOCK DRIVER
SH0013 Two Phase MOS Clock Driver

TAPE AND DISC FILE AMPLIFIERS

μ A733 Video Amplifier
 μ A739 Dual Low Noise Preamplifier

μA722

10-BIT CURRENT SOURCE

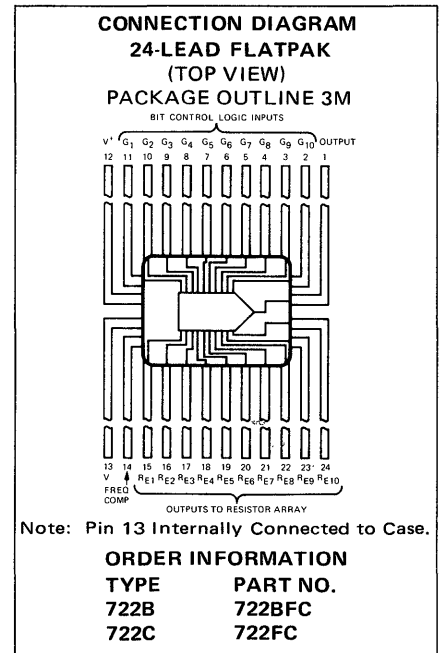
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA722 is a monolithic high-speed, 10-Bit Precision Current Source intended for use in current summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed, using the Fairchild Planar* epitaxial process, and consists of a reference supply, ten current sources connected to a single output summing line, and associated logic switches. The full scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722 is compatible with the Fairchild families of linear and digital circuits.

- 8 ± 1/2 BIT ACCURACY FROM 0°C TO +55°C
- 7 ± 1/2 BIT ACCURACY FROM -20°C TO +85°C
- 600 ns SWITCHING SPEED
- INTERNAL PRECISION REFERENCE
- TTL COMPATIBLE

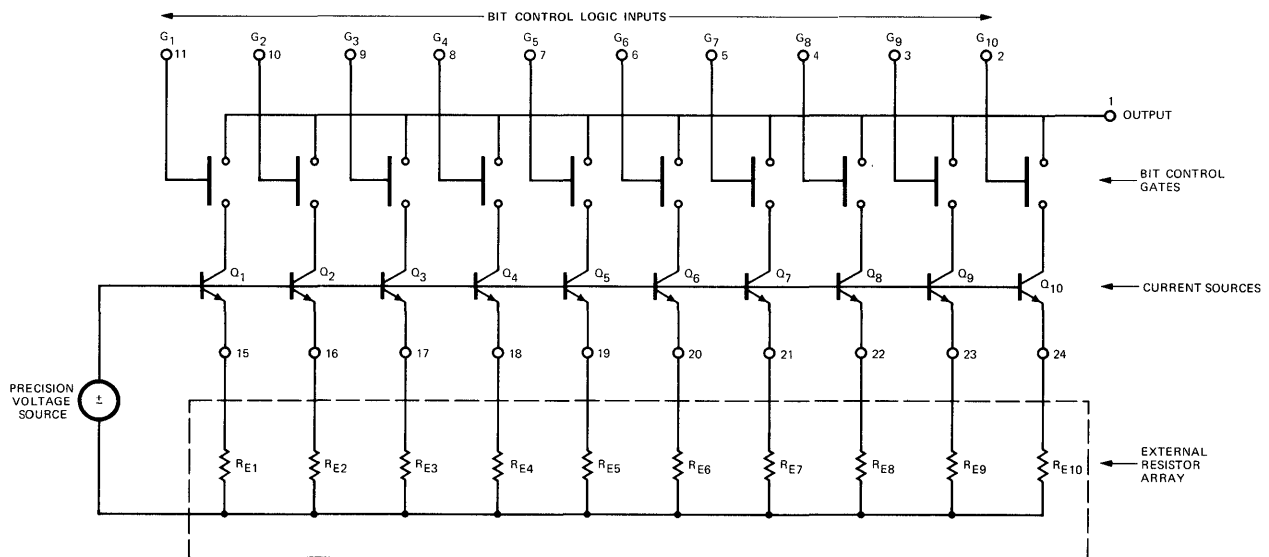
ABSOLUTE MAXIMUM RATINGS

Voltage from V ₊ to V ₋	-0.5 V to +18 V
Voltage from Output to V ₊	-12 V to +6 V
Voltage from Output to V ₋	0 V to +12 V
Voltage from Logic Inputs to Output	-9 V to +7 V
Voltage from Logic Inputs to V ₊	-18 V to 0 V
Voltage from Logic Inputs to V ₋	0 V to +12 V
Internal Power Dissipation (Note 1)	450 mW
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C



6

EQUIVALENT CIRCUIT



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A722

722B

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution					10	Bits
Absolute Error		$T_A = 25^\circ\text{C}$		$\pm.07$	$\pm.20$	%
		$0^\circ\text{C} \leq T_A \leq +55^\circ\text{C}$		$\pm.10$	$\pm.20$	%
		$-20^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		$\pm.13$	$\pm.39$	%
Output Current	Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
	Zero-Scale	Logic Inputs = 2.5 V		$\pm.002$	$\pm.25$	μA
Power Supply Rejection		$\Delta V_+ = \Delta V_- = \pm 5\%$		$\pm.06$	± 0.1	%/%
Output Resistance			0.2	1.2		$\text{M}\Omega$
Switching Speed				600		ns
Input HIGH Voltage			2.1	2.5		V
Input LOW Voltage				0.4	0.7	V
Power Consumption				165	250	mW

722C

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution					10	Bits
Absolute Error		$T_A = 25^\circ\text{C}$		$\pm.08$	$\pm.39$	%
		$0^\circ\text{C} \leq T_A \leq +55^\circ\text{C}$		$\pm.17$	$\pm.39$	%
		$-20^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		$\pm.22$	$\pm.78$	%
Output Current	Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
	Zero-Scale	Logic Inputs = 2.5 V		$\pm.002$	$\pm.25$	μA
Power Supply Rejection		$\Delta V_+ = \Delta V_- = \pm 5\%$		$\pm.06$	± 0.1	%/%
Output Resistance			0.2	1.2		$\text{M}\Omega$
Switching Speed				600		ns
Input HIGH Voltage			2.1	2.5		V
Input LOW Voltage				0.4	0.7	V
Power Consumption				165	250	mW

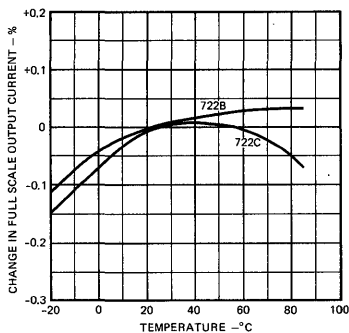
NOTES

- Rating applies for ambient temperatures to $+85^\circ\text{C}$.
- Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V^+ = 6.00\text{ V} \pm 0.1\text{ V}$, $V^- = -6.00\text{ V} \pm 0.1\text{ V}$, $V_{\text{out}} = 0\text{ V}$, $C_I = 200\text{ pF}$, and external resistor array as per Table 1.
- In Table 1, the maximum absolute value tolerance for $R_{E1} = \pm 10\%$.

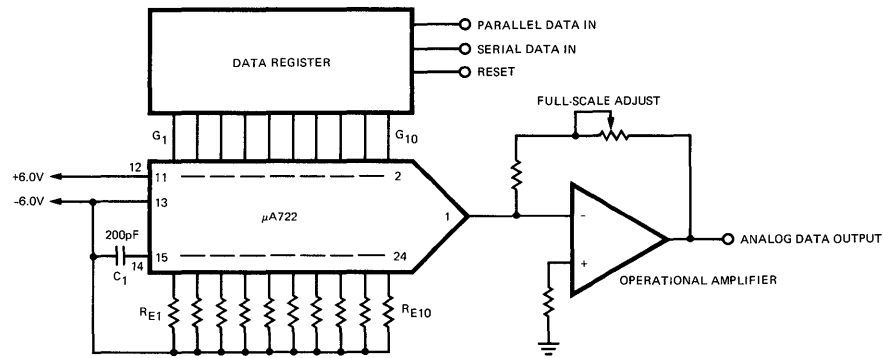
TABLE 1
BINARY CODE RESISTOR ARRAY
FOR $8 \pm 1/2$ BIT ACCURACY

Resistor Number (R_{Ej})	Nominal Value (k Ω)	Nominal Ratio (R_{Ej}/R_{E1})	722B		722C	
			Max. Ratio Tolerance ($T_A = 25^\circ\text{C}$) (%)	Max. Ratio Temp. Coeff. (ppm/ $^\circ\text{C}$)	Max. Ratio Tolerance ($T_A = 25^\circ\text{C}$) (%)	Max. Ratio Temp. Coeff. (ppm/ $^\circ\text{C}$)
R_{E1}	2.547	1.000	Note 3	± 5	Note 3	± 20
R_{E2}	5.094	2.000	± 0.02	± 5	± 0.10	± 20
R_{E3}	10.245	4.022	± 0.05	± 10	± 0.20	± 50
R_{E4}	20.60	8.088	± 0.10	± 20	± 0.20	± 50
R_{E5}	41.43	16.265	± 0.20	± 20	± 0.50	± 100
R_{E6}	81.93	32.17	± 0.20	± 50	± 0.50	± 100
R_{E7}	163.4	64.16	± 0.50	± 100	± 1.0	± 500
R_{E8}	325.7	127.9	± 1.0	± 200	± 1.0	± 500
R_{E9}	644.9	253.2	± 2.0	± 500	± 5.0	± 1000
R_{E10}	1275	500.8	± 2.0	± 500	± 5.0	± 1000

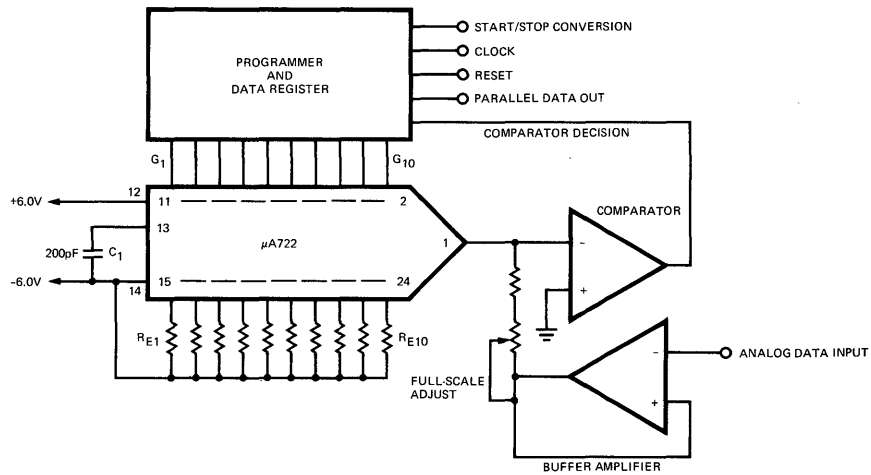
TYPICAL FULL-SCALE OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



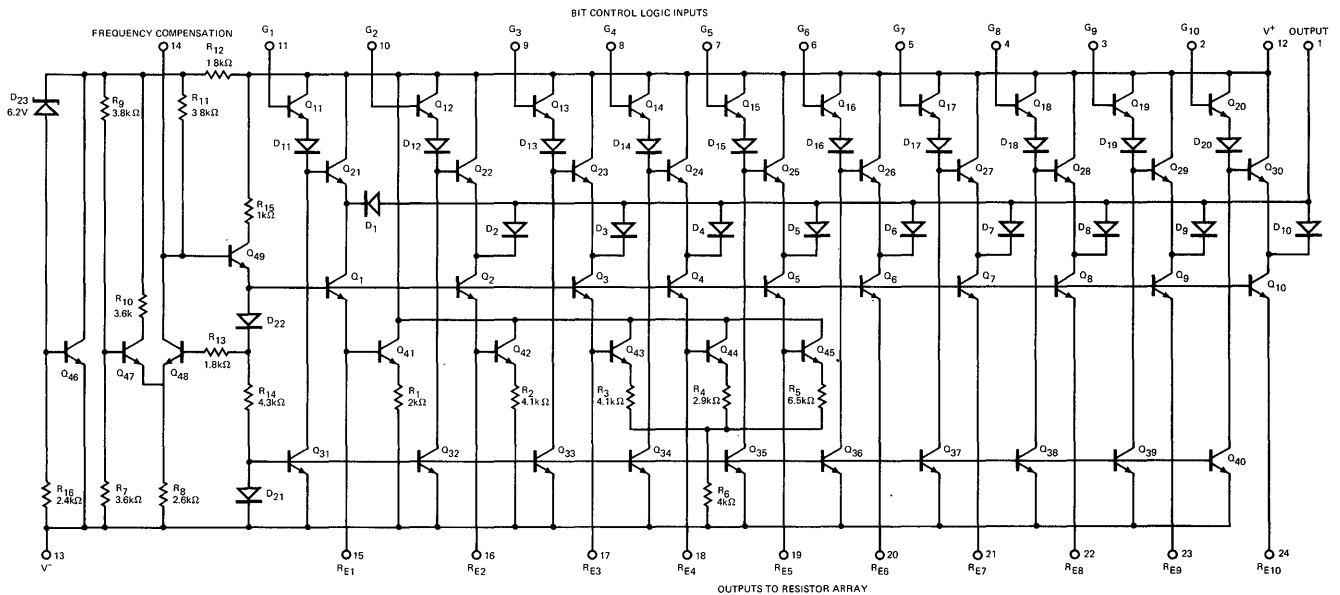
TYPICAL DIGITAL-TO-ANALOG CONVERTER



TYPICAL ANALOG-TO-DIGITAL CONVERTER



EQUIVALENT CIRCUIT



μA733

DIFFERENTIAL VIDEO AMPLIFIER

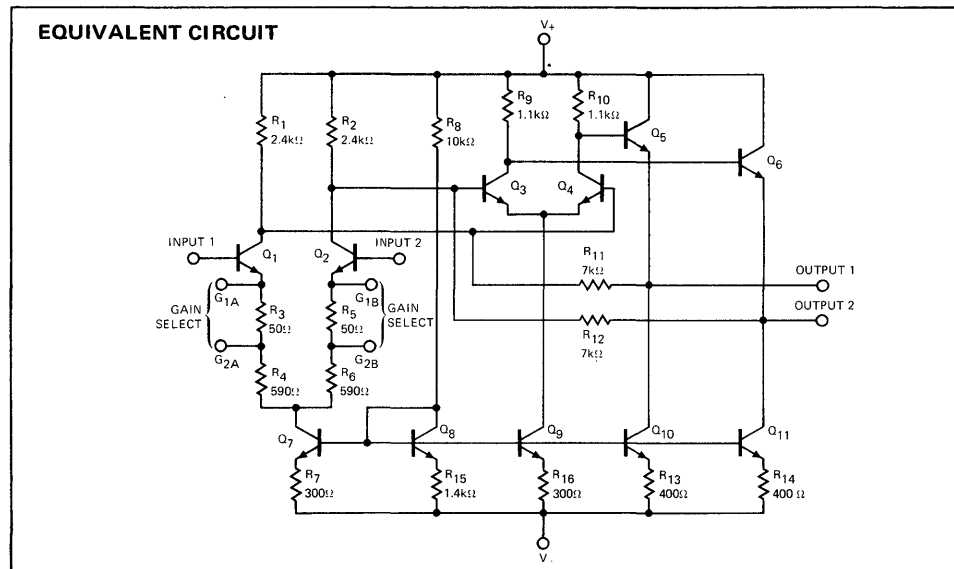
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier constructed using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

- 120 MHz BANDWIDTH
- 250 kΩ INPUT RESISTANCE
- SELECTABLE GAINS OF 10, 100, AND 400
- NO FREQUENCY COMPENSATION REQUIRED

ABSOLUTE MAXIMUM RATINGS

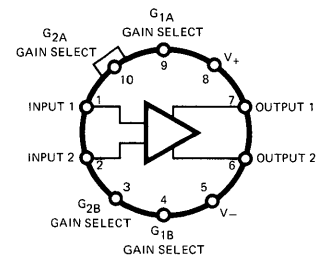
Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Flatpak	570 mW
DIP	670 mW
Operating Temperature Range	
Military (733)	-55° C to +125° C
Commercial (733C)	0° C to +70° C
Storage Temperature Range	-65° C to +150° C
Lead Temperature (Soldering, 60 second time limit)	300° C



Notes on following pages.

CONNECTION DIAGRAMS

**10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F**

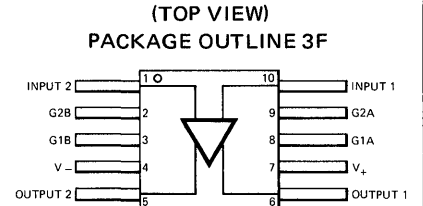


Note: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
733	733HM
733C	733HC

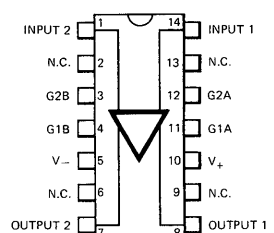
**10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F**



ORDER INFORMATION

TYPE	PART NO.
733	733FM

**14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A**



ORDER INFORMATION

TYPE	PART NO.
733	733DM
733C	733DC

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A733

733

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_S = \pm 6.0\text{ V}$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	$R_S = 50\Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\Omega, V_{OUT} = 1\text{ V}_{p-p}$				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\Omega, V_{OUT} = 1\text{ V}_{p-p}$				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		$k\Omega$
Gain 2		20	30		$k\Omega$
Gain 3			250		$k\Omega$
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	$R_S = 50\Omega, BW = 1\text{ kHz to } 10\text{ MHz}$		12		μV_{rms}
Input Voltage Range		± 1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{CM} = \pm 1\text{ V}, f \leq 100\text{ kHz}$	60	86		dB
Gain 2	$V_{CM} = \pm 1\text{ V}, f = 5\text{ MHz}$		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5\text{ V}$	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

Differential Voltage Gain					
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance					
Gain 2		8.0			$k\Omega$
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		± 1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage					
Gain 1				1.5	V
Gain 2 and Gain 3				1.2	V
Output Swing		2.5			V_{p-p}
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A733

733C

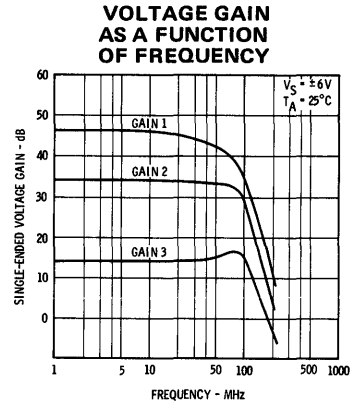
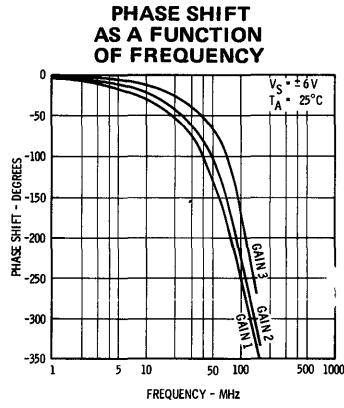
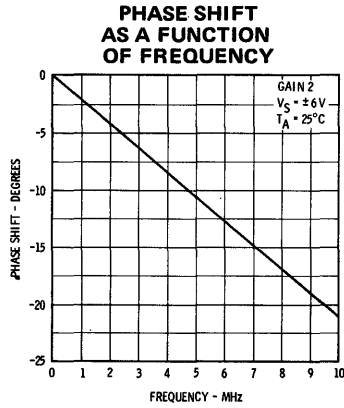
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_S = \pm 6.0\text{ V}$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	$R_S = 50\Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\Omega$, $V_{OUT} = 1\text{ V}_{p-p}$				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\Omega$, $V_{OUT} = 1\text{ V}_{p-p}$				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		$k\Omega$
Gain 2		10	30		$k\Omega$
Gain 3			250		$k\Omega$
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	$R_S = 50\Omega$, BW = 1 kHz to 10 MHz		12		μV_{rms}
Input Voltage Range		± 1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{CM} = \pm 1\text{ V}$, $f \leq 100\text{ kHz}$	60	86		dB
Gain 2	$V_{CM} = \pm 1\text{ V}$, $f = 5\text{ MHz}$		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5\text{ V}$	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA

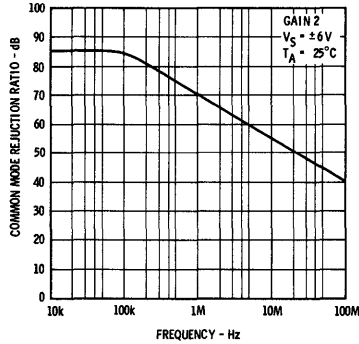
The following specifications apply for $0^\circ\text{C} \leq T_A \leq \pm 70^\circ\text{C}$

Differential Voltage Gain					
Gain 1 (Note 2)		250		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			$k\Omega$
Input Offset Current				6.0	μA
Input Bias Current				40	μA
Input Voltage Range		± 1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{CM} = \pm 1\text{ V}$, $f \leq 100\text{ kHz}$	50			dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5\text{ V}$	50			dB
Output Offset Voltage (All Gain)				1.5	V
Output Voltage Swing		2.8			V_{p-p}
Output Sink Current		2.5			mA
Power Supply Current				27	mA

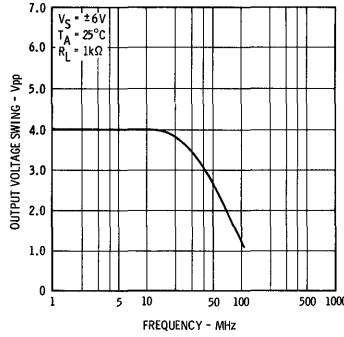
TYPICAL PERFORMANCE CURVES FOR 733 AND 733C



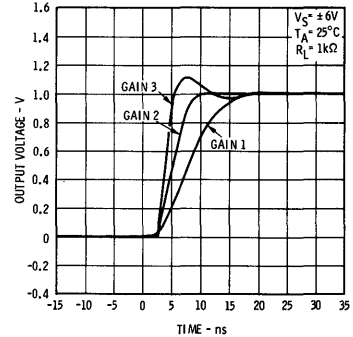
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



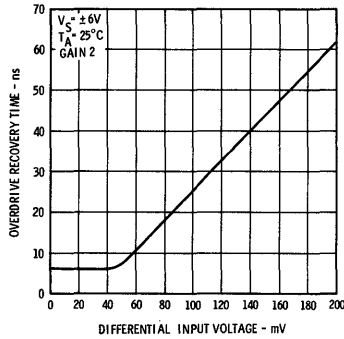
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



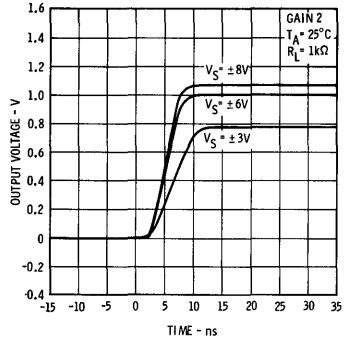
PULSE RESPONSE



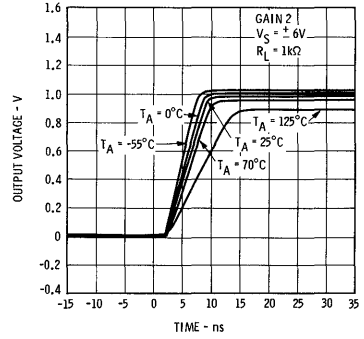
DIFFERENTIAL OVERDRIVE RECOVERY TIME



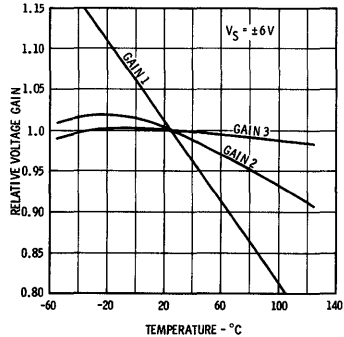
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



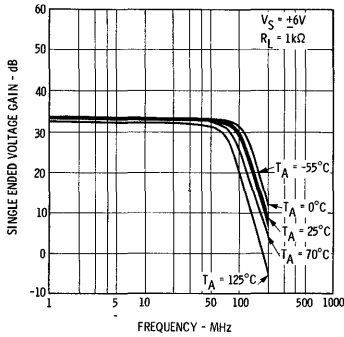
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



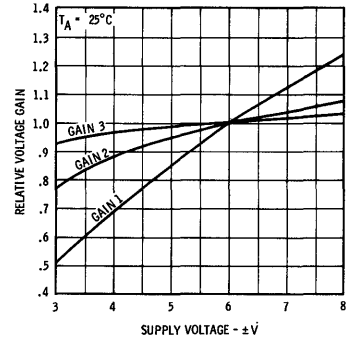
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE

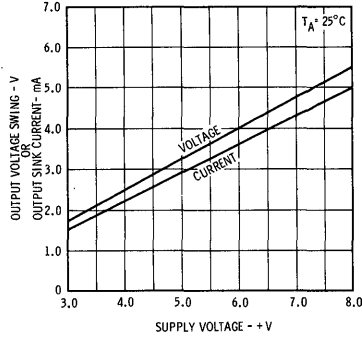


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

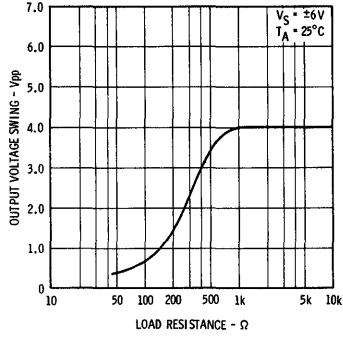


TYPICAL PERFORMANCE CURVES FOR 733 AND 733C

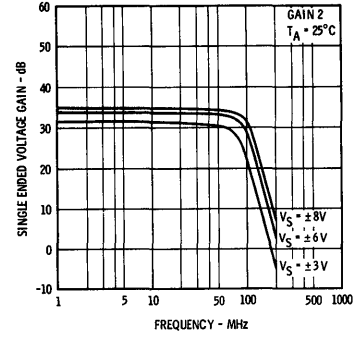
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



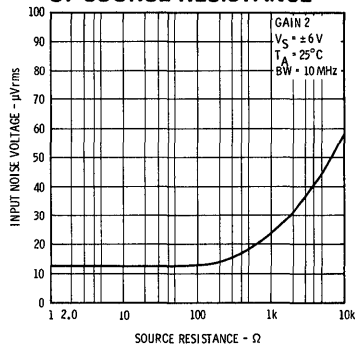
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



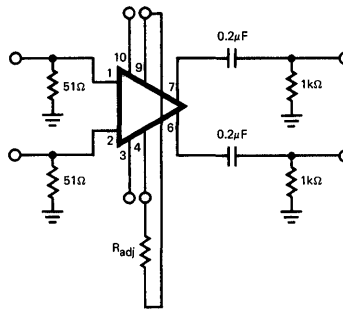
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



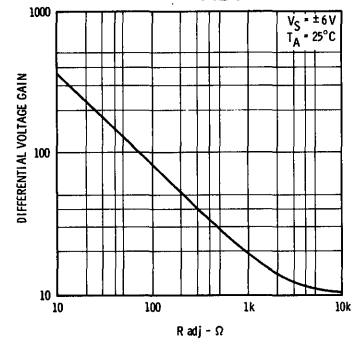
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



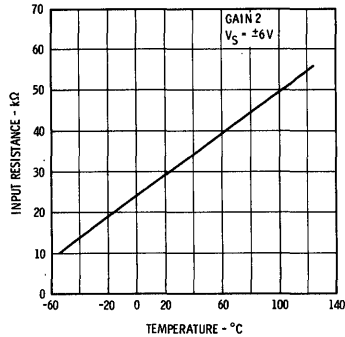
VOLTAGE GAIN ADJUST CIRCUIT



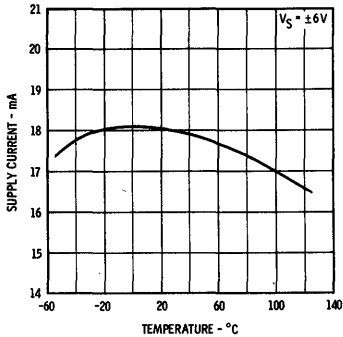
VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}



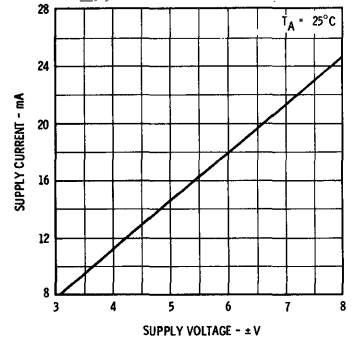
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

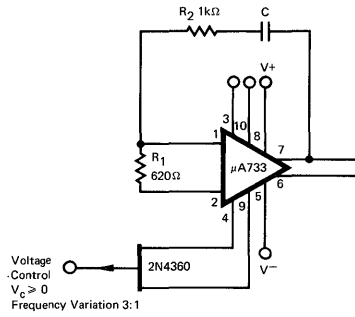


NOTES

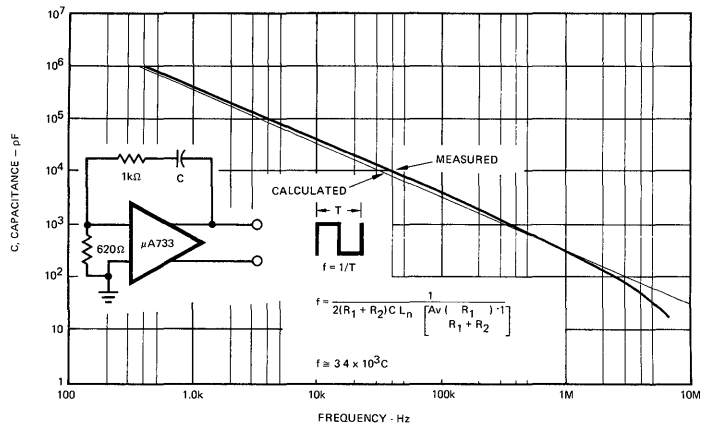
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP and 7.1 mW/°C for the Flatpak.
2. Gain Select pins G_{1A} and G_{1B} connected together.
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

TYPICAL APPLICATIONS

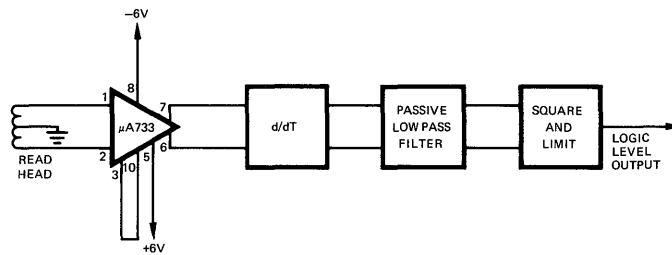
VOLTAGE CONTROLLED OSCILLATOR



OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



PHASE ENCODING PLAYBACK SYSTEM



- Phase Linearity: $\pm 4^\circ$ from 2 to 5 MHz
- Input Resistance: 30 k Ω
- Input Capacity: 2 pF
- Fixed Gain: 100

TTL/MSI 9307

SEVEN SEGMENT DECODER

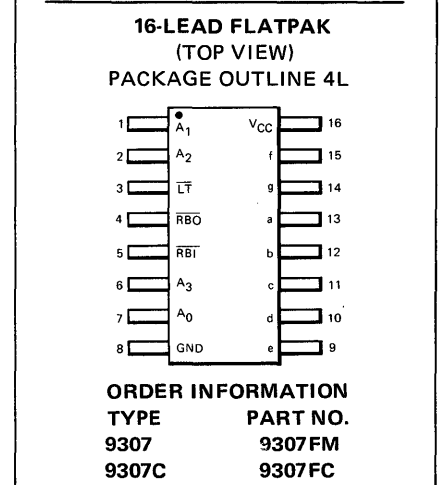
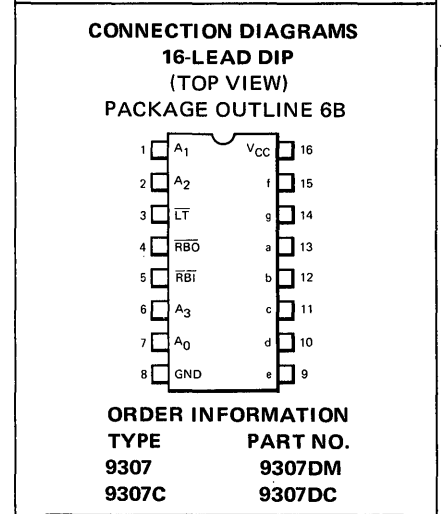
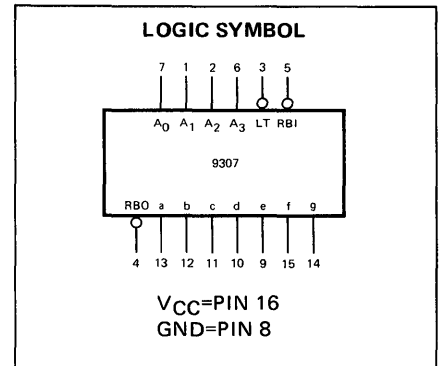
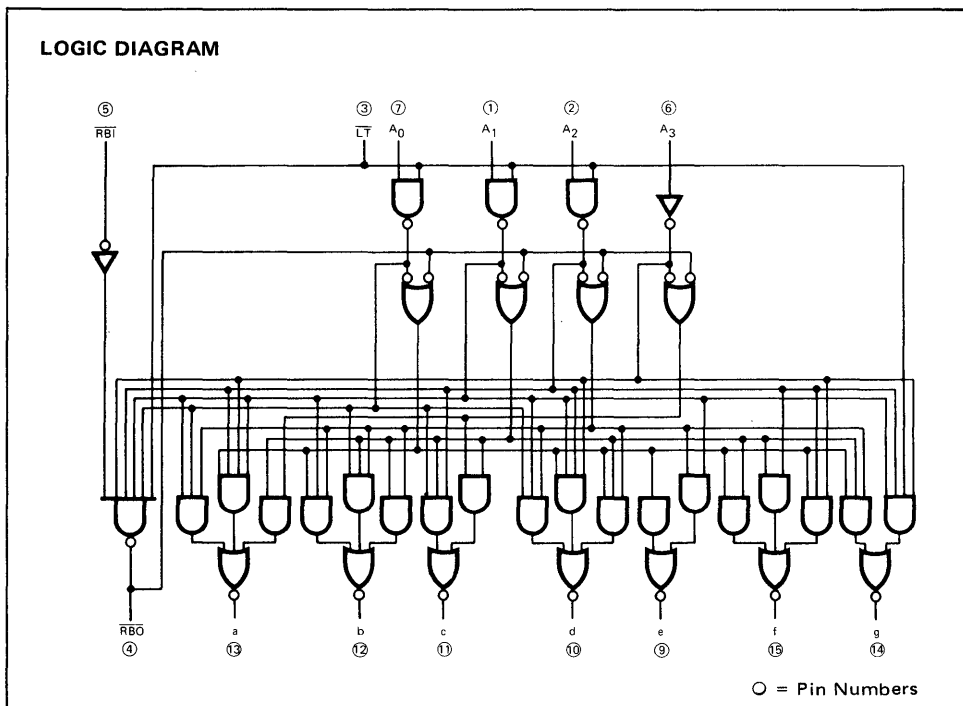
FOR ADDITIONAL INFORMATION SEE THE FAIRCHILD TTL DATA BOOK

DESCRIPTION — The 9307 is a Seven Segment Decoder designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used with seven segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays. The 9307 is compatible with all other Fairchild TTL devices.

- TTL COMPATIBLE
- AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES
- LAMP INTENSITY MODULATION CAPABILITY
- LAMP TEST FACILITY
- BLANKING INPUT
- ACTIVE HIGH OUTPUTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7 V
Voltage Applied to Outputs for HIGH Output State	-0.5 V to +V _{CC} value
Input Voltage (dc)	-0.5 V to +5.5 V



TTL/MSI 9317B • 9317C

SEVEN SEGMENT DECODER/DRIVER

FOR ADDITIONAL INFORMATION SEE THE FAIRCHILD TTL DATA BOOK.

DESCRIPTION — The 9317 is a TTL/MSI Seven Segment Decoder/Driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used to directly drive seven segment incandescent lamp displays and light emitting diode indicators (or indirectly drive neon, electro-luminescent, numeric displays). The 9317 is compatible with all members of the Fairchild TTL family.

The 9317 is available in two output current and latch voltage versions, the 9317B and C.

- TTL COMPATIBLE
- AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS
- LAMP INTENSITY MODULATION CAPABILITY
- LAMP TEST FACILITY
- BLANKING INPUT
- ACTIVE LOW OUTPUTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE
- DRIVE LAMPS DIRECTLY
- CODES IN EXCESS OF BINARY 9 DISABLE OUTPUTS
- ENHANCED RELIABILITY WITH UNIQUE NUMERIC ONE DISPLAY POSITION

PIN NAMES

A_0, A_1, A_2, A_3	Address Inputs
\overline{LT}	Lamp Test (Active LOW) Input
\overline{RBI}	Ripple Blanking (Active LOW) Input
\overline{RBO}	Ripple Blanking (Active LOW) Output
$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$	(Active LOW) Outputs

1 Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW

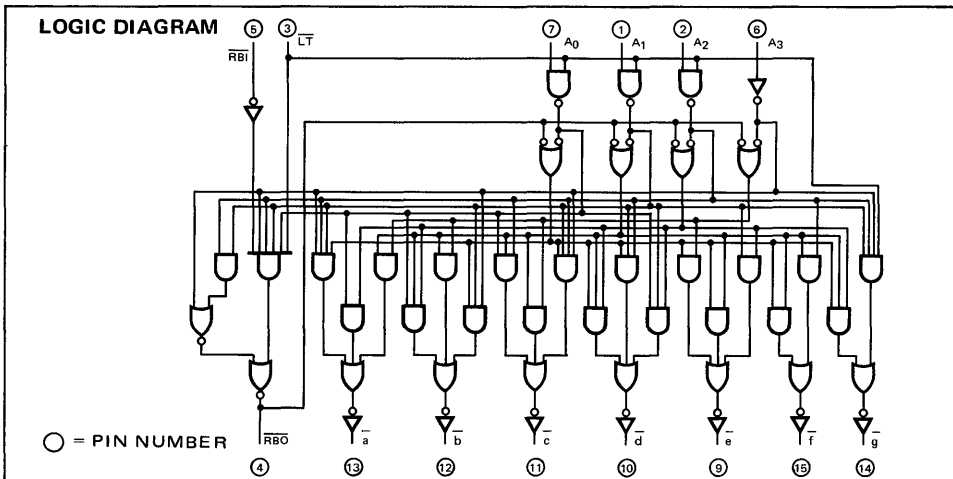
LOADING

	HIGH	LOW
A_0, A_1, A_2, A_3	1.0 U.L.	1.0 U.L.
\overline{LT}	5.0 U.L.	4.0 U.L.
\overline{RBI}	1.0 U.L.	0.5 U.L.
\overline{RBO}	1.5 U.L.	1.5 U.L.

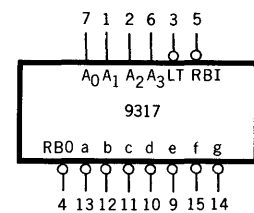
See Options

OPTIONS

PARAMETER	9317B	9317C
Latch Voltage	20 Volts	30 Volts
Output Current (Pins 9 through 15)	40 mA	20 mA

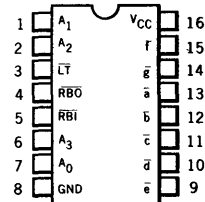


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

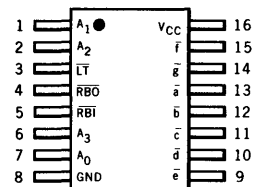
CONNECTION DIAGRAMS 16-LEAD DIP (TOP VIEW) PACKAGE OUTLINE 7B



ORDER INFORMATION

TYPE	PART NO.
9317B	9317BDM
9317B	9317BDC
9317C	9317CDM
9317C	9317CDC

16-LEAD FLATPAK (TOP VIEW) PACKAGE OUTLINE 4L



ORDER INFORMATION

TYPE	PART NO.
9317B	9317BFM
9317B	9317BFC
9317C	9317CFM
9317C	9317CFC

TTL/MSI 9368

SEVEN SEGMENT DECODER/DRIVER/LATCH

FOR ADDITIONAL INFORMATION SEE SEPARATE DATA SHEET

DESCRIPTION — The 9368 is a TTL/MSI Seven Segment Decoder Driver incorporating input latches, and output circuits to drive common cathode type LED displays directly.

- HIGH SPEED INPUT LATCHES FOR DATA STORAGE
- DRIVES COMMON CATHODE LED DISPLAYS DIRECTLY
- ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS
- HEXADECIMAL DECODE FORMAT
- LATCH SPEED COMPARABLE TO STANDARD MSI LATCHES
- DATA INPUT FAN IN ZERO WHEN LATCH NOT ENABLED*
- AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS
- PINOUT COMPARABLE WITH OTHER STANDARD MSI DECODERS SUCH AS 9307, 9317, 9357A (7446), 9357B (7447), 9358 (7448), 9359 (7449)

PIN NAMES

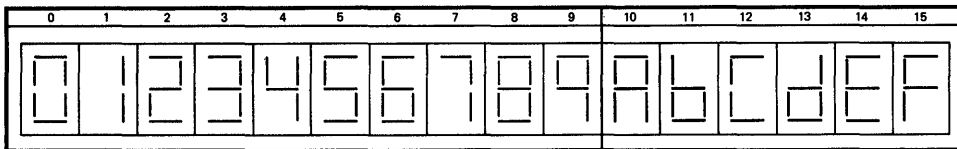
A_0, A_1, A_2, A_3	Address Inputs
\overline{EL}	Latch Enable
\overline{RBI}	Ripple Blanking (Active LOW) Input
RBO	Ripple Blanking (Active LOW) Output
a, b, c, d, e, f, g	(Active HIGH) Outputs

LOADING

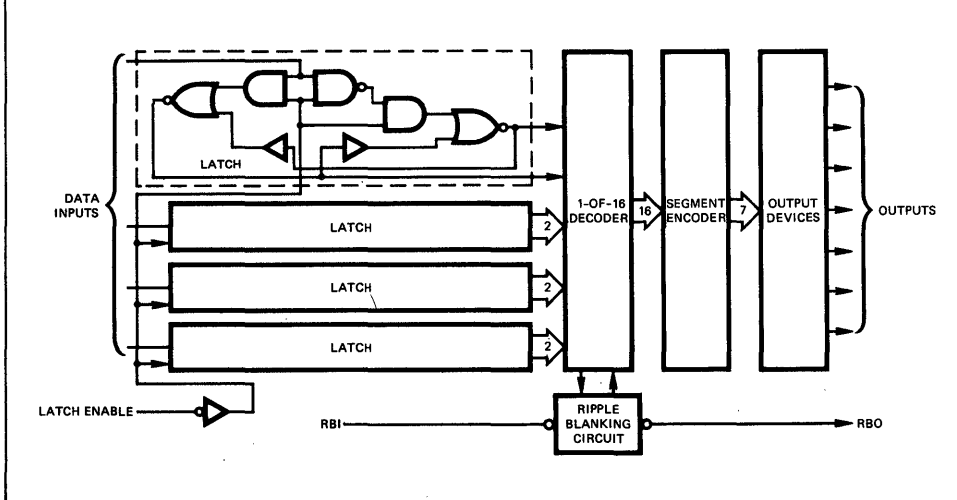
	HIGH	LOW
A_0, A_1, A_2, A_3	2.0 U.L.	1.0 U.L.*
\overline{EL}	1.0 U.L.	1.0 U.L.
\overline{RBI}	1.0 U.L.	1.0 U.L.
RBO	2.0 U.L.	2.0 U.L.
a, b, c, d, e, f, g	20 mA	"OFF"

*LOW level loading is 1 U.L. only when latch is enabled. When latch is disabled loading is 10 μ A.

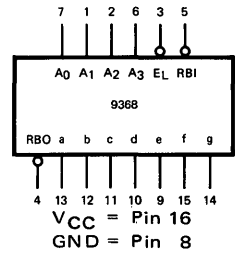
NUMERICAL DESIGNATIONS



BLOCK DIAGRAM



LOGIC SYMBOL

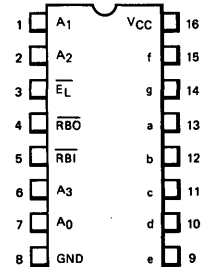


CONNECTION DIAGRAM

16-LEAD DIP

(TOP VIEW)

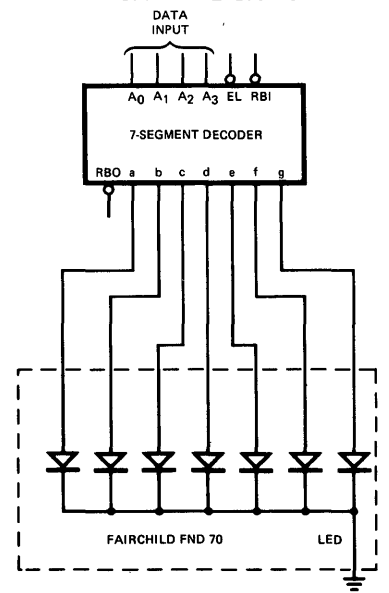
PACKAGE OUTLINE 6B



ORDER INFORMATION

TYPE	PART NO.
9368	9368DC

TYPICAL APPLICATION



TTL/MSI 9369

SEVEN SEGMENT DECODER/DRIVER/LATCH

FOR ADDITIONAL INFORMATION SEE SEPARATE DATA SHEET

DESCRIPTION — The 9369 is a TTL/MSI Seven Segment Decoder Driver incorporating input latches and output circuits to drive common cathode type LED displays. The outputs will source up to 50 mA per output, with one resistor per output needed to limit the current.

- HIGH SPEED INPUT LATCHES FOR DATA STORAGE
- DRIVES COMMON CATHODE LED DISPLAYS WITH UP TO 50 mA PER SEGMENT
- PROVIDES MULTIPLEX DRIVE FOR 10 LED'S RATED AT 5 mA AVERAGE PER SEGMENT
- ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS
- HEXADECIMAL DECODE FORMAT
- LATCH SPEED COMPARABLE TO STANDARD MSI LATCHES
- DATA INPUT FAN IN ZERO WHEN LATCH NOT ENABLED*
- AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS
- PINOUT COMPARABLE WITH OTHER STANDARD MSI DECODERS SUCH AS 9307, 9317, 9357A (7446), 9357B (7447), 9358 (7448)

PIN NAMES

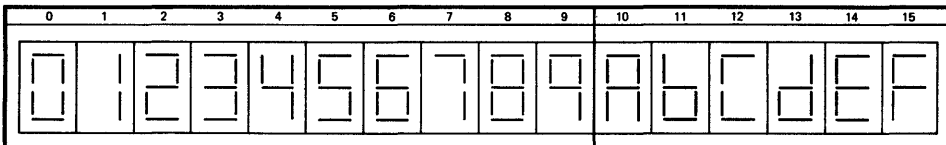
A_0, A_1, A_2, A_3	Address Inputs
$\overline{E_L}$	Latch Enable
\overline{RBI}	Ripple Blanking (Active LOW) Input
\overline{RBO}	Ripple Blanking (Active LOW) Output
a, b, c, d, e, f, g	(Active HIGH) Output Source Current

LOADING	
HIGH	LOW
2.0 U.L.	1.0 U.L.*
1.0 U.L.	1.0 U.L.
1.0 U.L.	1.0 U.L.
2.0 U.L.	2.0 U.L.
50 mA	"OFF"

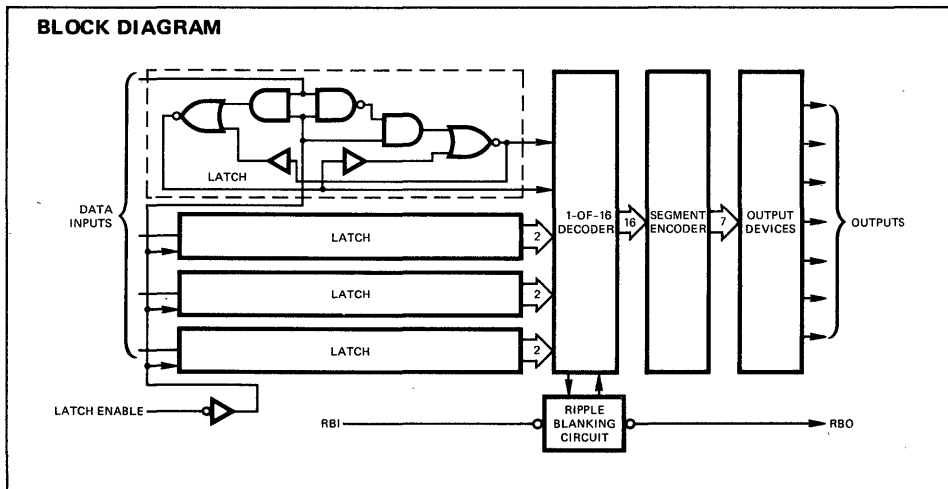
1 Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW

*LOW level loading is 1 U.L. only when latch is enabled. When latch is disabled loading is 10 μ A.

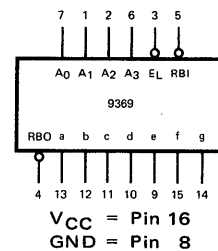
NUMERICAL DESIGNATIONS



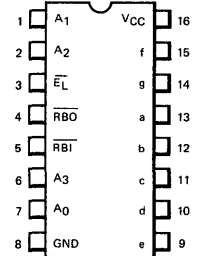
BLOCK DIAGRAM



LOGIC SYMBOL

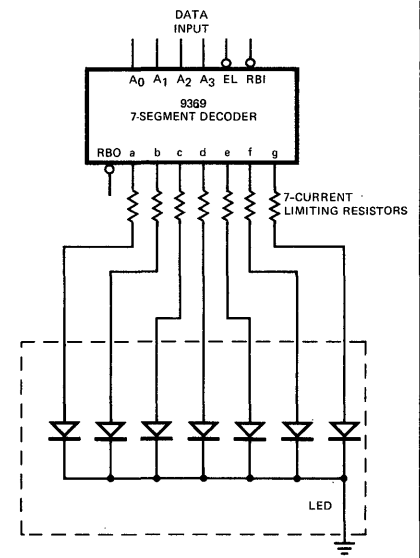


CONNECTION DIAGRAM 16-LEAD DIP (TOP VIEW) PACKAGE OUTLINE 6B



ORDER INFORMATION TYPE PART NO. 9369 9369DC

TYPICAL APPLICATION



TTL/MSI 9370

SEVEN SEGMENT DECODER/DRIVER/LATCH

FOR ADDITIONAL INFORMATION SEE SEPARATE DATA SHEET

DESCRIPTION — The 9370 is a TTL/MSI Seven Segment Decoder Driver incorporating input latches and output circuits to drive incandescent displays directly. It can also be used to drive common anode LED displays in either a multiplexed mode or directly with the aid of external current limiting resistors.

- HIGH SPEED INPUT LATCHES FOR DATA STORAGE
- 25 mA SINK CAPABILITY TO DRIVE EITHER INCANDESCENT OR COMMON ANODE LED DISPLAYS
- HEXADECIMAL DECODE FORMAT
- ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS
- DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH IS DISABLED*
- AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZERO'S AND/OR TRAILING EDGE ZERO'S
- PINOUT COMPATIBLE WITH OTHER STANDARD MSI DECODERS SUCH AS 9307, 9317, 9357A (7446), 9357B (7447), 9358 (7448)

PIN NAMES

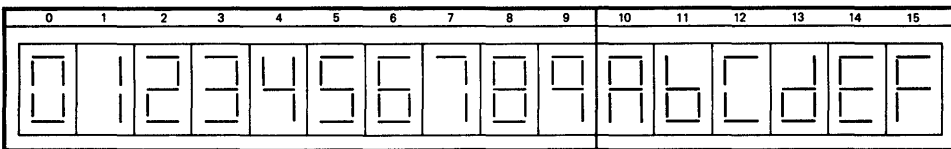
A_0, A_1, A_2, A_3	Address Inputs
\overline{EL}	Latch Enable
\overline{RBI}	Ripple Blanking (Active LOW) Input
\overline{RBO}	As an Output
\overline{RBO}	As an Input
$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$	(Active LOW) Open Collector Outputs

LOADING

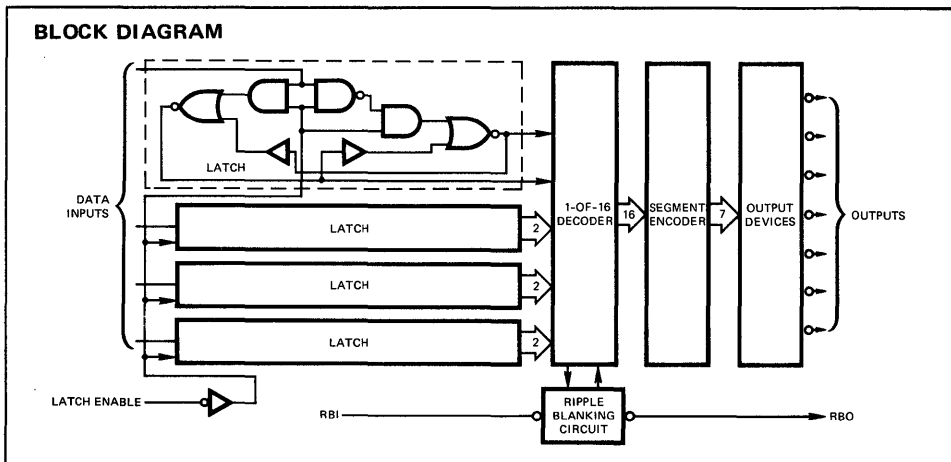
	HIGH	LOW
A_0, A_1, A_2, A_3	2.0 U.L.	1.0 U.L.*
\overline{EL}	1.0 U.L.	1.0 U.L.
\overline{RBI}	1.0 U.L.	1.0 U.L.
\overline{RBO} (As an Output)	2.0 U.L.	2.0 U.L.
\overline{RBO} (As an Input)	1.0 U.L.	2.0 U.L.
$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$	"OFF"	25 mA

* LOW level loading is 1 U.L. only when latch is enabled. When latch is disabled loading is 10 μ A.

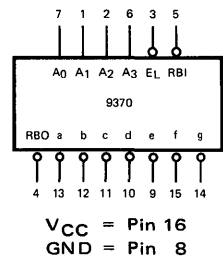
NUMERICAL DESIGNATIONS



BLOCK DIAGRAM



LOGIC SYMBOL

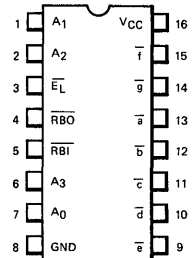


CONNECTION DIAGRAM

16-LEAD DIP

(TOP VIEW)

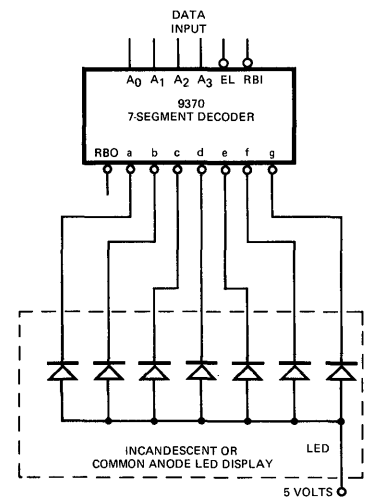
PACKAGE OUTLINE 6B



ORDER INFORMATION

TYPE	PART NO.
9370	9370DC

TYPICAL APPLICATION



9614

DUAL DIFFERENTIAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9614 is a TTL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTL, with the active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other (See Fig. 5). The active pull-up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing NAND and AND functions of the inputs, adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both input and output to handle line transients.

- SINGLE 5 VOLT SUPPLY
- TTL COMPATIBLE INPUTS
- OUTPUT SHORT CIRCUIT PROTECTION
- INPUT CLAMP DIODES
- OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS
- COMPLEMENTARY OUTPUTS FOR NAND, AND OPERATION
- UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR APPLICATION
- MILITARY TEMPERATURE RANGE

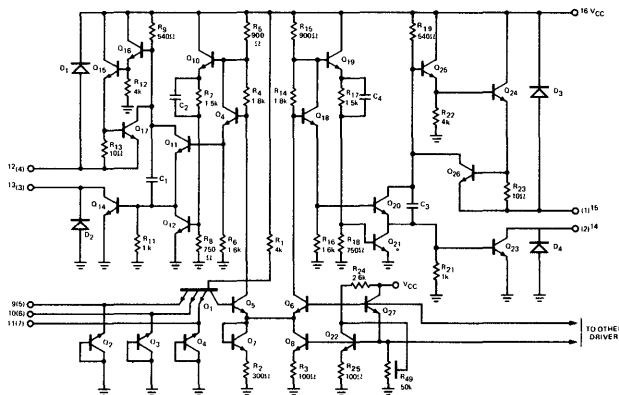
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature Range	-65°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.7 V to +7.0 V
Input Voltage	-0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	-0.5 V to +12 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (9614)	-55°C to +125°C
Commercial (9614C)	0°C to +75°C

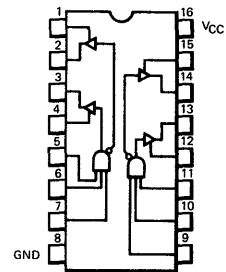
NOTE:

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the DIP and 7.1 mW/°C for the Flatpak.

EQUIVALENT CIRCUIT (1/2 9614)



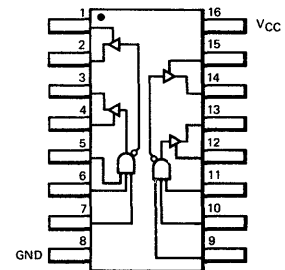
CONNECTION DIAGRAM
16-LEAD DIP
 (TOP VIEW)
 PACKAGE OUTLINE 8B



ORDER INFORMATION

TYPE	PART NO.
9614	9614DM
9614C	9614DC

16-LEAD FLATPAK
 (TOP VIEW)
 PACKAGE OUTLINE 4L



ORDER INFORMATION

TYPE	PART NO.
9614	9614FM

9614

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 10\%$)

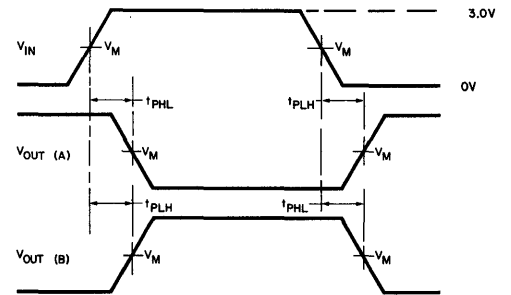
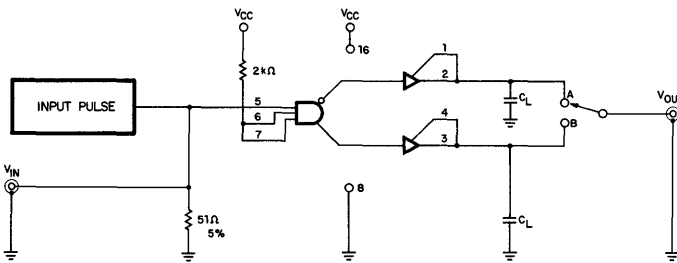
SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		-55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		400		200	400			mV	$I_{GL} = 40 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$
V_{OH}	Output HIGH Voltage	2.4		2.4	3.2		2.4		V	$I_{OH} = -10 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$
I_{SC}	Output Short-Circuit Current			-40	-90	-120			mA	$V_{OUT} = 0.0 \text{ V}$ $V_{CC} = 5.5 \text{ V}$
I_{CEX}	Output Leakage Current				10	100		200	μA	$V_{CEX} = 12.0 \text{ V}$ $V_{CC} = 5.5 \text{ V}$
I_F	Input Forward Current		-1.60		-1.10	-1.60		-1.60	mA	$V_F = 0.4 \text{ V}$ $V_{CC} = 5.5 \text{ V}$
I_R	Input Reverse Current				35	60		100	μA	$V_R = 4.5 \text{ V}$ $V_{CC} = 5.5 \text{ V}$
V_{IL}	Input LOW Voltage		0.8		1.3	0.8		0.8	V	$V_{CC} = 5.5 \text{ V}$
V_{IH}	Input HIGH Voltage	2.0		2.0	1.5		2.0		V	$V_{CC} = 4.5 \text{ V}$
V_{OLC}	Clamped Output LOW Voltage				-0.8	-1.5			V	$I_{OLC} = -40 \text{ mA}$ $V_{CC} = 5.5 \text{ V}$
I_{CC}	Supply Current				34	50			mA	Inputs = 0 V $V_{CC} = 5.5 \text{ V}$
I_{max}	Supply Current				46	65			mA	Inputs = 0 V $V_{max} = 7.0 \text{ V}$
t_{PLH}	Turn-Off Time				14	20			ns	$C_L = 30 \text{ pF}$ $V_{CC} = 5.0 \text{ V}$
t_{PHL}	Turn-On Time				18	20			ns	See Fig. 1 $V_M = 1.5 \text{ V}$
V_{CD}	Input Clamp Diode Voltage				-1.0	-1.5			V	$V_{CC} = 4.5 \text{ V}$ $I_{IC} = -12 \text{ mA}$

9614C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		450		200	450		450	mV	$I_{OL} = 40 \text{ mA}$ $V_{CC} = 4.75 \text{ V}$
V_{OH}	Output HIGH Voltage	2.4		2.4	3.2		2.4		V	$I_{OH} = -10 \text{ mA}$ $V_{CC} = 4.75 \text{ V}$
I_{SC}	Output Short-Circuit Current			-40	-90	-120			mA	$V_{OUT} = 0.0 \text{ V}$ $V_{CC} = 5.25 \text{ V}$
I_{CEX}	Output Leakage Current				10	100		200	μA	$V_{CEX} = 5.25 \text{ V}$ $V_{CC} = 5.25 \text{ V}$
I_F	Input Forward Current		-1.60		-1.10	-1.60		-1.60	mA	$V_F = 0.45 \text{ V}$ $V_{CC} = 5.25 \text{ V}$
I_R	Input Reverse Current				35	60		100	μA	$V_R = 4.5 \text{ V}$ $V_{CC} = 5.25 \text{ V}$
V_{IL}	Input LOW Voltage		0.8		1.3	0.8		0.8	V	$V_{CC} = 5.25 \text{ V}$
V_{IH}	Input HIGH Voltage	2.0		2.0	1.5		2.0		V	$V_{CC} = 4.75 \text{ V}$
V_{OLC}	Clamped Output LOW Voltage				-0.8	-1.5			V	$I_{OLC} = -40 \text{ mA}$ $V_{CC} = 5.25 \text{ V}$
I_{CC}	Supply Current				33	50			mA	Inputs = 0 V $V_{CC} = 5.25$
I_{max}	Supply Current				46	70			mA	Inputs = 0 V $V_{max} = 7.0 \text{ V}$
t_{PLH}	Turn-Off Time				14	30			ns	$C_L = 30 \text{ pF}$ $V_{CC} = 5.0 \text{ V}$
t_{PHL}	Turn-On Time				18	30			ns	See Fig. 1 $V_M = 1.5 \text{ V}$
V_{CD}	Input Clamp Diode Voltage				-1.0	-1.5			V	$V_{CC} = 4.75 \text{ V}$ $I_{IC} = -12 \text{ mA}$

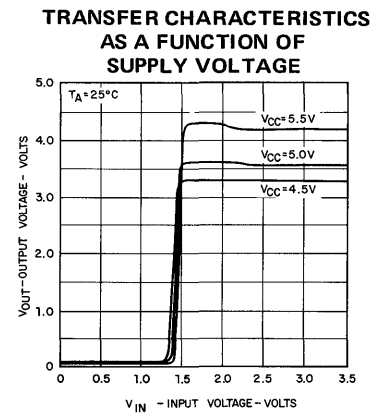
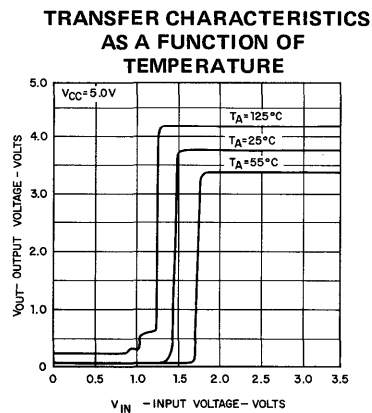
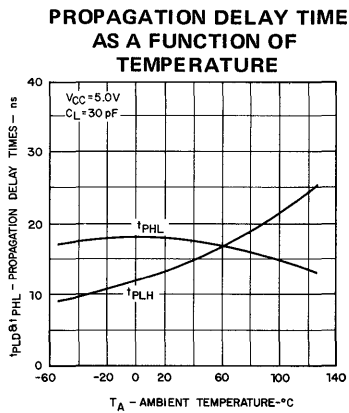
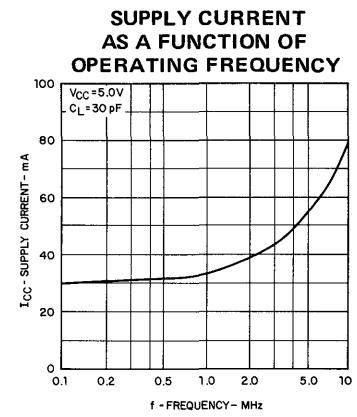
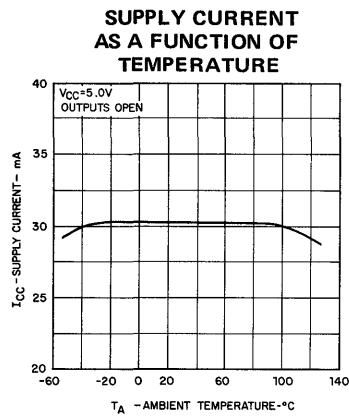
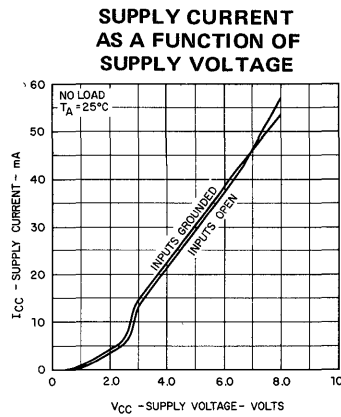
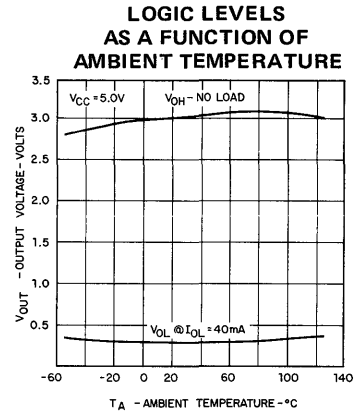
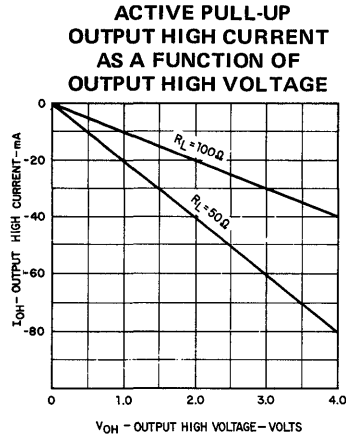
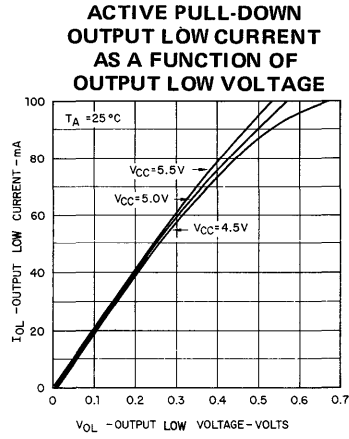
SWITCHING CIRCUIT AND WAVEFORMS



INPUT PULSE
 Frequency = 500 kHz
 Amplitude = $3.0 \pm 0.1 \text{ V}$
 Pulse Width = $110 \pm 10 \text{ ns}$
 $t_r = t_f \leq 5.0 \text{ ns}$

Fig. 1

TYPICAL ELECTRICAL CHARACTERISTICS



APPLICATIONS
DIFFERENTIAL MODE EXPANSION
MULTIPLEX OPERATION

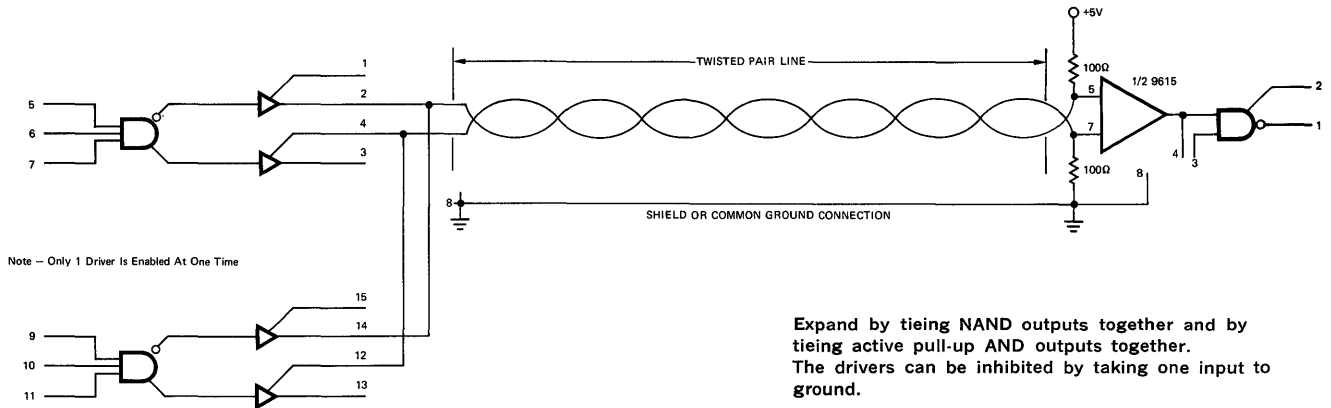
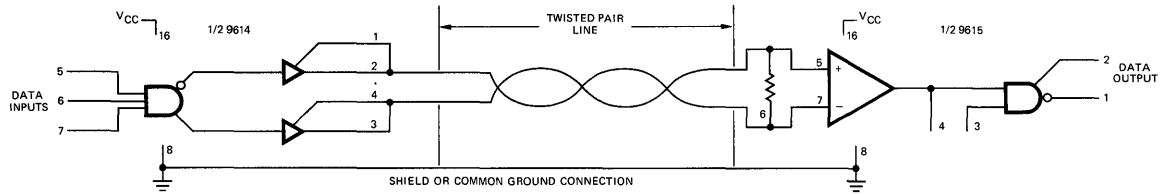


Fig. 2

SIMPLEX-BALANCED DIFFERENTIAL OPERATION



See 9615 Data Sheet for operation of 9615.

Fig. 3

TYPICAL REFLECTION DIAGRAM

NOTE--SEE 9621 DATA SHEET FOR USAGE OF REFLECTION DIAGRAM

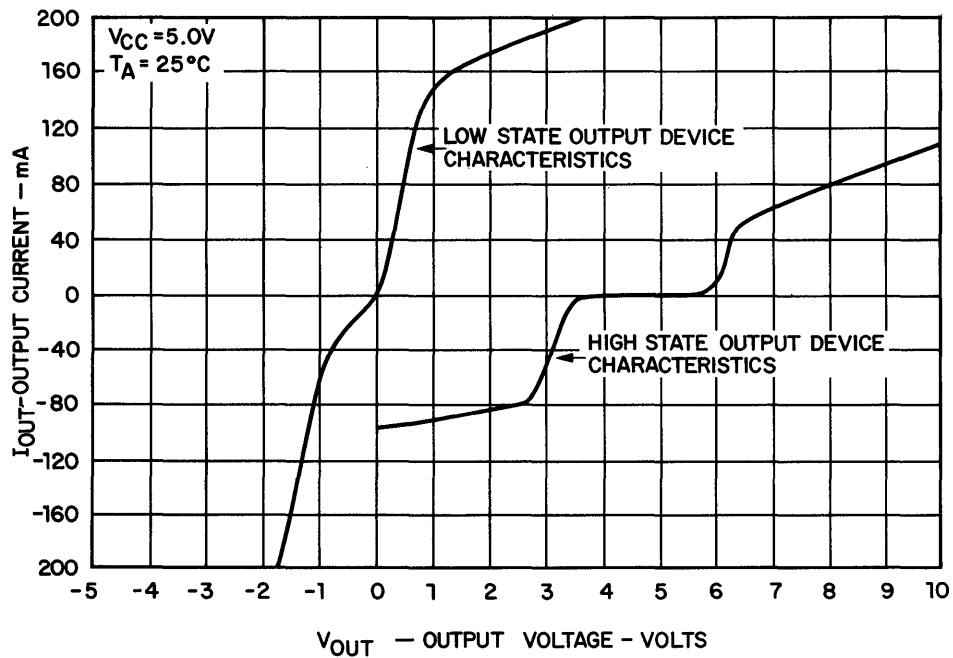


Fig. 4

9615

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9615 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 V supply. It can receive ± 500 mV of differential data in the presence of high level (± 15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe and a 130Ω terminating resistor are provided at the inputs. The output has an uncommitted collector with an active pull-up available on an adjacent pin to allow either wire-OR or active pull up TTL output configuration.

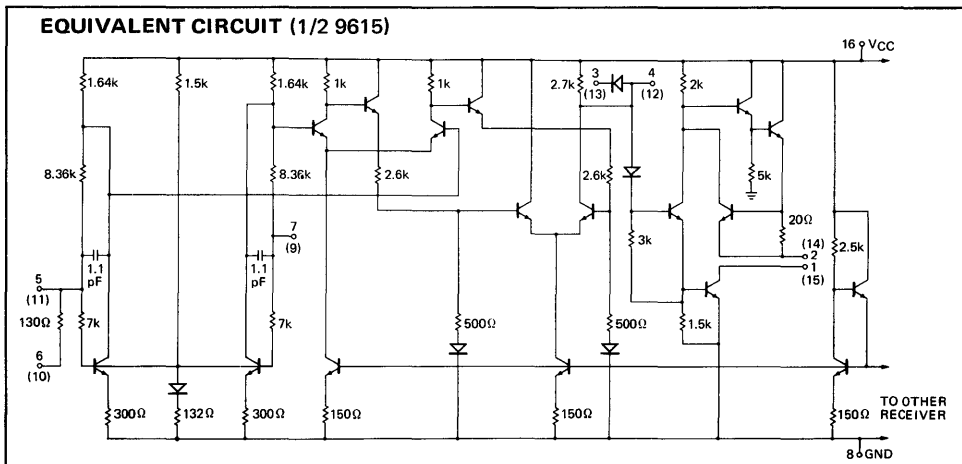
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **CHOICE OF AN UNCOMMITTED COLLECTOR OR ACTIVE PULL-UP**
- **STROBE**
- **FULL MILITARY TEMPERATURE RANGE**
- **SINGLE 5 V SUPPLY VOLTAGES**
- **FREQUENCY RESPONSE CONTROL**
- **130Ω TERMINATING RESISTOR**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

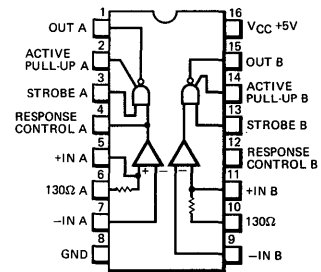
Storage Temperature	-65°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage Referred to Ground (Pins 5, 6, 7, 9, 10, 11)	±20 V
Voltage Applied to Outputs for HIGH output State without Active Pull-Up	-0.5 V to +13.2 V
Voltage Applied to Strobe	-0.5 V to +5.5 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (9615)	-55°C to +125°C
Commercial (9615C)	0°C to +75°C

NOTE:

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the DIP and 7.1 mW/°C for the Flatpak Package.

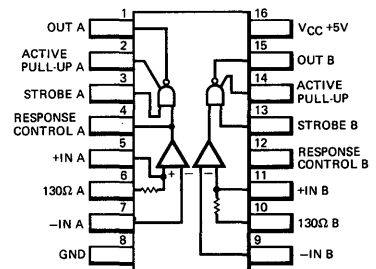


CONNECTION DIAGRAM
16-LEAD DIP
 (TOP VIEW)
 PACKAGE OUTLINE 6B



ORDER INFORMATION	
TYPE	PART NO.
9615	9615DM
9615C	9615DC

16-LEAD FLATPAK
 (TOP VIEW)
 PACKAGE OUTLINE 4C



ORDER INFORMATION	
TYPE	PART NO.
9615	9615FM

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 9615

9615

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS	
		-55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.			MAX.
V _{OL}	Output LOW Voltage		0.40		0.18	0.40		0.40	V	V _{CC} = 4.5 V, V _{OUT} = ** I _{OL} = 15.0 mA, *V _{DIFF} = 0.5 V
V _{OH}	Output HIGH Voltage	2.2		2.4	3.2		2.4		V	V _{CC} = 4.5 V, V _{OUT} = ** I _{OH} = -5.0 mA, *V _{DIFF} = -0.5 V
I _{CEX}	Output Leakage Current					100		200	μA	V _{CEX} = 12 V, *V _{DIFF} = V _{CC} = 4.5 V
I _{SC}	Output Shorted Current			-15	-39	-80			mA	V _{CC} = 5.5 V, **V _{SC} = 0 V, *V _{DIFF} = -0.5 V
I _{IN}	Input Current		-0.9		-0.49	-0.7		-0.7	mA	V _{CC} = 5.5 V, V _{IN} = 0.4 V Other Input = 5.5 V
I _{IN(ST)}	Strobe Input Current				-1.15	-2.4			mA	V _{CC} = 5.5 V, V _{IN} = 0.4 V *V _{DIFF} = 0.5 V
I _{IN(R-C)}	Response Control Input Current			-1.2	-3.4				mA	V _{CC} = 5.5 V, *V _{DIFF} = 0.5 V
V _{CM}	Common Mode Voltage	-15	+15	-15	±17.5	+15	-15	+15	V	V _{CC} = 5.0 V, *V _{DIFF} = +1.0V
I _{R(ST)}	Strobe Input Leakage Current					2.0		5.0	μA	V _{CC} = 4.5 V, *V _{DIFF} = -0.5 V V _R = 4.5 V
R _{IN}	Input Resistor			77	130	167			Ω	V _{CC} = 5.0 V, V _{IN(R)} = 1.0 V, +Input = GND
V _{TH} ***	Differential Input Threshold Voltage	-500	500	-500	-80	500	-500	500	mV	V _{CM} = 0
I _{CC}	Power Supply Current				28.7	50			mA	V _{CC} = 5.5 V, -Inputs = 0 V, +Inputs = 0.5 V
t _{PLH}	Turn-Off Time				30	50			ns	R _L = 3.9 kΩ, V _{CC} = 5.0 V, C _L = 30 pF, Fig. 1
t _{PHL}	Turn-On Time				30	50			ns	R _L = 390 Ω, V _{CC} = 5.0 V, C _L = 30 pF, Fig. 1

*V_{DIFF} is a differential input voltage referred from "+IN A" to "-IN A" and from "+IN B" to "-IN B".

**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

***See input-output transfer characteristic graphs on following pages.

9615C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS	
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.			MAX.
V _{OL}	Output LOW Voltage		0.45		0.25	0.45		0.45	V	V _{CC} = 4.75 V, V _{OUT} = ** I _{OL} = 15.0 mA, *V _{DIFF} = 0.5 V
V _{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		V	V _{CC} = 4.75 V, V _{OUT} = ** I _{OH} = -5.0 mA, *V _{DIFF} = -0.5 V
I _{CEX}	Output Leakage Current					100		200	μA	V _{CEX} = 5.25 V, *V _{DIFF} = V _{CC} = 4.75 V
I _{SC}	Output Shorted Current			-14		-100			mA	V _{CC} = 5.25 V, **V _{SC} = 0 V, *V _{DIFF} = -0.5 V
I _{IN}	Input Current		-0.9		-0.49	-0.7		-0.7	mA	V _{CC} = 5.25 V, V _{IN} = 0.45 V Other Input = 5.25 V
I _{IN(ST)}	Strobe Input Current				-1.15	-2.4			mA	V _{CC} = 5.25 V, V _{IN} = 0.45 V *V _{DIFF} = 0.5 V
I _{IN(R-C)}	Response Control Input Current			-1.2	-3.4				mA	V _{CC} = 5.25 V, *V _{DIFF} = 0.5 V
V _{CM}	Common Mode Voltage	-15	+15	-15	±17.5	+15	-15	+15	V	V _{CC} = 5.0 V, *V _{DIFF} = 1.0V
I _{R(ST)}	Strobe Input Leakage Current					5.0		10	μA	V _{CC} = 4.75 V, *V _{DIFF} = -0.5 V V _R = 4.5 V
R _{IN}	Input Resistor			74	130	179			Ω	V _{CC} = 5.0 V, V _{IN(R)} = 1.0 V, +Input = GND
V _{TH} ***	Differential Input Threshold Voltage	-500	500	-500	-80	500	-500	500	mV	V _{CM} = 0V
I _{CC}	Power Supply Current				28.7	50			mA	V _{CC} = 5.25 V, +Inputs = 0.5 V, -Inputs = 0 V
t _{PLH}	Turn-Off Time				30	75			ns	R _L = 3.9 kΩ, V _{CC} = 5.0 V, C _L = 30 pF, Fig. 1
t _{PHL}	Turn-On Time				30	75			ns	R _L = 390 Ω, V _{CC} = 5.0 V, C _L = 30 pF, Fig. 1

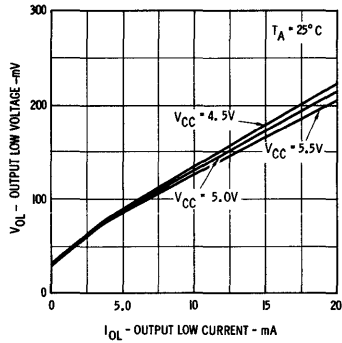
*V_{DIFF} is a differential input voltage referred from "+IN A" to "-IN A" and from "+IN B" to "-IN B".

**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

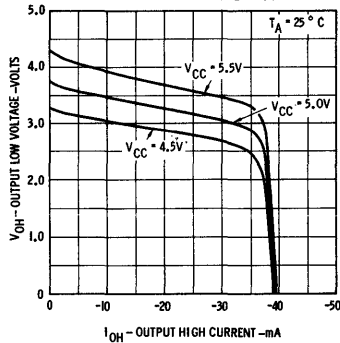
*** See input-output transfer characteristic graphs on following pages.

TYPICAL ELECTRICAL CHARACTERISTICS FOR 9615 AND 9615C

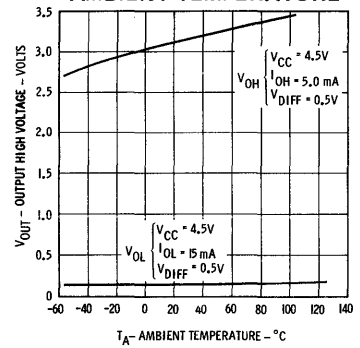
OUTPUT LOW VOLTAGE AS A FUNCTION OF OUTPUT LOW CURRENT



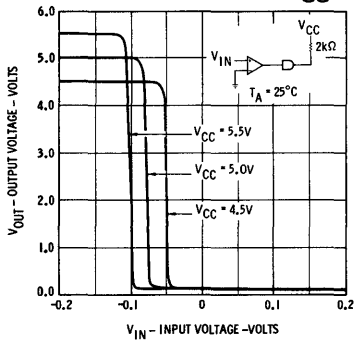
OUTPUT LOW VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



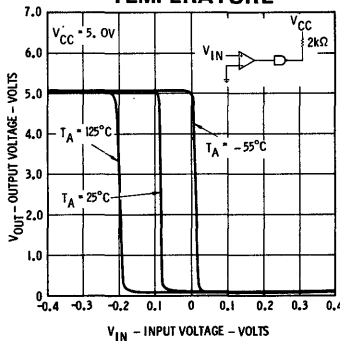
OUTPUT HIGH VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



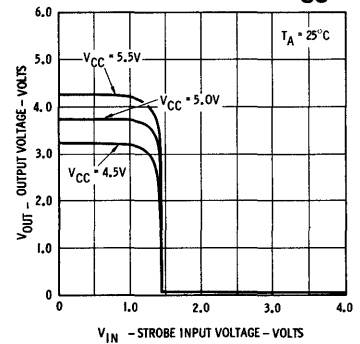
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF V_{CC}



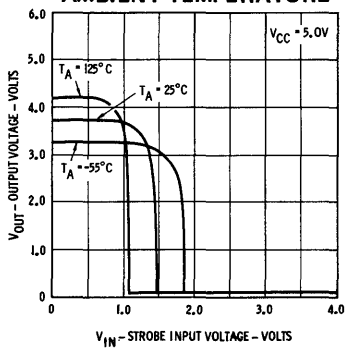
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF TEMPERATURE



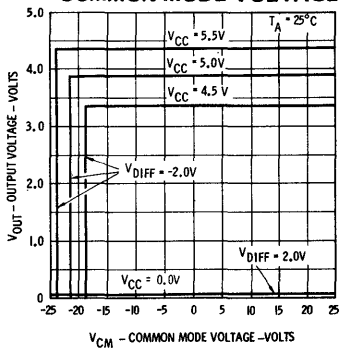
STROBE INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF V_{CC}



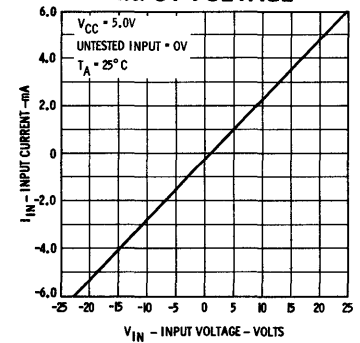
STROBE INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE



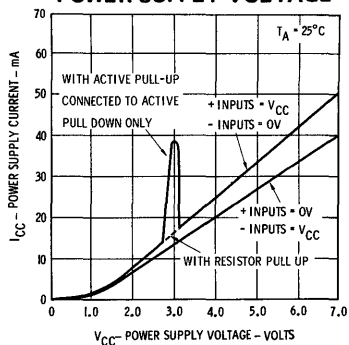
OUTPUT VOLTAGE AS A FUNCTION OF COMMON MODE VOLTAGE



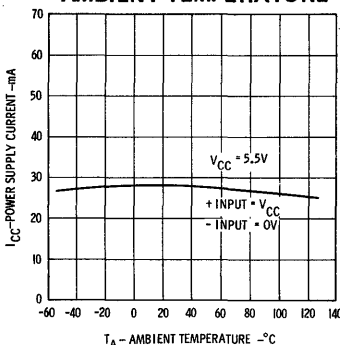
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



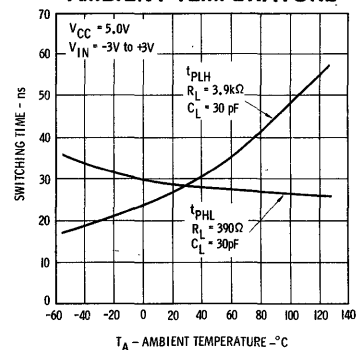
POWER SUPPLY CURRENT AS A FUNCTION OF POWER SUPPLY VOLTAGE



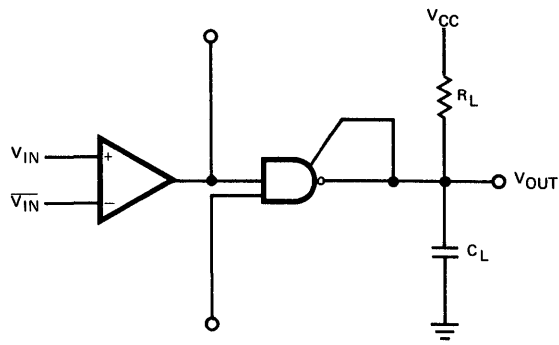
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

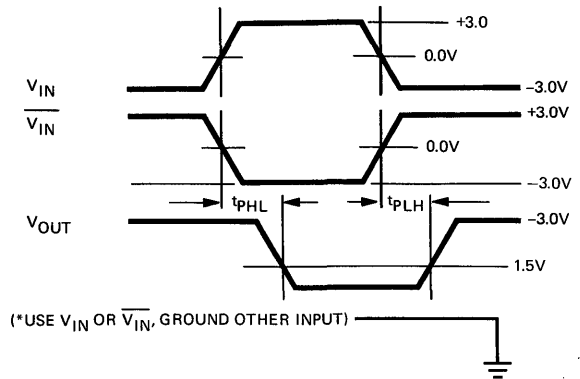
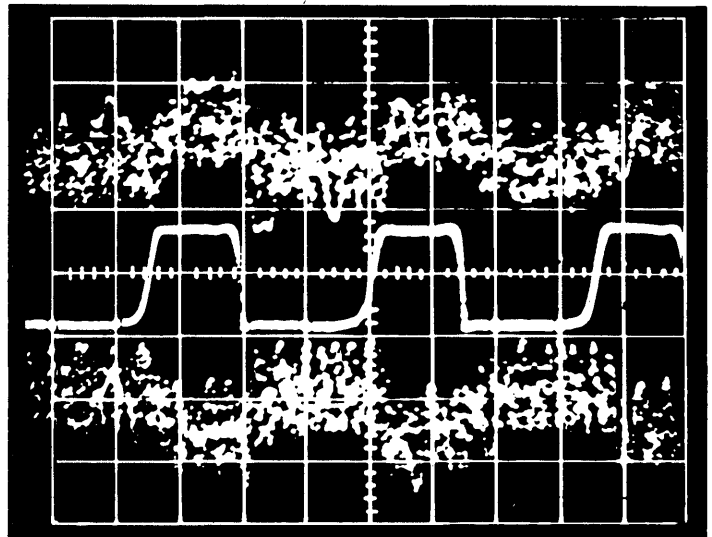
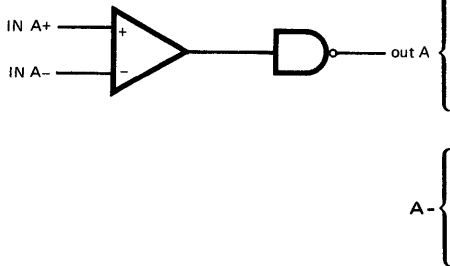


Fig. 1

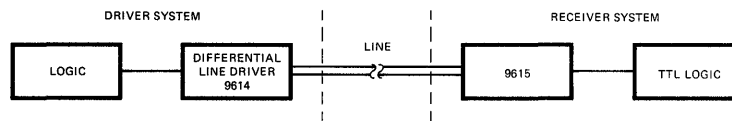
Photograph of a 9615 switching differential data in the presence of high common mode noise.



VERTICAL = 2.0 V DIV. HORIZONTAL = 50 ns/DIV.

Fig. 2

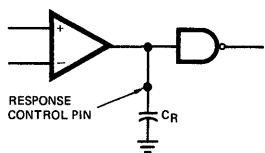
STANDARD USAGE



For example of operation see 9614 data sheet application section.

Fig. 3

FREQUENCY RESPONSE CONTROL



Note: $C_R > .01 \mu F$ may cause slowing of rise and fall times of the output.

FREQUENCY RESPONSE AS A FUNCTION OF CAPACITANCE

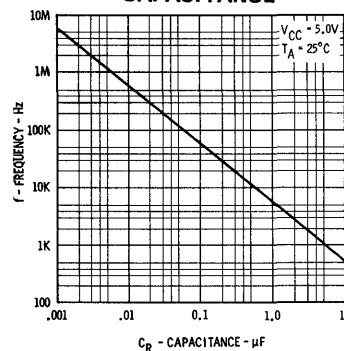


Fig. 4

9616

TRIPLE EIA RS-232-C/MIL-STD-188C LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9616 is a Triple Line Driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C (by the appropriate device selection). Each driver converts TTL/DTL logic levels to EIA/CCITT and/or MIL-STD-188C logic levels for transmission between data terminal equipment and data communications equipment. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH on the inhibit terminal interrupts signal transfer and forces the output to a $-V_{OUT}$ (EIA/CCITT MARK state).

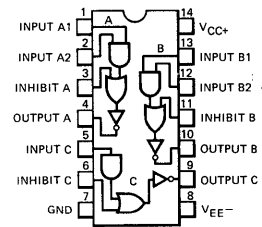
For the complementary function, see the 9617 Triple EIA RS-232-C Line Receiver and the 9627 Dual EIA RS-232-C and MIL-STD-188C Line Receiver.

- INTERNAL SLEW RATE LIMITING
- MEETS EIA RS-232-C AND CCITT V.24 AND/OR MIL-STD-188C
- LOGIC TRUE INHIBIT FUNCTION
- OUTPUT SHORT CIRCUIT CURRENT LIMITING
- OUTPUT VOLTAGE LEVELS INDEPENDENT OF SUPPLY VOLTAGES

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±15 V	
Input or Inhibit Voltage		-1.5 to +6.0 V	
Output Signal Voltage		±15 V	
Maximum Power Disipation (Note 1)		630 mW	
Storage Temperature Range		-65°C to +125°C	
Operating Temperature			
RS-232	Mil-Std-188	(9616)	-55°C to +125°C
RS-232		(9616C)	0°C to 75°C
RS-232	Mil-Std-188	(9616E)	0°C to 75°C
Lead Temperature (Soldering, 60 seconds)			300°C

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



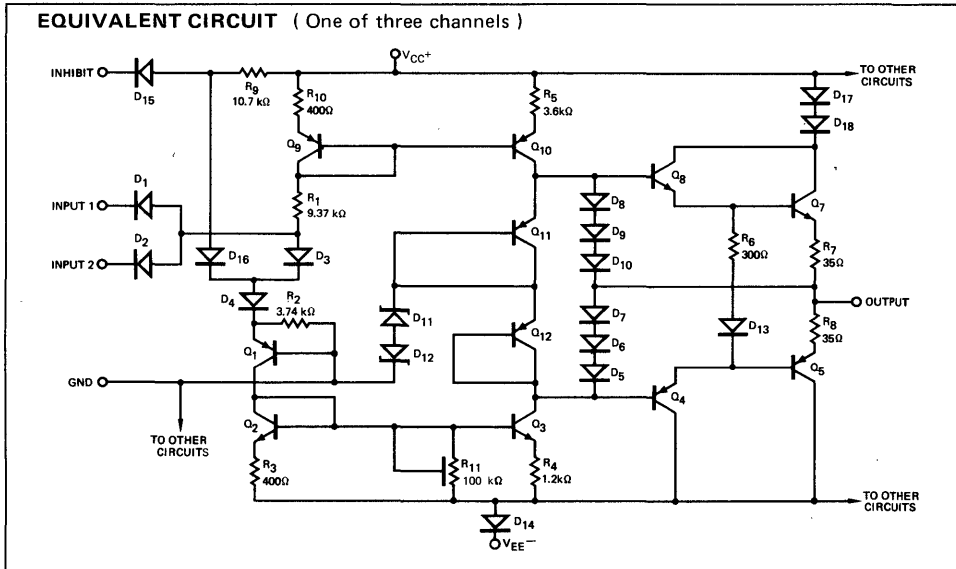
ORDER INFORMATION

TYPE	PART NO.
9616	9616 DM
9616C	9616 CDC
9616E	9616 EDC

TRUTH TABLE

INPUT	INHIBIT	OUTPUT
1	2	
All Sections:		
L	L	H
H	H	L
L	L	L
H	H	L
For Channels A & B add:		
L	H	H
H	L	H
L	H	L
H	L	L

(For Channel C, omit INPUT 2 Column)



*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 9616

9616 AND 9616E

RS232-C and MIL-STD-188C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 12V \pm 10\%$; $R_L \geq 3\text{ k}\Omega$, See Test Circuit, unless otherwise specified, Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	Output HIGH Voltage		5.0	6.0	7.0	V
V_{OL}	Output LOW Voltage		-7.0	-6.0	-5.0	V
	Ripple Rejection	Power Supply Ripple = 2.4Vp-p, f = 400 Hz		0.25		% of V_{OUT}
V_{OH} to V_{OL}	Output HIGH Voltage to Output LOW Voltage Magnitude Matching Error				± 10	%
R_{OUT}	Output Resistance, Power On	$R_L = 6\text{ k}\Omega$, $\Delta I_L = 10\text{ mA}$		75		Ω
I_{SC+}	Positive Output Short-Circuit Current			17	100	mA
I_{SC-}	Negative Output Short-Circuit Current			-17	-100	mA
V_{IH}	Input HIGH Voltage				2.0	V
V_{IL}	Input LOW Voltage		0.8			V
I_{IH}	Input HIGH Current	$V_{IN} = 2.4\text{ V}$			40	μA
		$V_{IN} = 5.5\text{ V}$			1.0	mA
I_{IL}	Input LOW Current	$V_{IN} = 0.4\text{ V}$	-1.6			mA
R_{OUT}	Output Resistance, Power Off	$-2.0\text{ V} \leq V_{OUT} \leq +2.0\text{ V}$ All Inputs and Supply Pins Grounded	300			Ω
I_+	Positive Supply Current	$T_A = +25^\circ\text{C}$ $V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8\text{ V}$		15		mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\text{ V}$		7.5		
I_-	Negative Supply Current	$T_A = +25^\circ\text{C}$ $V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8\text{ V}$		0		mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\text{ V}$		-15		

AC CHARACTERISTICS ($0 \leq T_A \leq 75^\circ\text{C}$, Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Positive Slew Rate	$0\text{ pF} \leq C_L \leq 2500\text{ pF}$ $R_L \geq 3\text{ k}\Omega$	4.0	15	30	V/ μs
	Negative Slew Rate	$0\text{ pF} \leq C_L \leq 2500\text{ pF}$ $R_L \geq 3\text{ k}\Omega$	30	-15	-4.0	V/ μs
t_{PLH}	Propagation Delay Time	No Load		320		ns
t_{PHL}	Propagation Delay Time	No Load		320		ns

- NOTES: 1. The operating temperature range for the 9616 is -55°C to $+125^\circ\text{C}$ and 9616E is 0°C to $+75^\circ\text{C}$.
 2. An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate. No external capacitor is needed to meet RS-232-C over the operating temperature range of 0°C to $+75^\circ\text{C}$.

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 9616

9616C

EIA RS232-C

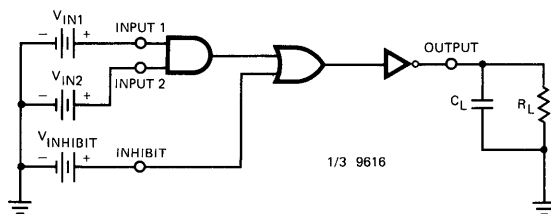
ELECTRICAL CHARACTERISTICS ($V_{CC+} = 12V$, $V_{EE-} = 12V \pm 10\%$, over operating temperature range, Test Circuit, $R_L = 3 k\Omega$, unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{OH}	Output HIGH Voltage	V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8V$	+5.0	+6.0	7.5	V
V_{OL}	Output LOW Voltage	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0 V$	7.5	-6.0	-5.0	V
I_{SC+}	Positive Output Short-Circuit Current	$R_L = 0\Omega$, V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8 V$		-17		mA
I_{SC-}	Negative Output Short-Circuit Current	$R_L = 0\Omega$, $V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0 V$		+17		mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	$V_{IN1} = V_{IN2} = 2.4 V$			40	μA
I_{IL}	Input LOW Current	$V_{IN1} = V_{IN2} = 0.4 V$	-1.6	-1.2		mA
	Inhibit HIGH Current	$V_{INHIBIT} = 2.4 V$			40	μA
	Inhibit LOW Current	$V_{INHIBIT} = 0.4 V$	-1.6	-1.2		mA
I_+	Total Positive Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8 V$		15		mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0 V$		7.5		mA
I_-	Total Negative Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8 V$		0		mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0 V$		-15		mA
R_{OUT}	Output Resistance, Power Off	$-2.0V \leq V_{OUT} \leq +2.0V$. All Inputs and Supplies Grounded.	300			Ω

AC CHARACTERISTICS

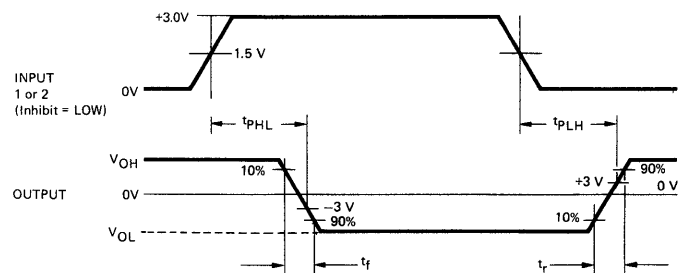
	Positive Slew Rate	$0 pF \leq C_L \leq 2500 pF$, $R_L \geq 3 k\Omega$	4.0	15	30	V/ μs
	Negative Slew Rate	$0 pF \leq C_L \leq 2500 pF$, $R_L \geq 3 k\Omega$	-30	-15	-4.0	V/ μs
t_{PLH}	Propagation Delay Time	No Load		320		ns
t_{PHL}	Propagation Delay Time	No Load		320		ns

SWITCHING TEST CIRCUIT



Note: Omit V_{IN2} for channel "C".

VOLTAGE WAVEFORMS



Pulse Generator Rise Time = 10 ± 5 ns

9617

TRIPLE EIA RS-232-C LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9617 is a monolithic Triple Line Receiver constructed using the Fairchild Planar* process. It is designed to meet the terminator electrical requirements of EIA RS-232-C and CCITT V.24. It receives line signals produced by the 9616, an EIA/CCITT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 k Ω and 7 k Ω and can withstand ± 25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground.

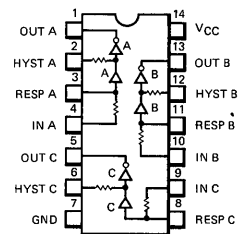
- MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS
- FAIL-SAFE OPERATION
- HYSTERESIS OR NON-HYSTERESIS MODE
- INDIVIDUAL RESPONSE CONTROLS
- TTL COMPATIBLE OUTPUT
- SINGLE +5 V SUPPLY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 V
Input Voltage	± 25 V
Output Current	25 mA
Maximum Power Dissipation (Note 1)	630 mW
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	0°C to $+75^{\circ}\text{C}$
Lead Temperature (Soldering, 60 seconds)	300°C

Note 1. Derate 8.3 mW/ $^{\circ}\text{C}$ above 70°C

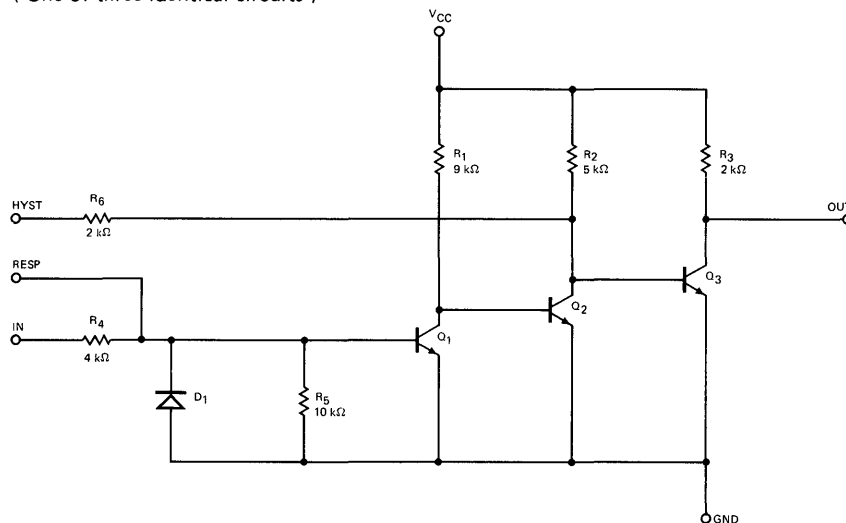
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
9617C	9617DC

EQUIVALENT CIRCUIT (One of three identical circuits)



*Planar is a patented Fairchild process.

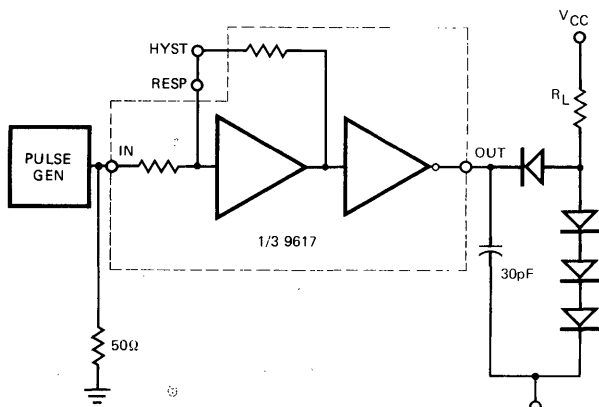
FAIRCHILD LINEAR INTEGRATED CIRCUIT • 9617

9617C

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0V, \pm 5\%, T_A = 25^\circ C$ Response Pin Open, unless otherwise specified)

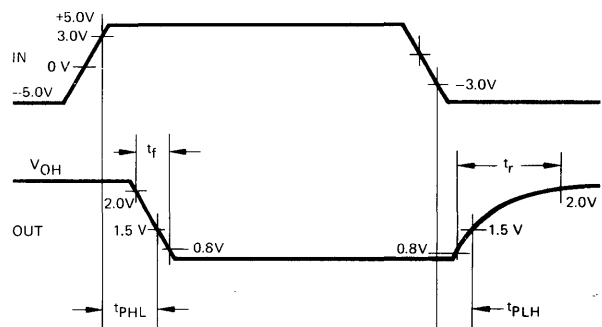
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Resistance	$V_I = \pm 25V$	3.0	4.0	7.0	$k\Omega$
Input Voltage	Open Circuit		0.2	2.0	V
Upper Input Threshold Voltage	RESP – HYST Connected	1.75	2.0	2.25	V
Lower Input Threshold Voltage	RESP – HYST Connected	0.75	0.85	1.25	V
Open Loop Threshold Voltage		0.4	1.0	1.2	V
Output HIGH Voltage	$V_{IN} = -3.0V, 0V$ or open circuit $V_{CC} = 4.5V, I_L = -200\mu A$	2.4	3.0		V
Output LOW Voltage	$V_{IN} = +3.0V$ $V_{CC} = 4.5V, I_L = 8.0mA$		0.3	0.4	V
Output Short-Circuit Current	$V_O = 0V$		2.5		mA
Supply Current	$V_{CC} = +5.5V, V_{IN} = 5.0V$		12		mA
Propagation Delay Time (t_{pLH})	$R_L = 3.9k\Omega$		60		ns
Risetime	$R_L = 3.9k\Omega$		150		ns
Propagation Delay Time (t_{pHL})	$R_L = 390\Omega$		40		ns
Fall Time	$R_L = 390\Omega$		50		ns

SWITCHING TEST CIRCUIT



All diodes FD100 or equivalent.

VOLTAGE WAVEFORMS



Input Pulse Characteristics:
 PRR = 1 MHz
 PW = 500 μs
 $t_r = t_f = 10 \pm 2ns$ (10% to 90%)

NOTE: Wiring capacitance should be minimized between outputs, hysteresis and response pins.

9620

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9620 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ± 500 mV of differential data in the presence of HIGH level (± 15 V) common mode voltages and deliver undisturbed TTL logic to the output. In addition to line reception the 9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including ECL, CTL, HLLDTL, RTL and TTL. HLLDTL output logic levels can be provided by tying the output to V_{CC2} (+12 V) through a resistor. The outputs can also be wired-OR. The 9620 offers the advantages of logic compatible voltages (+5 V, +12 V), TTL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components. See note 2.

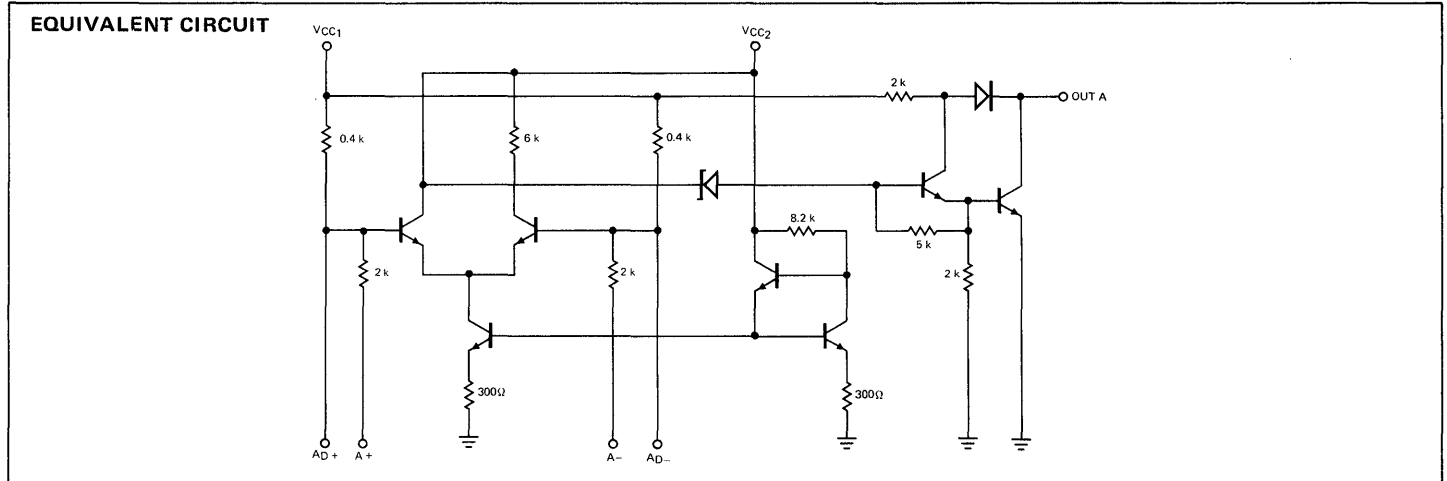
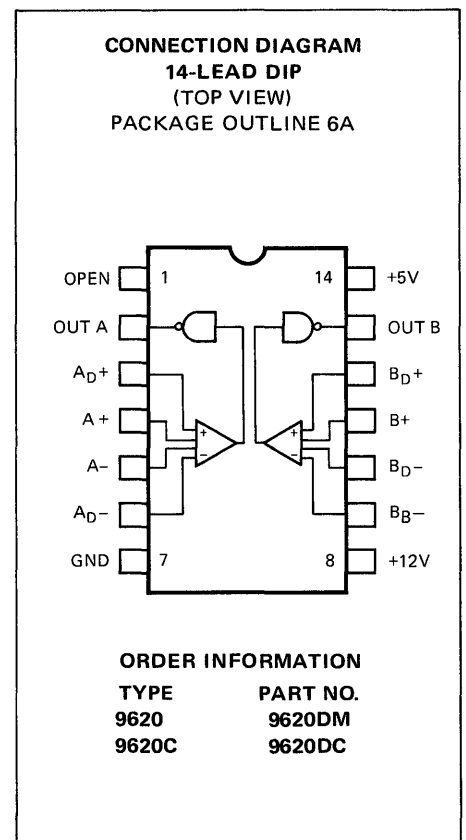
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **WIRED-OR CAPABILITY**
- **DIRECT INPUTS (A_D , B_D)**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature Range	
Military (9620)	-55°C to +125°C
Commercial (9620C)	-0°C to +75°C
V_{CC1} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	± 20 V
Voltage Applied to Outputs for HIGH Output State	-0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	670 mW

NOTE

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C.
2. The 9615 Dual Differential Line Receiver is recommended as a functional equivalent for the 9620 in new designs.



FAIRCHILD LINEAR INTEGRATED CIRCUITS • 9620

9620

ELECTRICAL CHARACTERISTICS ($V_{CC1} = 5.0\text{ V} \pm 10\%$, $V_{CC2} = 12.0\text{ V} \pm 10\%$) 9620

SYMBOL	PARAMETER	LIMITS						UNITS	CONDITIONS		
		-55°C		+25°C		+125°C					
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}	Output LOW Voltage	0.40		0.21 0.40		0.45		V	$V_{CC1} = 4.5\text{ V}$ $I_{OL} = 15.0\text{ mA}$	$V_{CC2} = 10.8\text{ V}$ $*V_{DIFF} = 0.5\text{ V}$	
V_{OH}	Output HIGH Voltage	2.8		3.0		2.9		V	$V_{CC1} = 4.5\text{ V}$ $I_{OH} = -0.2\text{ mA}$	$V_{CC2} = 10.8\text{ V}$ $*V_{DIFF} = -0.5\text{ V}$	
I_{CEX}	Output Leakage Current	50		100		200		μA	$V_{CEX} = 13.2\text{ V}$		
I_{SC}	Output Shorted Current			-1.4 -2.15 -3.1				mA	$V_{CC1} = 5.0\text{ V}$	$V_{CC2} = 12.0\text{ V}$	
I_F	Input Forward Current	-3.1		-2.1 -3.0		-3.0		mA	$V_{CC1} = 5.0\text{ V}$	$V_{CC2} = 12.0\text{ V}$ $V_{Input} = 0\text{ V}^{\dagger}$	
$\dagger V_{TH}$	Differential Input Threshold Voltage	500		120 500		500		mV	$V_{CC1} = 5.0\text{ V}$	$V_{CC2} = 12.0\text{ V}$	
$\dagger V_{CM}$	Common Mode Voltage	-15	15	-15	± 17.5	15	-15	15	V	$V_{CC1} = 5.0\text{ V}$ $*V_{DIFF} = 2.0\text{ V}$	$V_{CC2} = 12.0\text{ V}$
I_{VCC1}	5 V Supply Current	13		8.2 13		13		mA	$V_{CC1} = 5.5\text{ V}$ $V_{CC2} = 13.2\text{ V}$	+Input = 5.5 V -Input = 0 V	
I_{VCC2}	12 V Supply Current	8.0		5.6 8.0		8.0		mA	$V_{CC1} = 5.5\text{ V}$ $V_{CC2} = 13.2\text{ V}$	+Input = 5.5 V -Input = 0 V	
t_{PLH}	Turn-Off Time			35 50				ns	$R_L = 3.9\text{ k}\Omega$	$C_L = 3.0\text{ pF}$	
t_{PHL}	Turn-On Time			20 50				ns	$R_L = 390\ \Omega$	$C_L = 30\text{ pF}$	

\dagger All input voltages are referred to the attenuated inputs (A⁺, A⁻, B⁺, B⁻)
 $*V_{DIFF}$ is a differential input voltage referred from A⁺ to A⁻ and from B⁺ to B⁻.

9620C

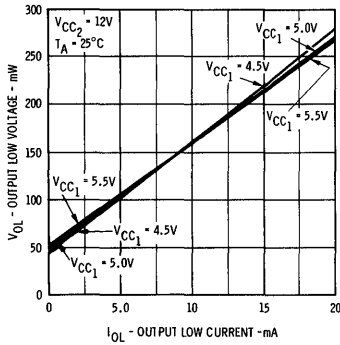
ELECTRICAL CHARACTERISTICS ($V_{CC1} = 5.0\text{ V} \pm 5\%$, $V_{CC2} = 12.0\text{ V} \pm 5\%$)

SYMBOL	PARAMETER	LIMITS						UNITS	CONDITIONS		
		0°C		+25°C		+75°C					
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}	Output LOW Voltage	0.45		0.25 0.45		0.50		V	$V_{CC1} = 4.75\text{ V}$ $I_{OL} = 15.0\text{ mA}$	$V_{CC2} = 11.4\text{ V}$ $*V_{DIFF} = 0.5\text{ V}$	
V_{OH}	Output HIGH Voltage	2.8		3.0 3.3		2.9		V	$V_{CC1} = 4.75\text{ V}$ $I_{OH} = -0.2\text{ mA}$	$V_{CC2} = 12.6\text{ V}$ $*V_{DIFF} = -0.5\text{ V}$	
I_{CEX}	Output Leakage Current	50		100		200		μA	$V_{CEX} = 5.25\text{ V}$		
I_{SC}	Output Shorted Current			-1.4 -2.15 -3.1				mA	$V_{CC1} = 5.0\text{ V}$	$V_{CC2} = 12.0\text{ V}$	
I_F	Input Forward Current	-3.1		-2.1 -3.0		-3.0		mA	$V_{CC1} = 5.0\text{ V}$	$V_{CC2} = 12.0\text{ V}$ $V_{Input} = 0\text{ V}^{\dagger}$	
$\dagger V_{TH}$	Differential Input Threshold Voltage	500		120 500		500		mV	$V_{CC1} = 4.75\text{ V}$	$V_{CC2} = 12.6\text{ V}$	
$\dagger V_{CM}$	Common Mode Voltage	-12	12	-12	± 17.5	12	-12	12	V	$V_{CC1} = 5.0\text{ V}$ $*V_{DIFF} = 2.0\text{ V}$	$V_{CC2} = 12.0\text{ V}$
I_{VCC1}	5 V Supply Current	13.5		8.2 13.5		13.5		mA	$V_{CC1} = 5.25\text{ V}$ $V_{CC2} = 12.6\text{ V}$	+Input = 5.25 V -Input = 0 V	
I_{VCC2}	12 V Supply Current	8.5		5.6 8.5		8.5		mA	$V_{CC1} = 5.25\text{ V}$ $V_{CC2} = 12.6\text{ V}$	+Input = 5.25 V -Input = 0 V	
t_{PLH}	Turn-Off Time			35 75				ns	$R_L = 3.9\text{ k}\Omega$	$C_L = 30\text{ pF}$	
t_{PHL}	Turn-On Time			20 75				ns	$R_L = 390\ \Omega$	$C_L = 30\text{ pF}$	

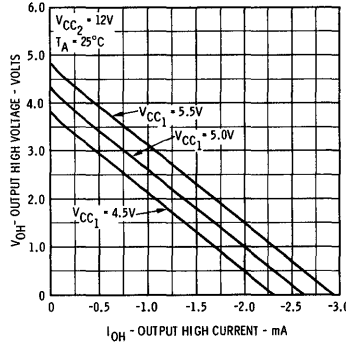
\dagger All input voltages are referred to the attenuated inputs (A⁺, A⁻, B⁺, B⁻)
 $*V_{DIFF}$ is a differential input voltage referred from A⁺ to A⁻ and from B⁺ to B⁻.

TYPICAL PERFORMANCE CURVES FOR 9620 AND 9620C

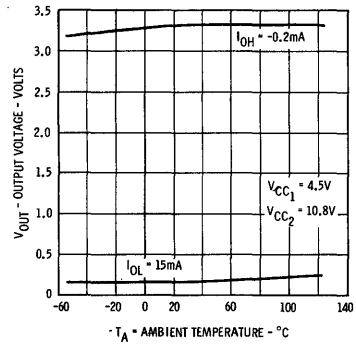
TYPICAL OUTPUT LOW VOLTAGE AS A FUNCTION OF OUTPUT LOW CURRENT



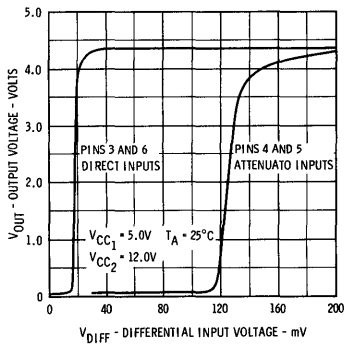
TYPICAL OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



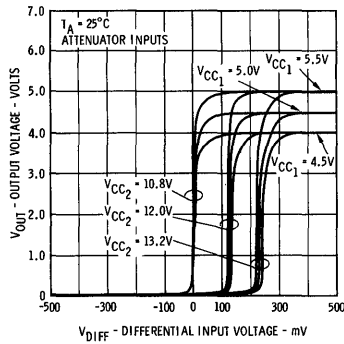
LOGIC LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



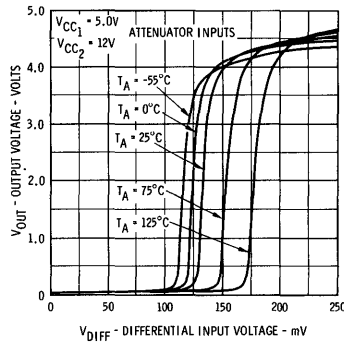
TYPICAL V_{OUT} AS A FUNCTION OF V_{DIFF} TRANSFER CHARACTERISTIC



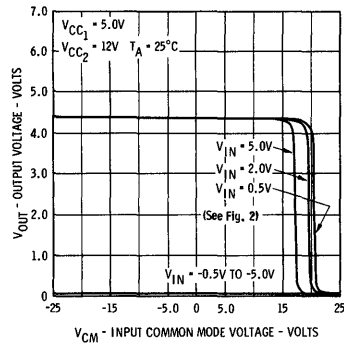
TYPICAL V_{OUT} AS A FUNCTION OF V_{DIFF} TRANSFER CHARACTERISTIC



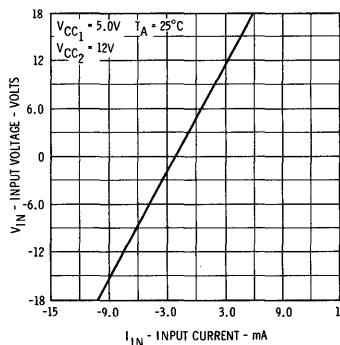
TYPICAL V_{OUT} AS A FUNCTION OF V_{DIFF} TRANSFER CHARACTERISTIC



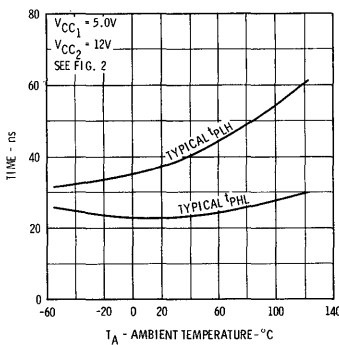
TYPICAL V_{OUT} AS A FUNCTION OF V_{CM} CHARACTERISTICS



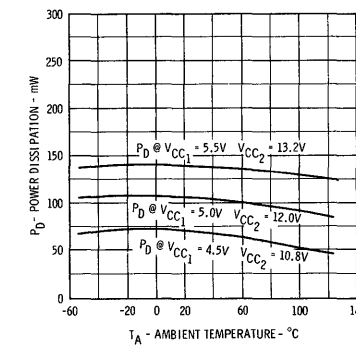
INPUT VOLTAGE AS A FUNCTION OF INPUT CURRENT



SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE



POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



STANDARD USAGE

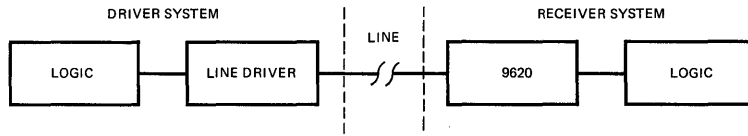
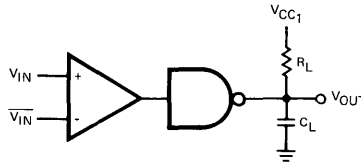
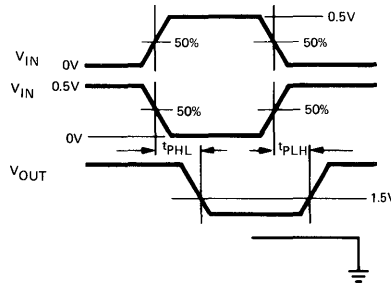


Fig. 1 SWITCHING TIME TEST CIRCUIT

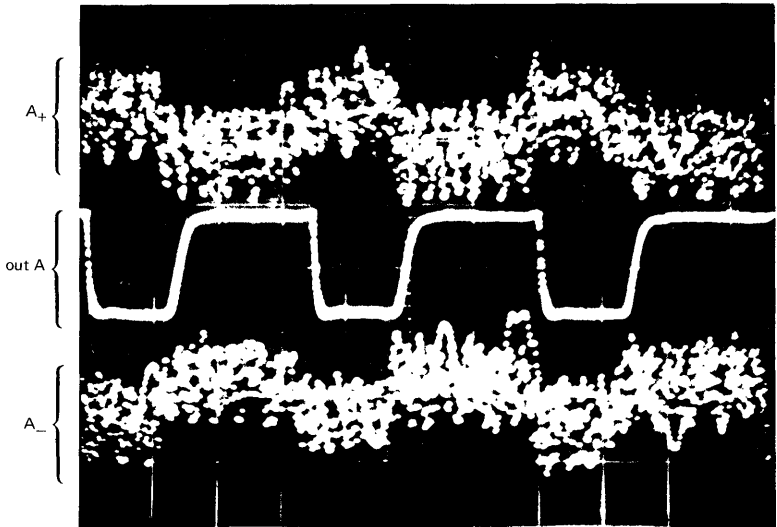
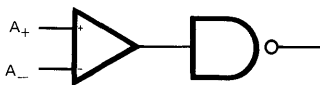


$V_{CC1} = 5.0 \text{ V}$
 $V_{CC2} = 12 \text{ V}$

WAVEFORMS



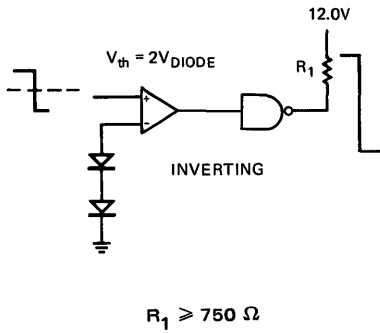
Photograph of a 9620 switching differential data in the presence of high common mode noise.



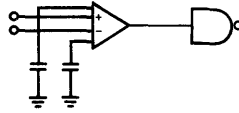
VERT = 2.0 V/div. HORIZ = 50 ns/div.

APPLICATIONS (Cont'd)

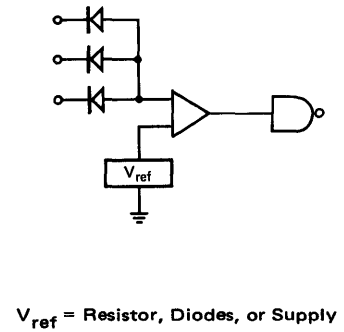
DIGITAL COMPARATOR WITH DIODE REFERENCE AND HIGH LEVEL LOGIC OUT



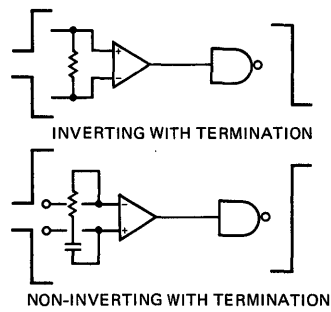
DIGITAL DIFFERENTIAL LINE RECEIVER WITH INPUTS ROLLED OFF



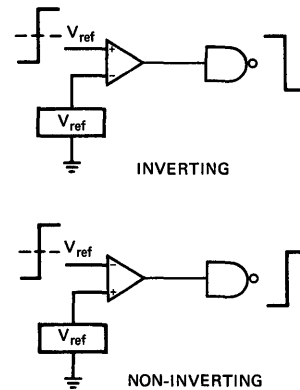
EXPANDED INTERFACE



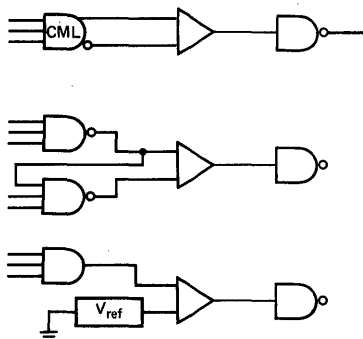
DIGITAL DIFFERENTIAL AMPLIFIER (Line Receiver)



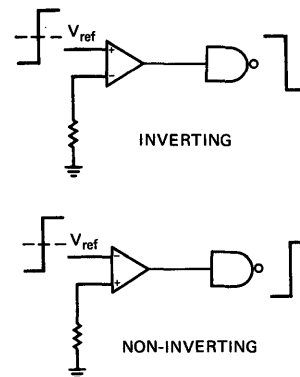
DIGITAL COMPARATOR



INTERFACING METHODS

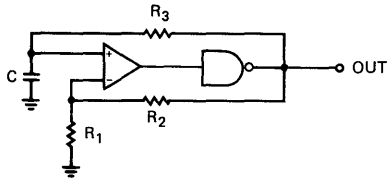


DIGITAL COMPARATOR WITH RESISTIVE DIVIDER AS REFERENCE



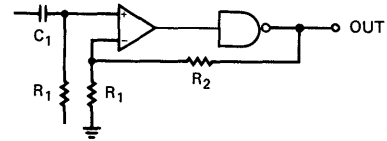
APPLICATIONS

MULTIVIBRATOR



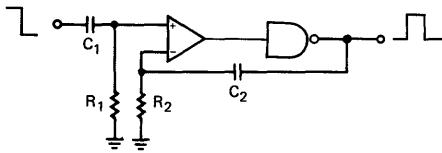
TYPICALLY
 $R_1 = 1.6 \text{ k}\Omega$, $R_2 = 2.7 \text{ k}\Omega$, $T = 1.3 R_3 C$

AC COUPLED DIGITAL AMPLIFIER WITH HYSTERESIS



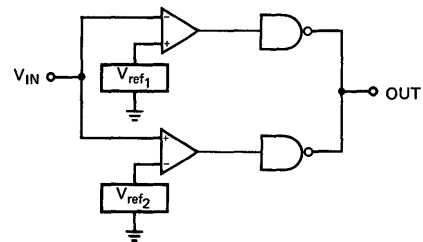
TYPICALLY
 $R_1 = 1.6 \text{ k}\Omega$, $R_2 = 2.7 \text{ k}\Omega$

MONOSTABLE MULTIVIBRATOR
 NEGATIVE EDGE TRIGGERING



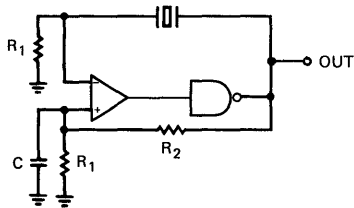
TYPICALLY
 $C_1 = 0.1 \mu\text{F}$, $R_1 = 1.2 \text{ k}\Omega$, $R_2 = 1.0 \text{ k}\Omega$
 Pulse Width = $50 \text{ ns} + 3.15 \times 10^3 C_2$

DOUBLE-ENDED COMPARATOR



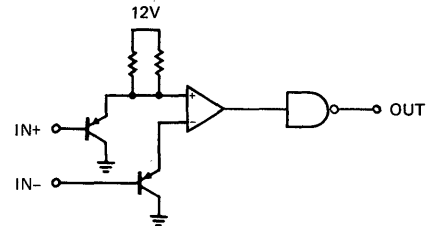
$$V_{OH} = V_{Ref_1} < V_{IN} < V_{Ref_2}$$

CRYSTAL CONTROLLED
 MULTIVIBRATOR



TYPICALLY
 $R_1 = 1.6 \text{ k}\Omega$, $R_2 = 2.7 \text{ k}\Omega$, $C = \frac{R_2}{1000}$

HIGH INPUT IMPEDANCE
 LINE RECEIVER
 (Positive Signals Only)



9621

DUAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130Ω twisted pair are provided. The output has the capability of driving high capacitance loads.

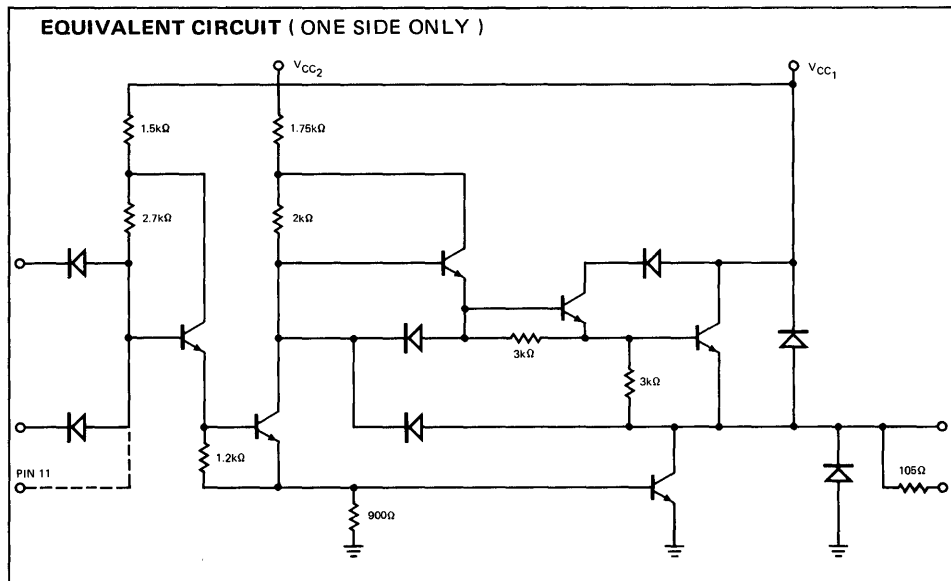
- TTL COMPATIBILITY
- TRANSMISSION LINE BACK-MATCHING
- OUTPUT CLAMP DIODES
- HIGH CAPACITANCE DRIVE
- HIGH OUTPUT VOLTAGE
- MILITARY TEMPERATURE RANGE

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65° C to +150° C
Operating Temperature Range	
Military (9621)	–55° C to +125° C
Commercial (9621C)	0° C to 75° C
V _{CC1} Pin Potential to Ground Pin	+3.8V to +8V
Input Voltage	–0.5V to +15V
Voltage Applied to Outputs	–2V to +V _{CC1} +1V
V _{CC2} Pin Potential to Ground Pin	V _{CC1} to +15V
Lead Temperature (Soldering, 60 seconds)	300° C
Internal Power Dissipation (Note 1)	
DIP	670mW

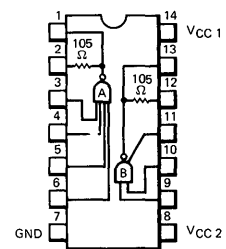
NOTE

1. Rating applies to ambient temperatures up to 70° C. Above 70° C derate linearly at 8.3mW/°C.



CONNECTION DIAGRAMS
14-LEAD DIP
(TOP VIEW)

PACKAGE OUTLINE 6A

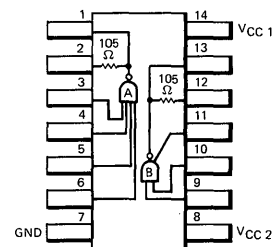


ORDER INFORMATION

TYPE	PART NO.
9621	9621DM
9621C	9621DC

14-LEAD FLATPAK
(TOP VIEW)

PACKAGE OUTLINE 3I



ORDER INFORMATION

TYPE	PART NO.
9621	9621FM

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 9621

9621

ELECTRICAL CHARACTERISTICS

SYMBOL	NOTES	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS	
			-55°C		+25°C		+125°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.			MAX.
V _{OL}		Output LOW Voltage		350		200	350		400	mV	I _{OL} = 20 mA V _{CC1} = 4.5 V V _{CC2} = 10.8 V
V _{OH}		Output HIGH Voltage	4.0		4.0	4.3		4.0		V	I _{OH} = -20 mA V _{CC1} = 4.5 V V _{CC2} = 10.8 V
I _{SC}	2	Output Short-Circuit Current			-180	-420				mA	V _{OUT} = 0 V V _{CC1} = 4.5 V V _{CC2} = 10.8 V
I _{OL}	2	Output LOW Current			150	200				mA	V _{OUT} = 5.0 V V _{CC1} = 4.5 V V _{CC2} = 10.8 V
I _F		Input Forward Current		-1.8		-1.15	-1.8		-1.8	mA	V _F = 0 V V _{CC1} = 5.5 V V _{CC2} = 13.2 V
I _R		Input Reverse Current		2.0		<1.0	2.0		5.0	μA	V _R = 5.5 V V _{CC1} = 5.5 V V _{CC2} = 13.2 V
V _{OLR}	3	Resistive Output LOW Voltage				380	500			mV	I _{OL} = 2.8 mA V _{CC1} = 5.0 V V _{CC2} = 12.0 V
V _{OHR}	3	Resistive Output HIGH Voltage			4.0	4.2				V	I _{OH} = -2.3 mA V _{CC1} = 5.0 V V _{CC2} = 12.0 V
V _{OLC}	4	Clamped Output LOW Voltage				-1.0	-2.0			V	I _{OL} = -20 mA V _{CC1} = 5.0 V V _{CC2} = 12.0 V
V _{OHc}	4	Clamped Output HIGH Voltage				6.0	7.0			V	I _{OH} = 20 mA V _{CC1} = 5.0 V V _{CC2} = 12.0 V
I _{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open V _{CC1} = 5.5 V V _{CC2} = 13.2 V
I _{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA	
t _{PLH}	5	Turn-Off Time				30	150			ns	C _L = 5000 pF V _{CC1} = 5.0 V V _{CC2} = 12.0 V
t _{PHL}	5	Turn-On Time				80	150			ns	
t _{PLH}		Turn-Off Time				13	25			ns	
t _{PHL}		Turn-On Time				9	25			ns	C _L = 30 pF V _{CC1} = 5.0 V V _{CC2} = 12.0 V
V _{IL}		Input LOW Voltage		1.3		1.5	1.0		0.7	V	V _{CC1} = 5.5 V, V _{CC2} = 10.8 V
V _{IH}		Input HIGH Voltage	2.2		2.0	1.7		1.8		V	V _{CC1} = 4.5 V, V _{CC2} = 13.2 V

NOTES:

2. Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
3. Test output resistance including 105Ω output resistor.
4. Tests output clamp diodes.
5. With both sides loaded at T_A = +125°C, maximum frequency = 500 kHz for Dual In-line package (θ_{JA} = 95°C/W) or 300 kHz for Flatpak (θ_{JA} = 165°C/W).
6. Maximum frequency = 500 kHz with both sides loaded at T_A = +75°C.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 9621

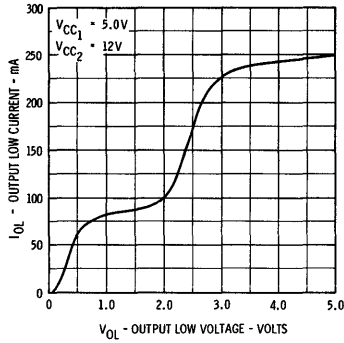
9621C

ELECTRICAL CHARACTERISTICS

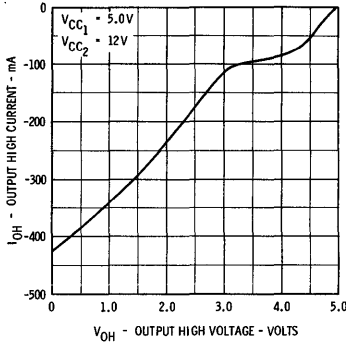
SYMBOL	NOTES	CHARACTERISTIC	LIMITS									
			0° C		+25° C			+75° C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.				MAX.
V _{OL}		Output LOW Voltage		400		200	400		450	mV	I _{OL} = 20 mA V _{CC1} = 4.75 V V _{CC2} = 11.4 V	
V _{OH}		Output HIGH Voltage	4.2		4.2	4.4		4.2		V	I _{OH} = -20 mA V _{CC1} = 4.75 V V _{CC2} = 11.4 V	
I _{SC}	2	Output Short-Circuit Current			-100	-420				mA	V _{OUT} = 0 V V _{CC1} = 4.75 V V _{CC2} = 11.4 V	
I _{OL}	2	Output LOW Current			75	200				mA	V _{OUT} = 5.0 V V _{CC1} = 4.75 V V _{CC2} = 11.4 V	
I _F		Input Forward Current		1.8		1.15	1.8		1.8	mA	V _F = 0 V V _{CC1} = 5.25 V V _{CC2} = 12.6 V	
I _R		Input Reverse Current		5.0		<1.0	5.0		10.0	μA	V _R = 5.5 V V _{CC1} = 5.25 V V _{CC2} = 12.6 V	
V _{OLR}	3	Resistive Output LOW Voltage				380	500			mV	I _{OL} = 2.8 mA V _{CC1} = 5.0 V V _{CC2} = 12.0 V	
V _{OHR}	3	Resistive Output HIGH Voltage			4.0	4.2				V	I _{OH} = -2.3 mA V _{CC1} = 5.0 V V _{CC2} = 12.0 V	
V _{OLC}	4	Clamped Output LOW Voltage				-1.0	-2.0			V	I _{OL} = -20 mA V _{CC1} = 5.0 V V _{CC2} = 12.0 V	
V _{OHC}	4	Clamped Output HIGH Voltage				6.0	7.0			V	I _{OH} = 20 mA V _{CC1} = 5.0 V V _{CC2} = 12.0 V	
I _{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open V _{CC1} = 5.25 V V _{CC2} = 12.6 V	
I _{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t _{PLH}	6	Turn-Off Time				30	200			ns	C _L = 5000 pF V _{CC1} = 5.0 V V _{CC2} = 12.0 V	
t _{PHL}	6	Turn-On Time				80	200			ns		
t _{PLH}		Turn-Off Time				13	40			ns	C _L = 30 pF V _{CC1} = 5.0 V V _{CC2} = 12.0 V	
t _{PHL}		Turn-On Time				9	40			ns		
V _{IL}		Input LOW Voltage		1.3		1.5	1.0		-0.7	V	V _{CC1} = 5.25 V, V _{CC2} = 12.6 V	
V _{IH}		Input HIGH Voltage	2.2		2.0	1.7		1.8		V	V _{CC1} = 4.75 V, V _{CC2} = 11.4 V	

TYPICAL ELECTRICAL CHARACTERISTICS FOR 9621 AND 9621C

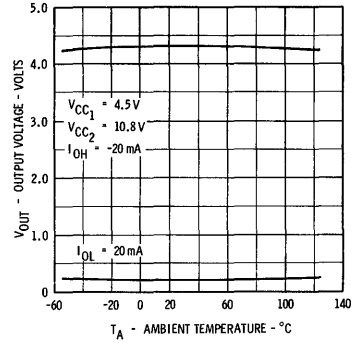
OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



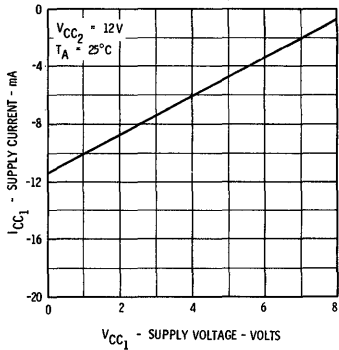
OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



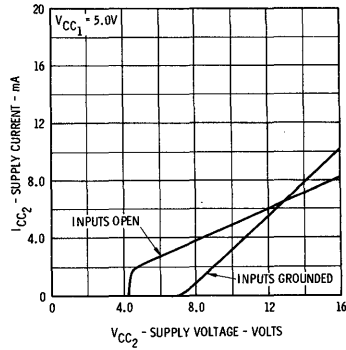
LOGIC LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



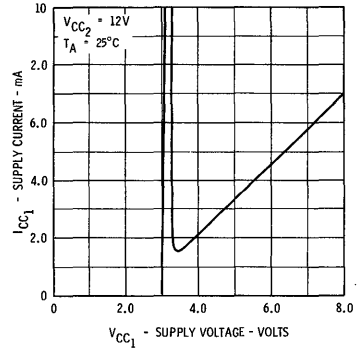
SUPPLY CURRENT AS A FUNCTION OF INPUTS GROUNDED



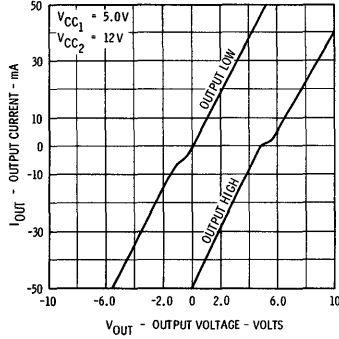
SUPPLY CURRENT AS A FUNCTION OF INPUTS OPEN



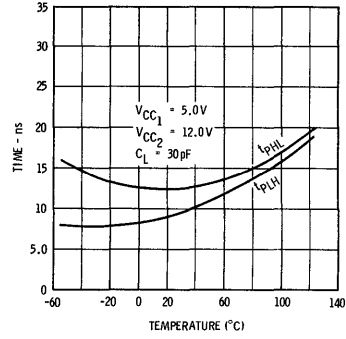
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



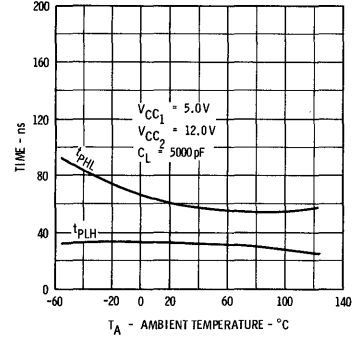
TYPICAL OUTPUT IMPEDANCE WITH BACK MATCHING RESISTORS



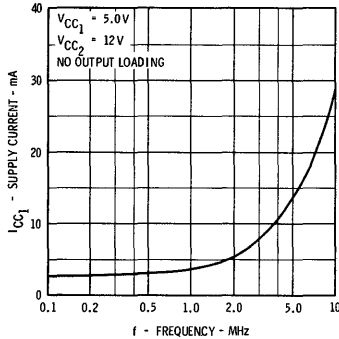
SWITCHING TIME AS A FUNCTION OF TEMPERATURE



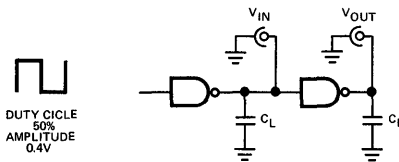
SWITCHING TIME AS A FUNCTION OF TEMPERATURE



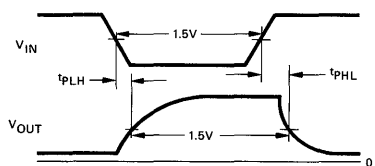
SUPPLY CURRENT AS A FUNCTION OF FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



DESCRIPTION OF REFLECTION DIAGRAM USAGE

The reflections on any line may be found by using the following procedure:

1. Draw the driver output characteristics for both the HIGH state and the LOW state on an I-V graph in the same manner as the reflection diagram.
2. Draw the receiver input characteristic on the same graph. The two points of intersection of the receiver and driver characteristics are the two dc operating points.
3. Choose to analyze either the reflections for the output going LOW or HIGH. In the example chosen the negative transition is analyzed.
4. Draw a line with a slope equal to the impedance of the line to be used, ($Z_0 = 100 \Omega$ in the example), from the HIGH state operating point (labeled A on our graph) to the LOW state output device characteristic (B_1). B_1 equals the conditions at the driver output immediately after turn-on.
5. Reverse the slope of Z_0 and sketch it from B_1 to the receiver input characteristic (C_1). C_1 equals the conditions at the receiver when the wavefront B_1 first reaches it.
6. By continuing this procedure of reversing the slope of Z_0 at each node all the reflections ($B_1, C_1, B_2, C_2, B_3, C_3 \dots B_N, C_N$), where B_X is the voltage at the driver and C_X is the voltage at the receiver, can be found.

The same procedure is used to check the reflections when switching the output HIGH.

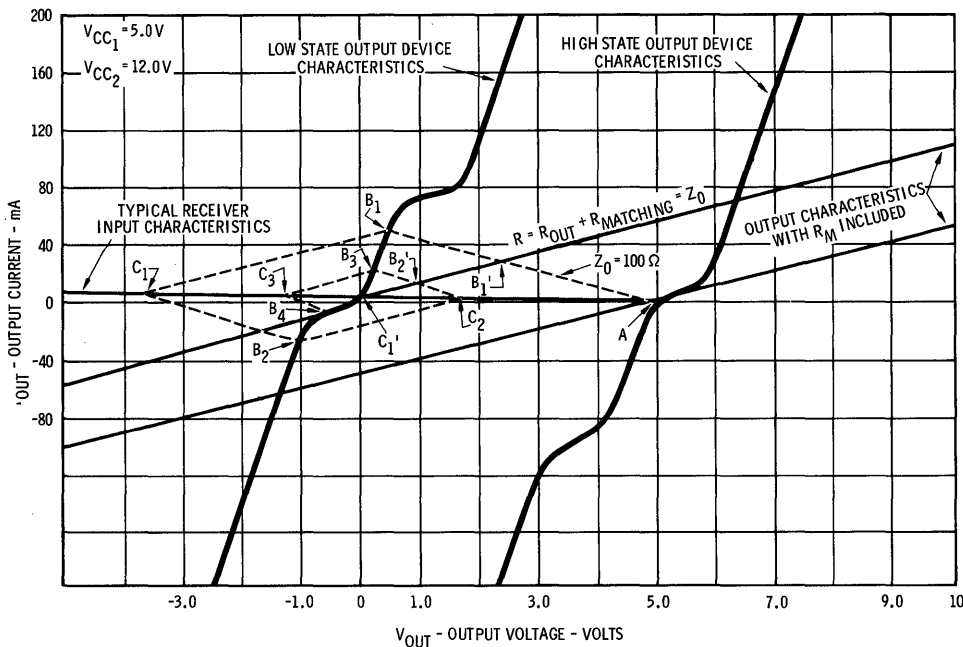
BACK-MATCHING, also referred to as reverse termination, offers several advantages to the user. It reduces the system power by not requiring the high current for resistive termination and it reduces the dc line losses because IR drops in the line become minimum.

To back-match any line (output switching low):

1. Measure the output resistance, R_{out} , from the LOW state operating point to B.
2. Subtract R_{out} from Z . ($R_{out} + R_M = Z_0$). This value R_M , is the required back-matching resistance.
3. Place R_M in series with the output of driver.
4. The reflections that occur on the line with R_M inserted can be treated in the same manner as the general case. The results are B_1 , and C_1 , and the receiver will not see any reflections.

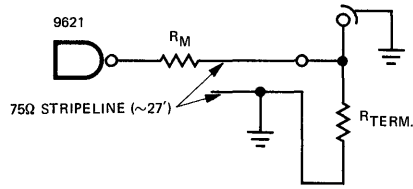
When switching the line differentially $R_M + R_{out} = Z_0/2$. The matched output characteristics of the 9621 make it possible to back-match effectively and require analysis of switching only one state.

TYPICAL REFLECTION DIAGRAM*



* GRAPHICAL ANALYSIS
First Presented by John B. James of I.C.T. (Eng.) LTD.

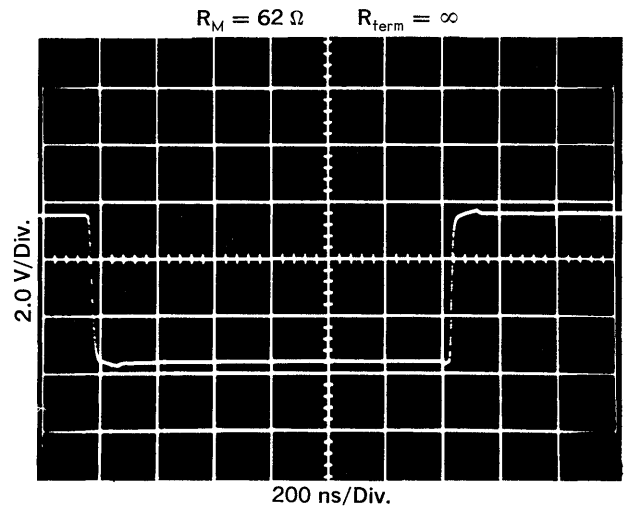
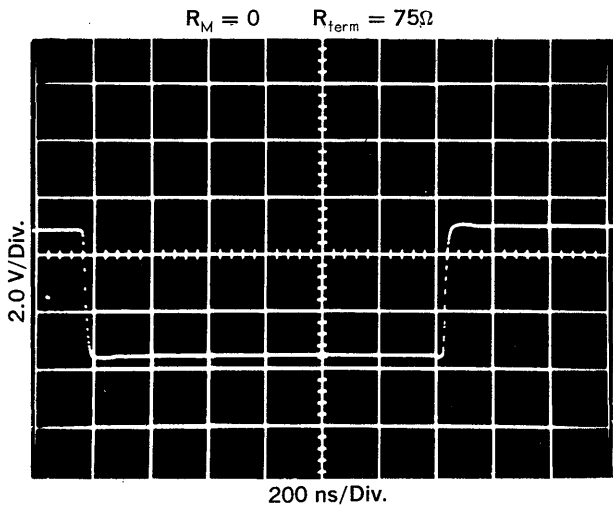
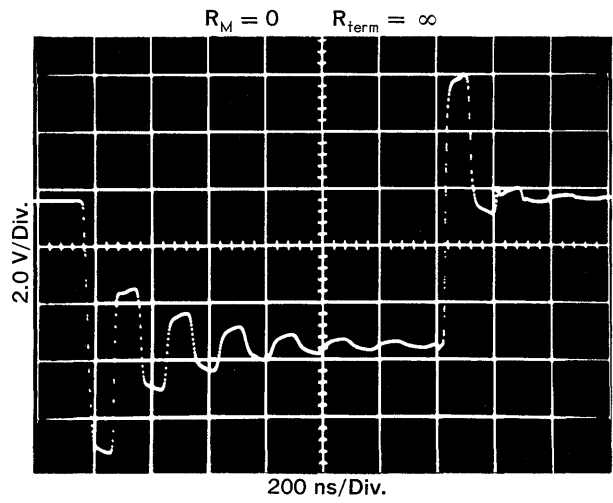
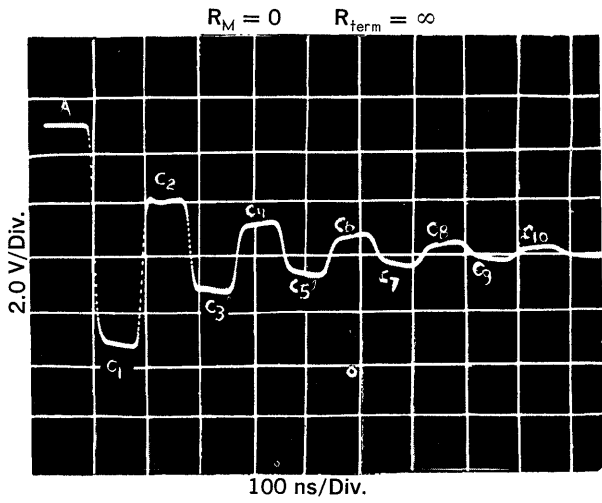
REFLECTION TEST CIRCUIT



BACK MATCHING TABLE

Z_0	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

The reflections are two delay's of the line wide. R_{term} is the total impedance seen at the receiving end.



9622

DUAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

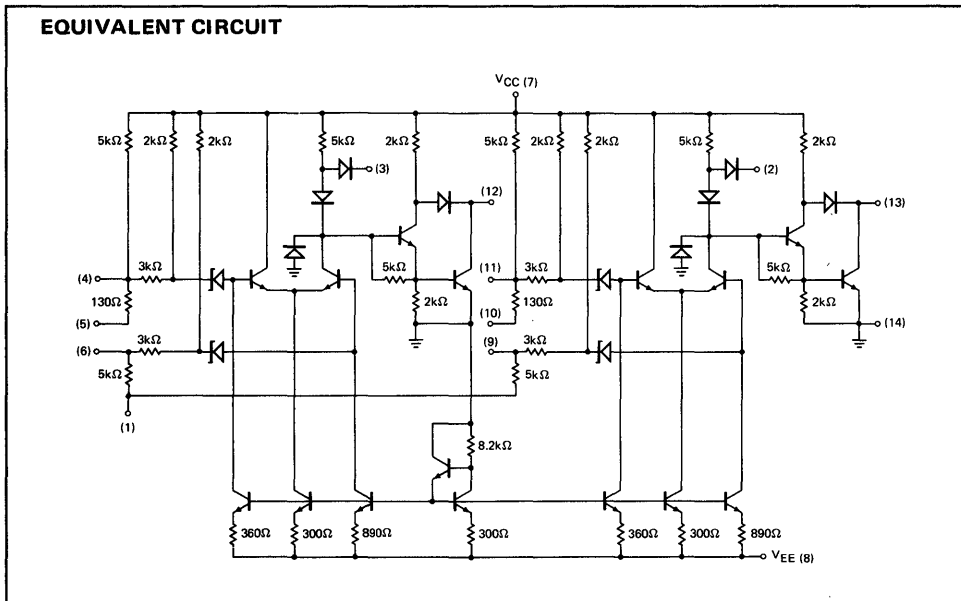
GENERAL DESCRIPTION — The 9622 is a Dual Line Receiver designed to discriminate a worst case logic swing of 2.0V from a $\pm 10V$ common mode noise signal or ground shift. A 1.5V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only $\pm 5\%$ (75 mV) over the military and industrial temperature ranges.

The 9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S_3 (Note 1). A 130Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output HIGH level can be increased to +12V by tying it to a positive supply through a resistor. The output circuits allow wired-OR operation.

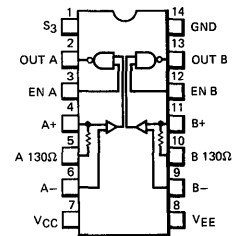
- TTL COMPATIBLE THRESHOLD VOLTAGE
- INPUT TERMINATING RESISTORS
- CHOICE OF OUTPUT STATE WITH INPUTS OPEN
- TTL COMPATIBLE OUTPUT
- HIGH COMMON MODE
- WIRE-OR CAPABILITY
- ENABLE INPUTS
- FULL MILITARY TEMPERATURE RANGE
- LOGIC COMPATIBLE SUPPLY VOLTAGES

NOTE

1. S_3 connected to V_{CC} —open inputs causes output to be HIGH.
 S_3 connected to Ground—open inputs causes output to be LOW.

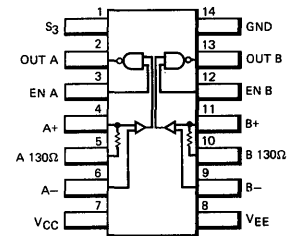


CONNECTION DIAGRAM
14-LEAD DIP
 (TOP VIEW)
 PACKAGE OUTLINE 6A



ORDER INFORMATION	
TYPE	PART NO.
9622	9622DM
9622C	9622DC

14-LEAD FLATPAK
 (TOP VIEW)
 PACKAGE OUTLINE 3I



ORDER INFORMATION	
TYPE	PART NO.
9622	9622FM

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 9622

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Operating Temperature	
Military (9622)	-55°C to +125°C
Commercial (9622C)	0°C to +75°C
Internal Power Dissipation (Note 2)	
DIP	670 mW
Flatpak	570 mW
V _{CC} Pin Potential to Ground Pin	-0.5V to +7V
Input Voltage	±15V
Voltage Applied to Outputs for Output HIGH State	-0.5V to +13.2V
V _{EE} Pin Potential to Ground Pin	-0.5V to -12V
Enable Pin Potential to Ground Pin	-0.5V to +15V
Lead Temperature (Soldering, 60 seconds)	300°C

NOTE

2. Rating applies to ambient temperature up to 70°C. Above 70°C derate linearly at 8.3mW/°C for the DIP and 7.1mW/°C for the Flatpak.

9622

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS	
		-55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.			MAX.
V _{OL}	Output LOW Voltage		0.40		0.17	0.40		0.40	Volts	V _{CC} = 4.5 V V _{EE} = -11 V *V _{DIFF} = 2.0 V I _{OL} = 12.4 mA
V _{OH}	Output HIGH Voltage	2.8		3.0	3.3		2.9		Volts	V _{CC} = 4.5 V V _{EE} = -9.0 V *V _{DIFF} = 1.0 V I _{OH} = -0.2 mA
I _{CEX}	Output Leakage Current		50			100		200	μA	V _{CC} = 4.5 V V _{EE} = -11 V *V _{DIFF} = 1.0 V V _{CEX} = 12 V
I _{SC}	Output Shorted Current	-1.3	-3.1	-1.4	-2.15	-3.1	-1.3	-3.1	mA	V _{CC} = 5.0 V V _{EE} = -10 V *V _{DIFF} = 1.0 V V _{SC} = 0 V
I _R (ENABLE)	Enable Input Leakage Current					2.0		5.0	μA	V _{CC} = 4.5 V V _{EE} = -11 V S ₃ = 4.5 V V _R = 4.0 V
I _F (ENABLE)	Enable Input Forward Current		-1.5		-0.96	-1.5		-1.5	mA	V _{CC} = 5.5 V V _{EE} = -9.0 V S ₃ = 0 V V _F = 0 V
I _F (+Input)	+Input Forward Current		-2.3		-1.67	-2.1		-2.0	mA	V _{CC} = 5.0 V V _{EE} = -10 V -Input = GND V _F = 0 V
I _F (-Input)	-Input Forward Current		-2.6		-1.87	-2.4		-2.3	mA	V _{CC} , S ₃ = 5.0 V V _{EE} = -10 V +Input = GND V _F = 0 V
V _{IL} (ENABLE)	Input LOW Voltage		1.3		1.4	1.0		0.7	Volts	V _{CC} = 5.0 V ±10% V _{EE} = -10 V ±10%
V _{TH}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	Volts	V _{CC} = 5.0 V ±10% V _{EE} = -10 V ±10%
V _{CM}	Common Mode Voltage			-10	±12	+10			Volts	V _{CC} = 5.0 V V _{EE} = -10 V *V _{DIFF} = 1.0 V or 2.0 V
R _{130Ω}	Terminating Resistance			100	130	175			Ω	
I _{CC}	5 V Supply Current				13.7	22.9			mA	V _{CC} = 5.5 V V _{EE} = -11 V S ₃ , +Inputs = 5.5 V, -Inputs = 0 V
I _{EE}	-10 V Supply Current				-6.5	-11.1			mA	V _{CC} = 5.5 V V _{EE} = -11 V S ₃ , +Inputs = 5.5 V, -Inputs = 0 V
t _{PLH}	Turn-Off Time				38	50			ns	V _{CC} = 5.0 V V _{EE} = -10 V V _{IN} 0→3 V, R _L = 3.9 kΩ, C _L = 30 pF
t _{PHL}	Turn-On Time				35	50			ns	V _{CC} = 5.0 V V _{EE} = -10 V V _{IN} 0→3.0 V, R _L = 0.39 kΩ, C _L = 30 pF

*V_{DIFF} is a differential input voltage referred from A+ to A- and from B+ to B-.

6

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 9622

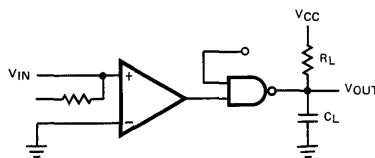
9622C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$)

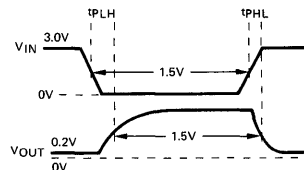
SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS	
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		0.45		0.17	0.45		0.45	Volts	$V_{CC} = 4.75 \text{ V}$ $*V_{DIFF} = 2.0 \text{ V}$ $V_{EE} = -10.5 \text{ V}$ $I_{OL} = 14.1 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.9		3.0	3.3		2.9		Volts	$V_{CC} = 4.75 \text{ V}$ $*V_{DIFF} = 1.0 \text{ V}$ $V_{EE} = -9.5 \text{ V}$ $I_{OH} = -0.2 \text{ mA}$
I_{CEX}	Output Leakage Current		80			100		200	μA	$V_{CC} = 4.75 \text{ V}$ $*V_{DIFF} = 1.0 \text{ V}$ $V_{EE} = -10.5 \text{ V}$ $V_{CEX} = 5.25 \text{ V}$
I_{SC}	Output Shorted Current	-1.3	-3.1	-1.4	-2.15	-3.2	-1.3	-3.1	mA	$V_{CC} = 5.0 \text{ V}$ $*V_{DIFF} = 1.0 \text{ V}$ $V_{EE} = -10 \text{ V}$ $V_{SC} = 0 \text{ V}$
I_R (ENABLE)	Enable Input Leakage Current					5		10	μA	$V_{CC} = 4.75 \text{ V}$ $S_3 = 4.75 \text{ V}$ $V_{EE} = -10.5 \text{ V}$ $V_R = 4.0 \text{ V}$
I_F (ENABLE)	Enable Input Forward Current		-1.5		-0.96	-1.5		-1.5	mA	$V_{CC} = 5.25 \text{ V}$ $S_3 = 0 \text{ V}$ $V_{EE} = -9.5 \text{ V}$ $V_F = 0 \text{ V}$
I_F (+Input)	+Input Forward Current		-2.6		-1.67	-2.4		-2.3	mA	$V_{CC} = 5.0 \text{ V}$ $V_{EE} = -10 \text{ V}$ -Input = GND $V_F = 0 \text{ V}$
I_F (-Input)	-Input Forward Current		-2.9		-1.87	-2.7		-2.6	mA	$V_{CC}, S_3 = 5.0 \text{ V}$ $V_{EE} = -10 \text{ V}$ +Input = GND $V_F = 0 \text{ V}$
V_{IL} (ENABLE)	Input LOW Voltage		1.2		1.4	1.0		0.85	Volts	$V_{CC} = 5.0 \text{ V} \pm 5\%$ $V_{EE} = -10 \text{ V} \pm 5\%$
V_{TH}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	Volts	$V_{CC} = 5.0 \text{ V} \pm 5\%$ $V_{EE} = -10 \text{ V} \pm 5\%$
V_{CM}	Common Mode Voltage			-7.5	± 12	+7.5			Volts	$V_{CC} = 5.0 \text{ V}$ $V_{EE} = -10 \text{ V}$ $*V_{DIFF} = 1.0 \text{ V}$ or 2.0 V
$R_{130\Omega}$	Terminating Resistance			91	130	185			Ω	
I_{CC}	5 V Supply Current				13.7	22.9			mA	$V_{CC} = 5.25 \text{ V}$ $S_3, +\text{Inputs} = 5.25 \text{ V}, -\text{Inputs} = 0 \text{ V}$
I_{EE}	-10 V Supply Current				-6.5	-11.1			mA	$V_{CC} = 5.25 \text{ V}$ $S_3, +\text{Inputs} = 5.25 \text{ V}, -\text{Inputs} = 0 \text{ V}$
t_{PLH}	Turn-Off Time				38	100			ns	$V_{CC} = 5.0 \text{ V}$ $V_{EE} = -10 \text{ V}$ $V_{IN} 0 \rightarrow 3.9 \text{ V}, R_L = 3.9 \text{ k}\Omega, C_L = 30 \text{ pF}$
t_{PHL}	Turn-On Time				35	100			ns	$V_{CC} = 5.0 \text{ V}$ $V_{EE} = -10 \text{ V}$ $V_{IN} 0 \rightarrow 3.0 \text{ V}, R_L = 0.39 \text{ k}\Omega, C_L = 30 \text{ pF}$

* V_{DIFF} is a differential input voltage referred from A+ to A- and from B+ to B-.

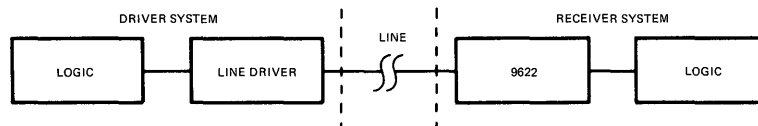
SWITCHING TIME TEST CIRCUIT



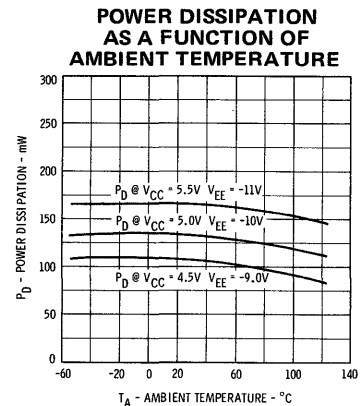
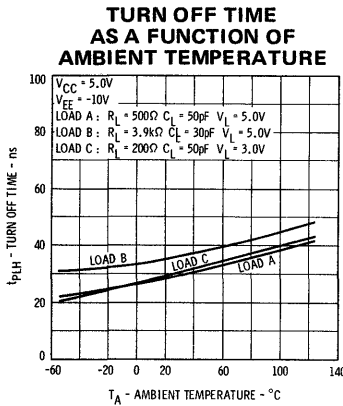
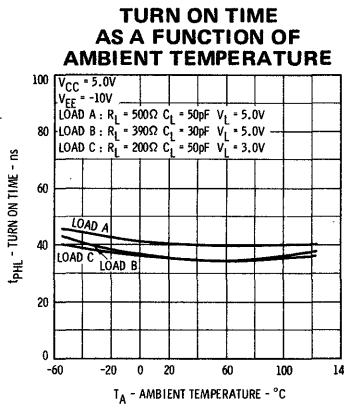
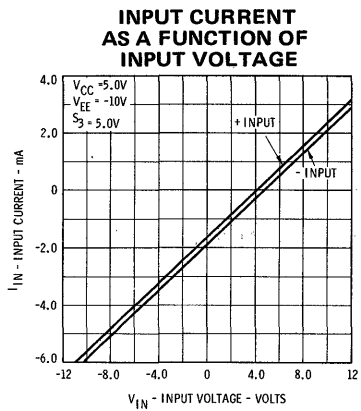
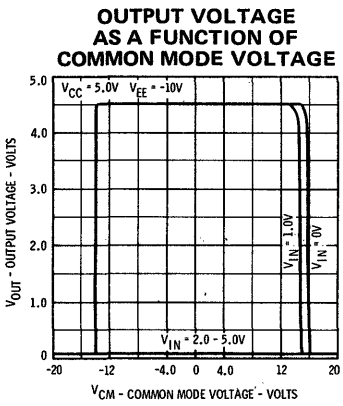
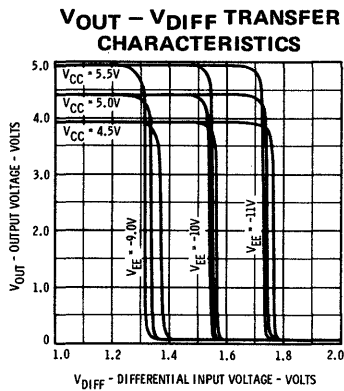
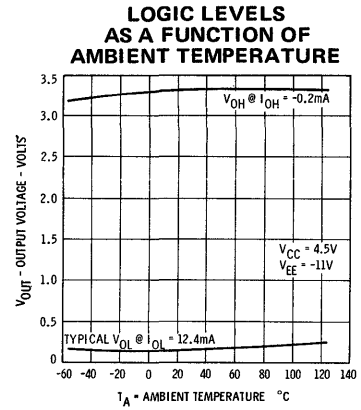
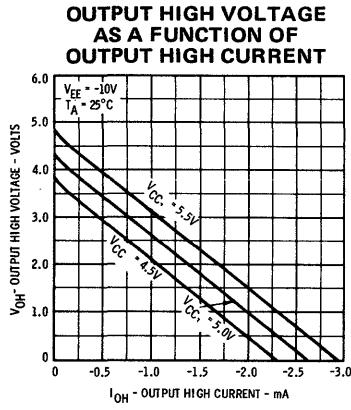
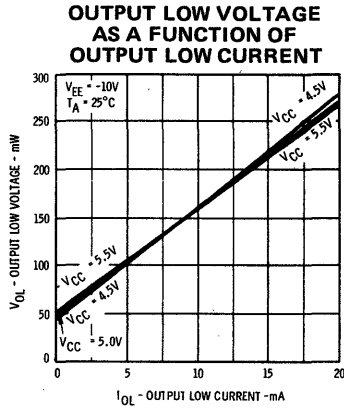
WAVEFORMS



STANDARD USAGE



TYPICAL PERFORMANCE CURVES FOR 9622 AND 9622C



9624•9625

DUAL TTL, MOS INTERFACE ELEMENTS

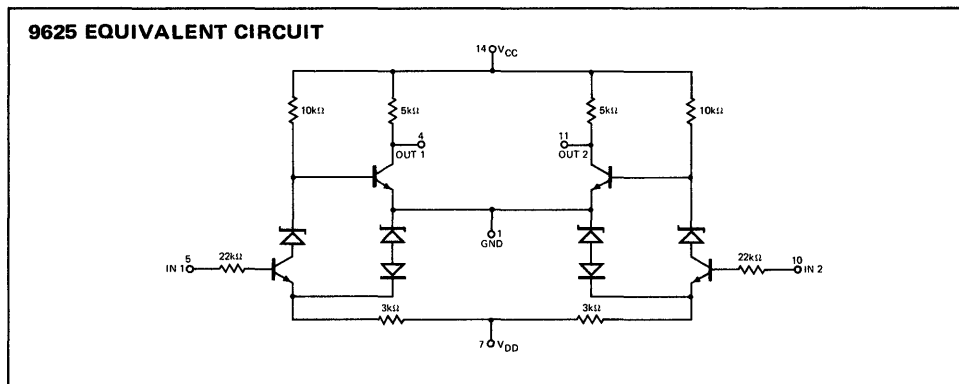
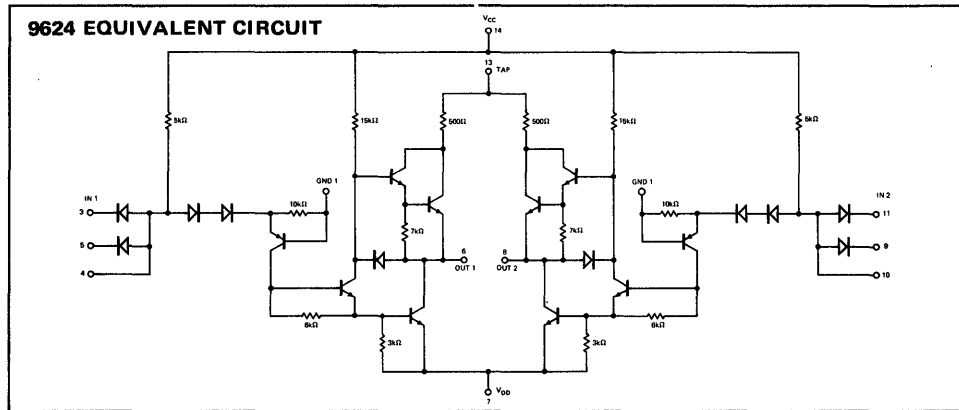
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9624 is a Dual 2-Input TTL Compatible Interface Gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

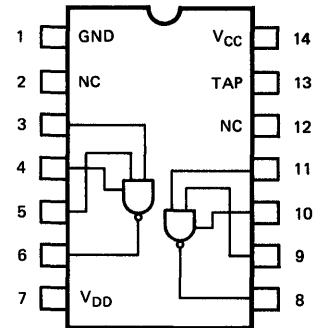
The 9625 is a dual MOS to TTL level converter. It is designed to convert standard negative MOS logic levels to TTL levels. The 9625 features a high input impedance which allows preservation of the driving MOS logic level.

NOTE: The TTL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the 9624 is represented as a NAND gate and the 9625 as a non-inverting buffer. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state "1" or TRUE), the 9624 acts as an AND gate and the 9625 as an inverter.

- TTL COMPATIBLE INPUTS/OUTPUT
- MOS COMPATIBLE OUTPUT/INPUTS
- LOW POWER



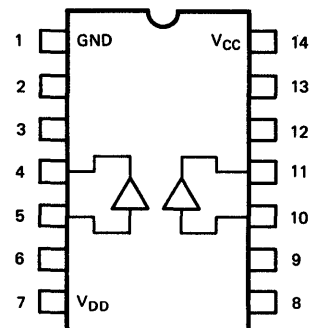
CONNECTION DIAGRAMS
9624
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
9624	9624DM
9624C	9624DC

9625
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
9625	9625DM
9625C	9625DC

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V _{CC} Pin Potential to Ground Pin	V _{DD} to +10 V
Voltage Applied to Outputs for HIGH Output State (9624)	V _{DD} to +V _{CC} value
Voltage Applied to Outputs for HIGH Output State (9625)	-0.5 V to V _{CC} value
Input Voltage (dc) (9624)	-0.5 V to +5.5 V
Input Voltage (dc) (9625)	V _{CC} to V _{DD}
V _{DD} Pin Potential to Ground Pin	-30 V to +0.5 V
V _{DD} Pin Potential to Tap Pin (9624)	-30 V to +0.5 V
V _{TAP}	V _{CC} +0.5 V
Internal Power Dissipation (Note 3)	670 mW
Lead Temperature (Soldering, 60 seconds)	300°C
Operating Temperature Range	
Military (9624 and 9625)	-55°C to +125°C
Commercial (9624C and 9625C)	0°C to +75°C

9624

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS
		-55°C		+25°C		+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.		
V _{OH1}	Output HIGH Voltage	-1.0		-1.0	-0.5		-1.0	Volts	V _{CC} = 4.5 V, V _{DD} = -28 V, V _{TAP} = 0 V I _{OH} = -10 μA
V _{OH2}	Output HIGH Voltage	+3.5		+3.5	+4.0		+3.5	Volts	V _{CC} = 5.5 V, V _{DD} = -20 V, V _{TAP} = 5.5 V Inputs at V _{IL} , I _{OH} = -10 μA
V _{OL}	Output LOW Voltage			See Note 1				Volts	V _{CC} = 4.5 V, I _{OL} = 10 mA, V _{DD} = -15 to 28 V @ V _{IH} , 0 ≤ V _{TAP} ≤ V _{CC} (Note 2)
V _{IH}	Input HIGH Voltage	2.1		1.9			1.7	Volts	Guaranteed Input HIGH Threshold for all Inputs
V _{IL}	Input LOW Voltage		1.4		1.1		0.8	Volts	Guaranteed Input LOW Threshold for all Inputs
I _F	Input Load Current		-1.40		-1.25		-1.13	mA	V _{CC} = 5.5 V, V _F = 0.4 V, V _{DD} = -11 to -28 V
I _R	Input Leakage Current		2.0		2.0		5.0	μA	V _{CC} = 5.5 V, V _R = 4.0 V, V _{DD} = -11 to -28 V
I _{CEX}	Output Leakage Current				50			μA	V _{CC} = 5.5 V, V _{TAP} = 0 V, V _{DD} = -28 V, V _{OUT} = 0 V
I _{SC}	Output Short-Circuit Current	-12	-31	-14		-32	-11	mA	V _{CC} = 4.5 V, V _{TAP} = 0 V, V _{IN} = 0 V V _{DD} = -11 V, V _{OUT} = -11 V
I _{VCC}	V _{CC} Supply Current					6.1		mA	V _{CC} = 5.5 V, V _{DD} = -15 V, V _{TAP} = 0 V Inputs Open
I _{MAX}	Max. Current					10		mA	V _{CC} = 10 V, V _{DD} = -30 V, Inputs Open V _{TAP} = 0 V
t _{PLH}	Switching Speed				190	250		ns	V _{CC} = 5.0 V, See Figure 1
t _{PHL}	Switching Speed				50	100		ns	V _{DD} = -13 V, V _{TAP} = 0 V

9624C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS
		0°C		+25°C		+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.		
V _{OH1}	Output HIGH Voltage	-1.0		-1.0	-0.5		-1.0	Volts	V _{CC} = 4.75 V, V _{DD} = -28 V, V _{TAP} = 0 V I _{OH} = -10 μA
V _{OH2}	Output HIGH Voltage	+3.25		+3.25	+3.75		+3.25	Volts	V _{CC} = 5.25 V, V _{DD} = -20 V, V _{TAP} = 5.25 V I _{OH} = -10 μA, Inputs at V _{IL}
V _{OL}	Output LOW Voltage			See Note 1				Volts	V _{CC} = 4.5 V, I _{OL} = 10 mA, V _{DD} = -11 to -28 V @ 0 ≤ V _{TAP} ≤ V _{CC} (Note 2)
V _{IH}	Input HIGH Voltage	2.0		1.9			1.8	Volts	Guaranteed Input HIGH Threshold for all Inputs
V _{IL}	Input LOW Voltage		1.2		1.1		0.95	Volts	Guaranteed Input LOW Threshold for all Inputs
I _F	Input Load Current		-1.32		-1.25		-1.20	mA	V _{CC} = 5.25 V, V _F = 0.45 V
I _R	Input Leakage Current		5.0		5.0		10	μA	V _{CC} = 5.25 V, V _R = 4.5 V
I _{CEX}	Output Leakage Current				100			μA	V _{CC} = 5.25 V, V _{TAP} = 0 V V _{DD} = -28 V, V _{OUT} = 0 V
I _{SC}	Output Short-Circuit Current	-12	-31	-14		-32	-12	mA	V _{CC} = 4.75 V, V _{TAP} = 0 V, V _{IN} = 0 V V _{DD} = -11 V, V _{OUT} = -11 V
I _{VCC}	V _{CC} Supply Current					6.1		mA	V _{CC} = 5.25 V, V _{DD} = -15 V, V _{TAP} = 0 V Input Open
I _{MAX}	Max. Current					10		mA	V _{CC} = 8.0 V, V _{DD} = -30 V, V _{TAP} = 0 V Input Open
t _{PLH}	Switching Speed				190	250		ns	V _{CC} = 5.0 V, See Figure 1
t _{PHL}	Switching Speed				50	100		ns	V _{DD} = -13 V, V _{TAP} = 0 V

9625

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS	
		-55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.			MAX.
V _{OH}	Output HIGH Voltage	2.5		2.6			2.5		Volts	V _{CC} = 4.5 V, I _{OH} = -60 μA V _{DD} = -11 V, Inputs at V _{IH}
V _{OL}	Output LOW Voltage	0.5					0.5		Volts	V _{CC} = 5.5 V, I _{OL} = 1.5 mA V _{CC} = 4.5 V, I _{OL} = 1.2 mA V _{DD} = -11 V, Inputs at V _{IL}
V _{IH}	Input HIGH Voltage	-3.0		-3.0			-3.0		Volts	Guaranteed Input HIGH Threshold for all Inputs
V _{IL}	Input LOW Voltage	-9.0		-9.0			-9.0		Volts	Guaranteed Input LOW Threshold for all Inputs
I _F	Input Load Current	210		210			210		μA	V _{CC} = 5.0 V, V _F = -3.0 V, V _{DD} = -13 V
I _{CEX}	Output Leakage Current			50					μA	V _{CC} = V _{CEX} = 4.5 V, V _{DD} = -13 V
I _{VCCL}	Supply Current			4.8					mA	V _{CC} = 5.5 V, V _{DD} = -15 V, V _{IN} = -10 V
I _{VCCH}	Supply Current			2.1					mA	V _{CC} = 5.5 V, V _{DD} = -15 V, V _{IN} = 0 V
I _{VDD}	V _{DD} Supply Current			-9.0					mA	V _{CC} = 5.5 V, V _{DD} = -15 V Input Open or GND
I _{MAX}	Max. V _{DD} Supply Current			-25					mA	V _{CC} = 8.0 V, V _{DD} = -20 V, V _{IN} = 0 V
t _{PLH}	Switching Speed			55 100					ns	V _{CC} = 5.0 V, V _{DD} = -13 V
t _{PHL}	Switching Speed			90 150					ns	See Figure 2

9625C

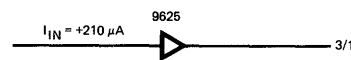
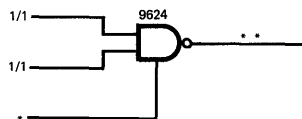
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS	
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.			MAX.
V _{OH}	Output HIGH Voltage	2.5		2.6			2.5		Volts	V _{CC} = 4.75 V, I _{OH} = -60 μA V _{DD} = -11 V, Inputs at V _{IH}
V _{OL}	Output LOW Voltage	0.5		0.5			0.5		Volts	V _{CC} = 5.25 V, I _{OL} = 1.52 mA V _{CC} = 4.75 V, I _{OL} = 1.33 mA, Inputs at V _{IL}
V _{IH}	Input HIGH Voltage	-3.0		-3.0			-3.0		Volts	Guaranteed Input HIGH Threshold for all Inputs
V _{IL}	Input LOW Voltage	-9.0		-9.0			-9.0		Volts	Guaranteed Input LOW Threshold for all Inputs
I _F	Input Load Current	210		210			210		μA	V _{CC} = 5.0 V, V _F = -3.0 V, V _{DD} = -13 V
I _{CEX}	Output Leakage Current			100					μA	V _{CC} = V _{CEX} = 4.75 V, V _{DD} = -13 V
I _{VCCL}	Supply Current			4.8					mA	V _{CC} = 5.25 V, V _{DD} = -15 V, V _{IN} = -10 V
I _{VCCH}	Supply Current			2.1					mA	V _{CC} = 5.25 V, V _{DD} = -15 V, V _{IN} = 0 V
I _{VDD}	V _{DD} Supply Current			-9.0					mA	V _{CC} = 5.5 V, V _{DD} = -15 V Input Open or GND
I _{MAX}	Max. V _{DD} Supply Current			-25					mA	V _{CC} = 8.0 V, V _{DD} = -20 V, V _{IN} = 0 V
t _{PLH}	Switching Speed			55 100					ns	V _{CC} = 5.0 V, V _{DD} = -13 V
t _{PHL}	Switching Speed			90 150					ns	See Figure 2

NOTES

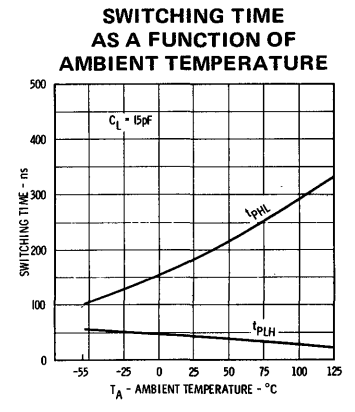
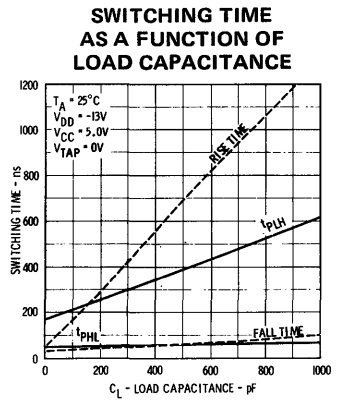
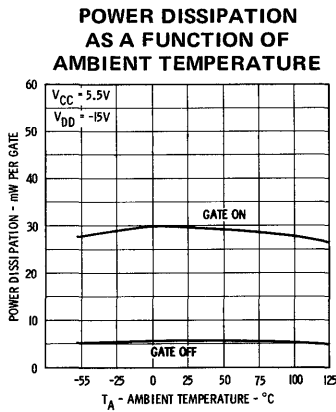
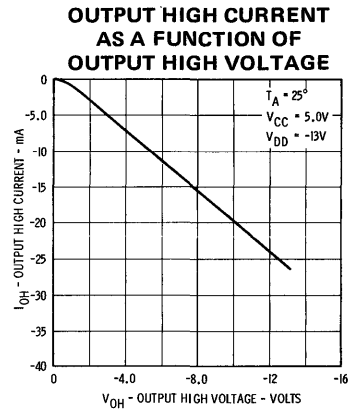
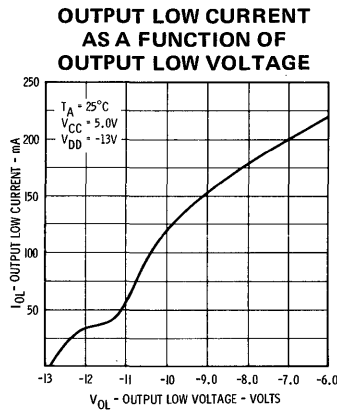
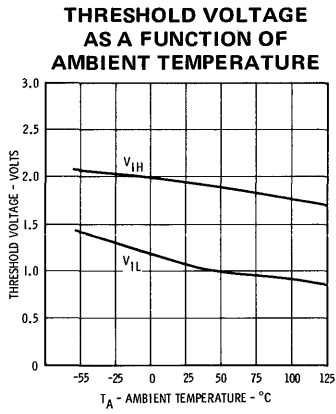
1. Max = V_{DD} +1.0 V over Temperature Range. Typ = V_{DD} +0.2 V over Temperature Range.
2. At no time shall the voltage from V_{DD} to V_{TAP} exceed 30 V. See Absolute Maximum Ratings.
3. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C.

LOADING RULES:

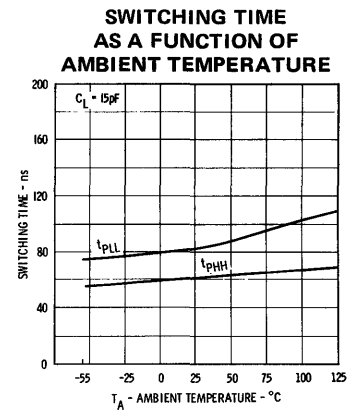
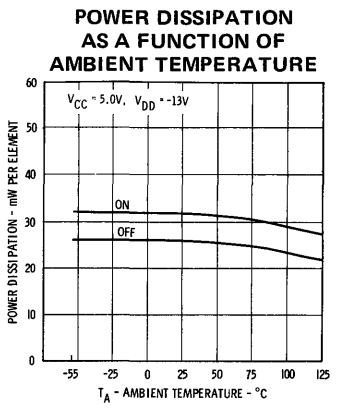
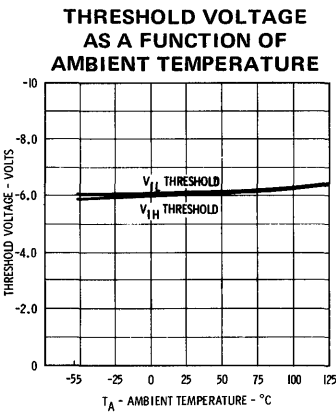


- *The extender pin allows the number of inputs to be extended by adding diodes or the DTμL 933 extender.
- **Fan out into MOS is limited only by MOS leakage currents.

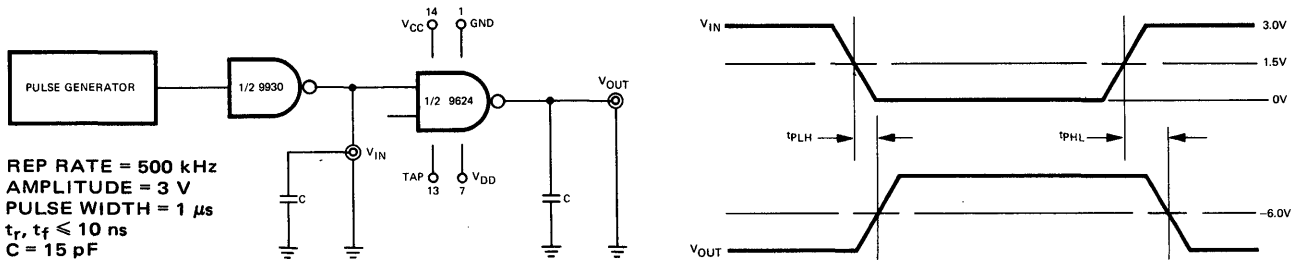
TYPICAL PERFORMANCE CURVES FOR 9624 AND 9624C



TYPICAL PERFORMANCE CURVES FOR 9625 AND 9625C



9624 SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

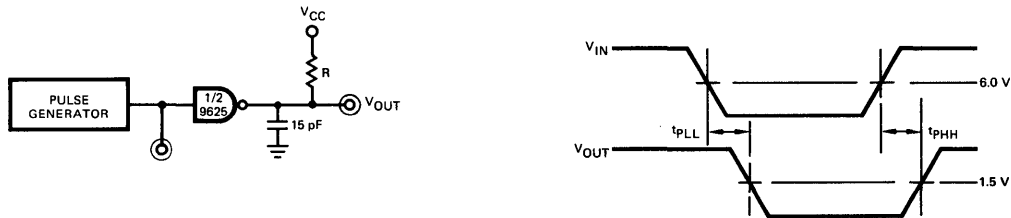


REP RATE = 500 kHz
 AMPLITUDE = 3 V
 PULSE WIDTH = 1 μ s
 $t_r, t_f \leq 10$ ns
 C = 15 pF

TESTS	CONDITIONS			
	T_A ($^{\circ}$ C)	V_{CC} (Volts)	V_{DD} (Volts)	Tap Voltage
t_{PLH}, t_{PHL}	25	5.0	-13	0

Fig. 1

9625 SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



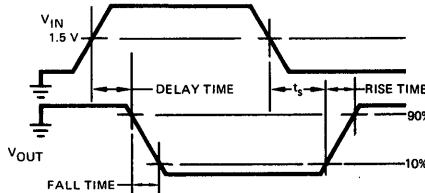
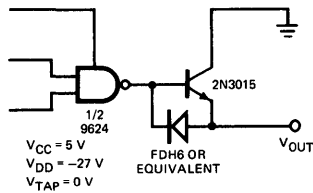
Rep Rate = 500 kHz
 Amplitude = -10 V
 Pulse Width = 1.0 μ s
 $t_r, t_f = 20$ ns

TESTS	CONDITIONS			
	T_A ($^{\circ}$ C)	V_{CC} (Volts)	V_{DD} (Volts)	R (k Ω)
t_{PLL}, t_{PHH}	25	5.0	-13	3.75

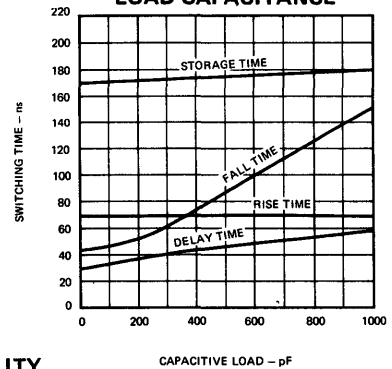
Fig. 2

APPLICATIONS

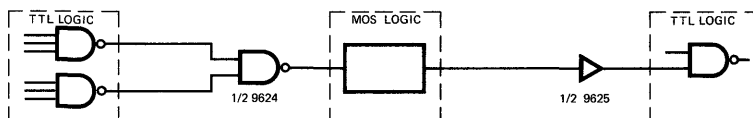
9624 Clock Driving
 (using a high capacitance drive scheme)



TYPICAL SWITCHING TIMES AS A FUNCTION OF LOAD CAPACITANCE



INCREASING HIGH DRIVE LEVEL CAPABILITY



9627

DUAL EIA RS-232-C/MIL-STD-188C LINE RECEIVER

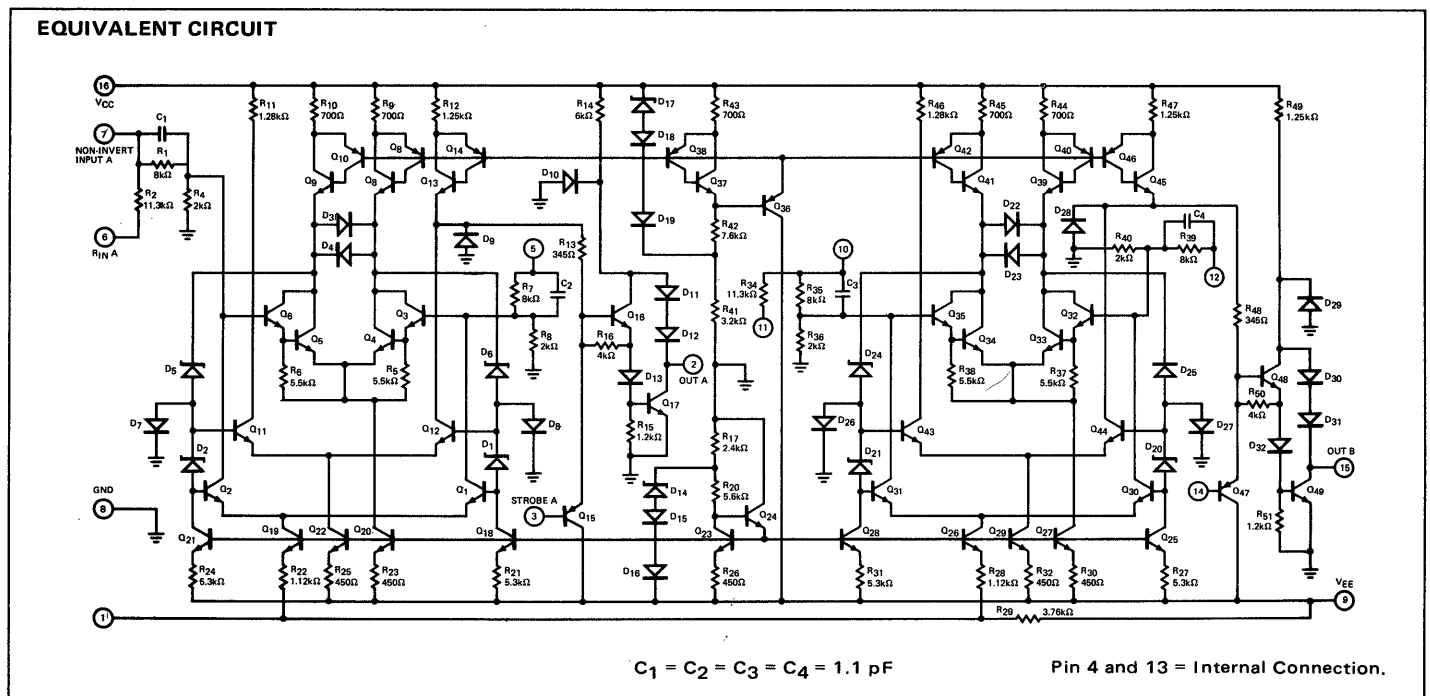
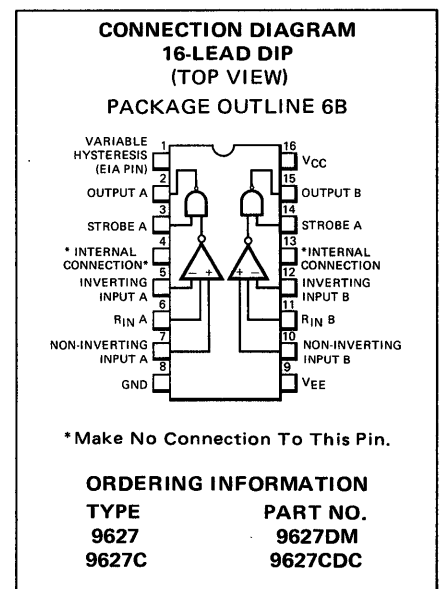
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 9627 is a Dual Line Receiver which meets the electrical interface specifications of EIA RS-232-C and MIL-STD-188C. The input circuitry accommodates $\pm 25V$ input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The 9627 provides both a selectable hysteresis range and selectable receiver input resistance. When pin 1 is tied to V_{EE} , the switching points are at $+2.6V$ and $-2.6V$, thus meeting RS-232-C requirements. When pin 1 is open, the switching points are at $+0.45V$ and $-0.45V$, thus satisfying the requirements for MIL-STD-188C LOW level interface. Connecting the R_{IN} pin to the (-) input yields an input impedance in the range of $3k\Omega$ to $7k\Omega$ and satisfies RS-232-C requirements; leaving R_{IN} unconnected, the input resistance will be greater than $6k\Omega$ to satisfy MIL-STD-188C.

The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wire-AND function. A TTL/DTL strobe is also provided for each receiver. The EIA failsafe mode of operation is shown in the application section of this data sheet.

For the complementary function, see the 9616 triple EIA RS-232C/MIL-STD-188 line driver.

- EIA RS-232-C INPUT STANDARDS
- MIL-STD-188C INPUT STANDARDS
- VARIABLE HYSTERESIS CONTROL
- HIGH COMMON MODE REJECTION
- R_{IN} CONTROL ($5k\Omega$ OR $10k\Omega$)
- WIRED-OR CAPABILITY
- CHOICE OF INVERTING AND NON-INVERTING INPUTS
- OUTPUTS AND STROBE TTL COMPATIBLE



FAIRCHILD LINEAR INTEGRATED CIRCUIT • 9627

ABSOLUTE MAXIMUM RATINGS

V _{CC} to Ground	0V to +15V
V _{EE} to Ground	0V to -15V
Input Voltage Referred to Ground Pin	±25V
Strobe to Ground Voltage	-0.5V to +5.5V
Maximum Applied Output Voltage	-0.5V to +15V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (9627)	-55°C to +125°C
Commercial (9627C)	0°C to +75°C
Maximum Power Dissipation (Note 1)	730mW
Lead Temperature (Soldering, 60 seconds)	300°C

NOTE

- Rating applies up to 75°C ambient temperature. Above 75°C derate linearly at 8.3mW/°C.

9627 • 9627C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V ±10%, V_{EE} = 12V ±10% Over Operating Temperature Range, Unless Otherwise Specified)

MIL-STD-188C

SYMBOL	PARAMETER	CONDITIONS (Pins 6 and 11 open. Inverting inputs open. Pin 1 open.)	MIN.	TYP.	MAX.	UNITS
V _{OL}	Output LOW Voltage	V _{CC} = +10.8V, V _{EE} = -13.2V Non-Inverting Input = -0.6V, I _{OL} = 6.4mA			0.4	V
V _{OH}	Output HIGH Voltage	V _{CC} = +10.8V, V _{EE} = -13.2V	2.4			V
I _{SC}	Output Shorted Current	V _{CC} = +13.2V, V _{EE} = -10.8V Non-Inverting Input = +0.6V Outputs Grounded			3.0	mA
I _{IH} (Strobe)	Input HIGH Current (Strobe)	V _{CC} = +10.8V, V _{EE} = -13.2V Non-Inverting Input = +0.6V			40	μA
		V _S = 2.4V			1.0	mA
R _{IN}	Input Resistance	V _{CC} = +13.2V, V _{EE} = -13.2V Non-Inverting Input = +3V or -3V	6k			Ω
I _{TH+}	Positive Threshold Current	V _{OUT} = 2.4 V			100	μA
I _{TH-}	Negative Threshold Current	V _{OUT} = 0.4 V	-100			μA
	I _{TH+} + and I _{TH-} Magnitude Matching Error				±10	%
V _{IL} (Strobe)	Input LOW Voltage (Strobe)	V _{Non-Inverting Input} = -0.6V			0.8	V
V _{IH} (Strobe)	Input HIGH Voltage (Strobe)	V _{Non-Inverting Input} = +0.6V V _{CC} = +13.2V, V _{EE} = -10.8V	2.0			V
I ₊	Positive Supply Current	V _{Non-Inverting Input} = -0.6V		11.5	13.4	mA
I ₋	Negative Supply Current	V _{Non-Inverting Input} = +0.6V	-10.4	-8.0		mA

RS-232C

SYMBOL	PARAMETER	CONDITIONS (Non-inverting inputs connected to ground, R _{IN} inputs connected to inverting inputs)	MIN.	TYP.	MAX.	UNITS
R _{IN}	Input Resistance	V _{IN} = +3.0V to +25V	3.0		7.0	kΩ
		V _{IN} = -3.0V to -25V	3.0		7.0	kΩ
V _{IN}	Input Voltage	Open Circuit	-2.0		2.0	V
V _{TH+}	Positive Threshold Voltage				0.6	V
V _{TH-}	Negative Threshold Voltage		-0.6			V

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 9627

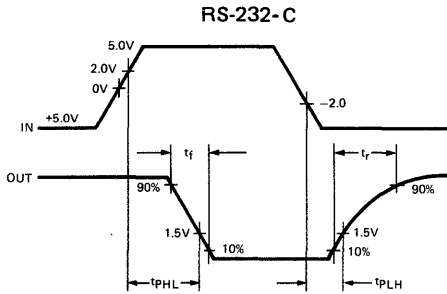
9627 • 9627C

AC CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = +12.0\text{V}$, $V_{EE} = -12.0\text{V}$)

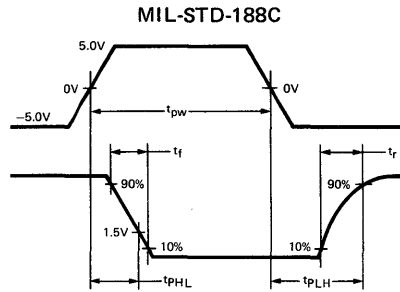
MIL-STD-188C • RS-232-C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
t_{PLH}	Propagation Delay Time	$V_{IN} = 10\text{Vp-p}$, Shaped for 10kHz		60	250	ns
t_{PHL}	Propagation Delay Time	$V_{IN} = 10\text{Vp-p}$, Shaped for 10kHz		84	250	ns

SWITCHING WAVEFORMS

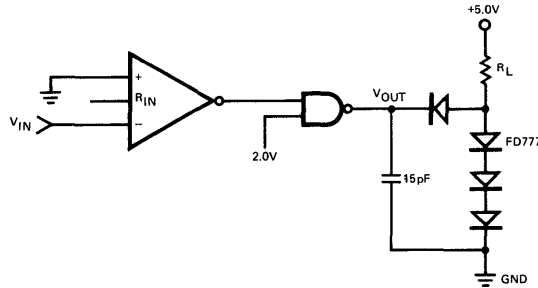


$PRR = 10\text{kHz}$
 $PW = 50\mu\text{s}$
 $4\text{V}/\mu\text{s} \leq \text{Slope} \leq 30\text{V}/\mu\text{s}$
 $390\Omega \leq R_L \leq 3.9\text{k}\Omega$

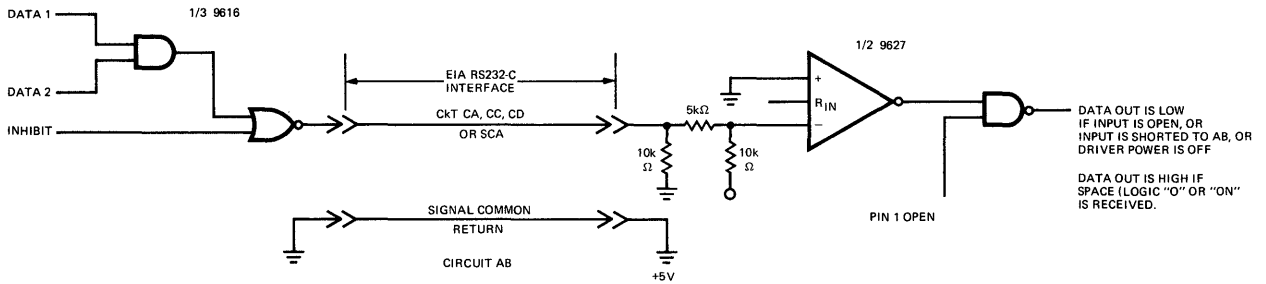


$R_L = 390\Omega$ $R_L = 3.9\text{k}\Omega$
 $t_{pw} = 50\mu\text{s}$
 t_r and $t_f = 5 \pm 2.5\mu\text{s}$

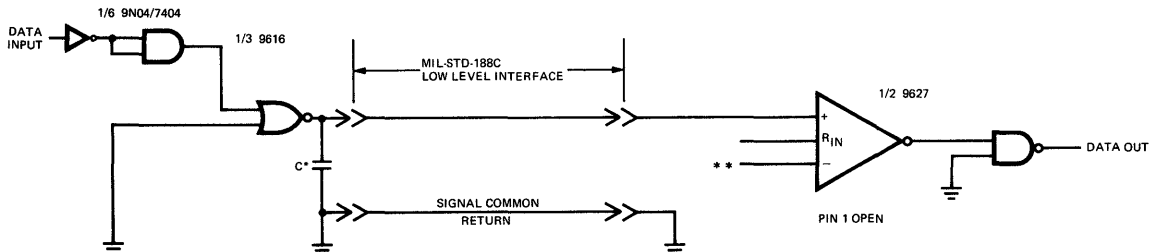
SWITCHING TIME TEST CIRCUIT



EIA RS-232-C INTERFACE WITH FAILSAFE RECEIVER



MIL-STD-188C INTERFACE



* Capacitor For Transmitter Waveshaping at Applicable Modulation Rate.

** For balanced input threshold, leave unused input open. (Don't connect to ground.)

9650

4-BIT CURRENT SOURCE

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9650 is a high speed, 4-Bit Precision Current Source, intended for use in D/A and A/D converters with up to 12-bit accuracy. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process and consists of a reference transistor and four logic operated precision current sources connected to a single output summing line. Logic inputs are fully TTL compatible under all temperature and supply conditions. A clamp circuit is provided to prevent turn on latchup on the reference input.

- 200 ns SETTLING TIME ($12 \pm 1/2$ LSB)
- STANDARD SUPPLY LEVELS
- VARIABLE BIT CURRENTS
- REFERENCE COMPENSATION
- TTL COMPATIBLE

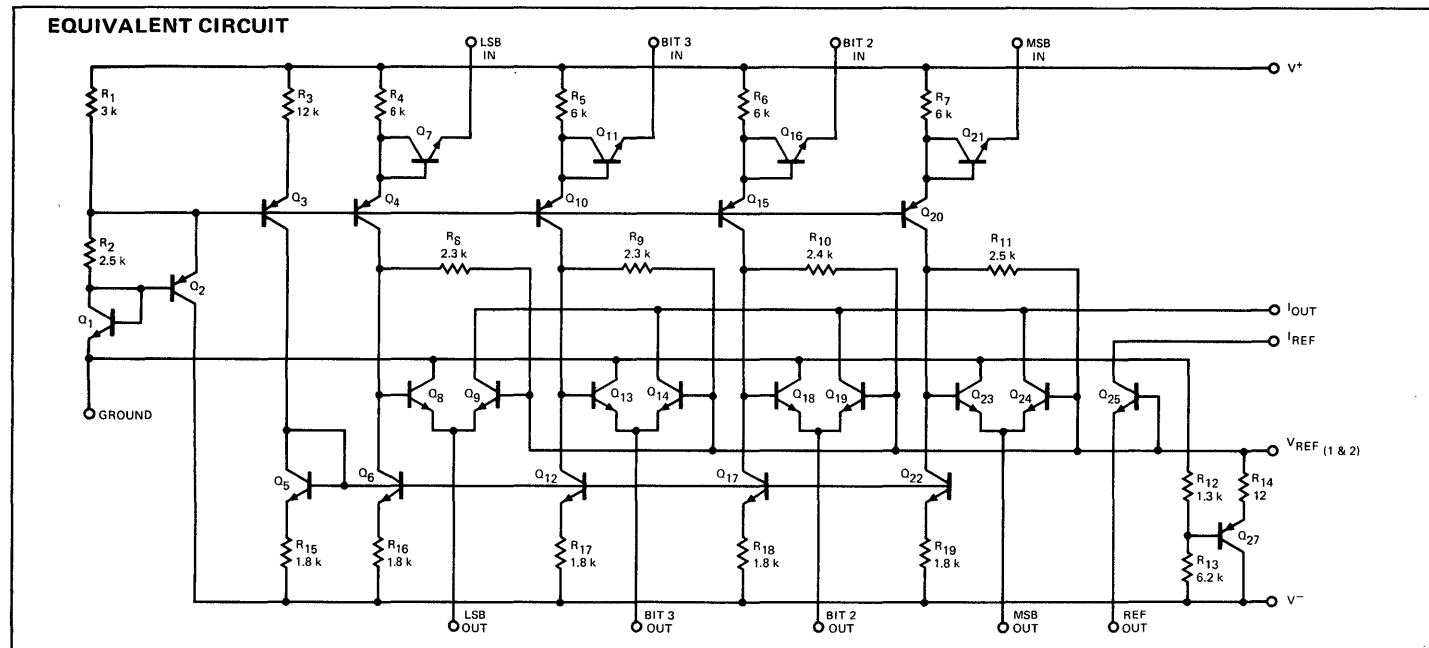
ABSOLUTE MAXIMUM RATINGS

V+	+7 V
V-	-18 V
MSB Current	2.0 mA
Logic Input Voltage	+5.5 V
Power Dissipation (Note 1)	730 mW
Storage Temperature	-65°C to +150°C
Operating Temperature	
Military (9650-1, 9650-2, 9650-3)	-55°C to +125°C
Commercial (9650-1C, 9650-2C, 9650-3C)	0°C to 70°C
Lead Temperature (Soldering, 60 seconds)	+300°C
VREF Inputs	+7 V to V-
Output (Note 2)	+18 V to VREF

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6B

ORDER INFORMATION

TYPE	PART NO.
9650-1	9650-1DM
9650-2	9650-2DM
9650-3	9650-3DM
9650-1C	9650-1DC
9650-2C	9650-2DC
9650-3C	9650-3DC



Notes on following page.

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 9650

9650-1 • 9650-2 • 9650-3

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Power Supply Range 4.5 V, -14 V to 5.5 V, -16 V, unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (TYPE)	MIN.	TYP.	MAX.	UNITS
Linearity	(9650-1)			±0.01	% of FSI
	(9650-2)			±0.05	% of FSI
	(9650-3)			±0.2	% of FSI
Full Scale Output Current Error	(9650-1)			±0.1	%
	(9650-2)			±0.2	%
	(9650-3)			±0.4	%
Power Supply Coefficient of Full Scale Output Current	(9650-1)			±0.0025	%/V
	(9650-2, 9650-3)			±0.01	%/V
V_{BE} Range	(9650-1, 9650-2)	570		630	mV
	(9650-3)	550		650	mV
h_{FE} of Reference Transistor	(9650-1)	500	1500		
	(9650-2, 9650-3)	300	1000		
Output Impedance	All Bits On		5.0		MΩ

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$

Accuracy	(9650-1)			±0.025	% of FSI
	(9650-2)			±0.1	% of FSI
	(9650-3)			±0.3	% of FSI
Full Scale Output Current Error	(9650-1)			±0.2	%
	(9650-2)			±0.3	%
	(9650-3)			±0.6	%
Power Supply Coefficient of Full Scale Output Current	(9650-1)			±0.005	%/V
	(9650-2, 9650-3)			±0.02	%/V
Input LOW Voltage	Each Bit On			0.7	V
Input HIGH Voltage	Each Bit Off	2.0			V
Input LOW Current	$V_{IL} = 0.4\text{ V}$			-1.6	mA
Input HIGH Current	$V_{IH} = 2.4\text{ V}$			40	μA
Output Current	Bit 1 (MSB)		1.0	2.0	mA
	Bit 2		0.5	1.0	mA
	Bit 3		0.25	0.5	mA
	Bit 4 (LSB)		0.125	0.25	mA
Output Current	All Bits Off				
	(9650-1)		5.0	250	nA
	(9650-2, 9650-3)		5.0	500	nA
Output Voltage	Feeding Op Amp Summing Junction Resistive Load		0		V
		-4.0		V^+	V
Reference Current	Using Compensation Transistor		1.0		mA
V_{REF} Current			±1.0	±2.2	mA
Reference Limit Current	$V_{REF} = 0\text{ V}$	20		75	mA
Positive Supply Current	(9650-1, 9650-2)			8.0	mA
	(9650-3)			10	mA
Negative Supply Current	(9650-1, 9650-2)			-11	mA
	(9650-3)			-15	mA

NOTES:

1. Rating applies for ambient temperature to 70°C . Derate linearly at $9.1\text{ mW}/^\circ\text{C}$ for ambient temperatures above 70°C .
2. V_{REF} Voltage $\geq -7.0\text{ V}$.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 9650

9650-1C • 9650-2C • 9650-3C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Power Supply Range 4.5 V, -14 V to 5.5 V, -16 V, unless otherwise specified)

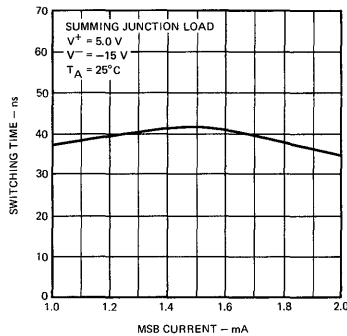
PARAMETER (see definitions)	CONDITIONS (TYPE)	MIN.	TYP.	MAX.	UNITS
Linearity	(9650-1C)			±0.01	% of FSI
	(9650-2C)			±0.05	% of FSI
	(9650-3C)			±0.2	% of FSI
Full Scale Output Current Error	(9650-1C)			±0.1	%
	(9650-2C)			±0.2	%
	(9650-3C)			±0.4	%
Power Supply Coefficient of Full Scale Output Current	(9650-1C 9650-2C, 9650-3C)			±0.003	%/V
				±0.012	%/V
V_{BE} Range	(9650-1C, 9650-2C) 9650-3C)	570		630	mV
		550		650	mV
h_{FE} of Reference Transistor	(9650-1C) 9650-2C, 9650-3C)	500	1500		
		300	1000		
Output Impedance	All Bits On		5.0		M Ω

The following specifications apply for $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$

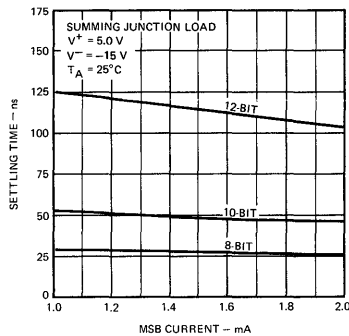
Accuracy	(9650-1C) 9650-2C) 9650-3C)			±0.025	% of FSI
				±0.1	% of FSI
				±0.3	% of FSI
Full Scale Output Current Error	(9650-1C) 9650-2C) 9650-3C)			0.2	%
				0.3	%
				0.6	%
Power Supply Coefficient of Full Scale Output Current	(9650-1C) 9650-2C, 9650-3C)			±0.006	%/V
				±0.024	%/V
Input LOW Voltage	Each Bit On			0.8	V
Input HIGH Voltage	Each Bit Off	2.0			V
Input LOW Current	$V_{IL} = 0.4\text{ V}$			-1.6	mA
Input HIGH Current	$V_{IH} = 2.4\text{ V}$			40	μA
Output Current	Bit 1 (MSB) Bit 2 Bit 3 Bit 4 (LSB)		1.0	2.0	mA
			0.5	1.0	mA
			0.25	0.5	mA
			0.125	0.25	mA
Output Current	All Bits Off 9650-1C) 9650-2C, 9650-3C)		5.0	250	nA
			5.0	500	nA
Output Voltage	Feeding Op Amp Summing Junction Resistive Load	-4.0	0	V^+	V
					V
Reference Current	Using Compensation Transistor		1.0		mA
V_{REF} Current			±1.0	±2.2	mA
Reference Limit Current	$V_{REF} = 0\text{ V}$	20		75	mA
Positive Supply Current	(9650-1C, 9650-2C) 9650-3C)			8.0	mA
				10	mA
Negative Supply Current	(9650-1C, 9650-2C) 9650-3C)			-11	mA
				-15	mA

TYPICAL PERFORMANCE CURVES

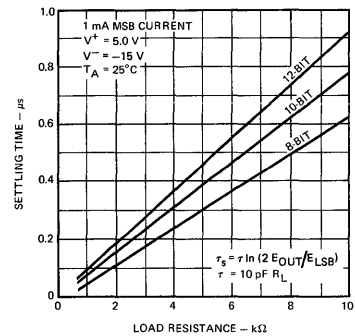
SWITCHING TIME AS A FUNCTION OF MSB CURRENT (50% IN TO 10% OUT)



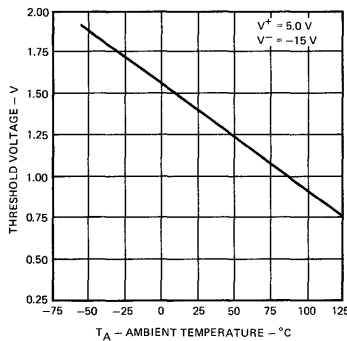
OUTPUT CURRENT SETTLING TIME AS A FUNCTION OF MSB CURRENT (0 TO FSI OUTPUT ± 1/2 LSB)



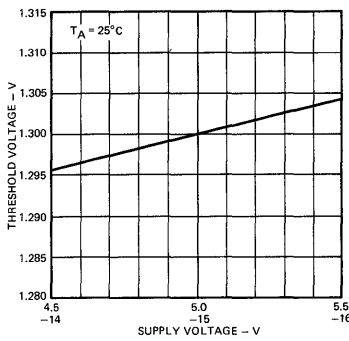
SETTLING TIME AS A FUNCTION OF LOAD RESISTANCE (0 TO FSI OUTPUT ± 1/2 LSB)



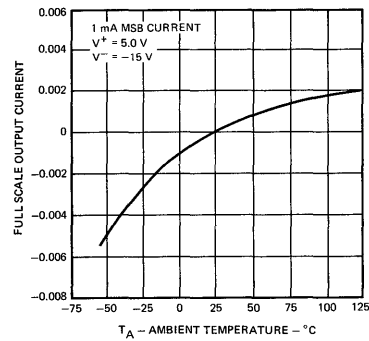
INPUT LOGIC THRESHOLD VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT LOGIC THRESHOLD VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



FULL SCALE OUTPUT CURRENT DRIFT AS A FUNCTION OF AMBIENT TEMPERATURE



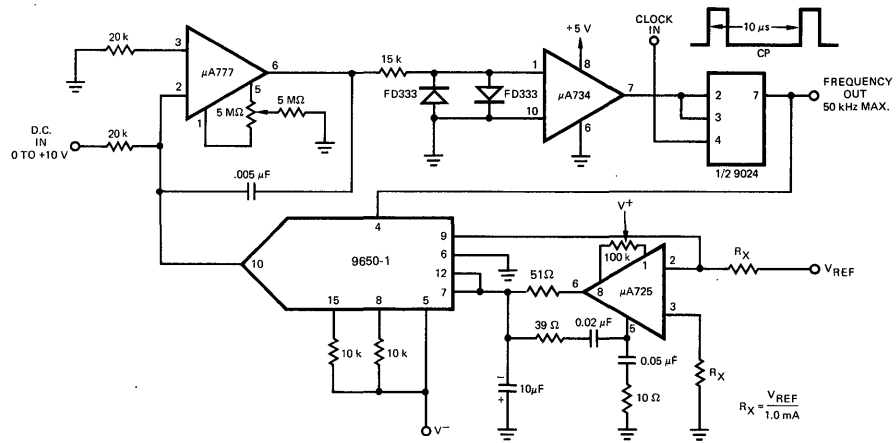
TRUTH TABLE

LOGIC INPUT	NOMINAL OUTPUT CURRENT (mA)	LOGIC INPUT	NOMINAL OUTPUT CURRENT (mA)
0000	1.875	1000	0.875
0001	1.750	1001	0.750
0010	1.625	1010	0.625
0011	1.500	1011	0.500
0100	1.375	1100	0.375
0101	1.250	1101	0.250
0110	1.125	1110	0.125
0111	1.000	1111	0.000

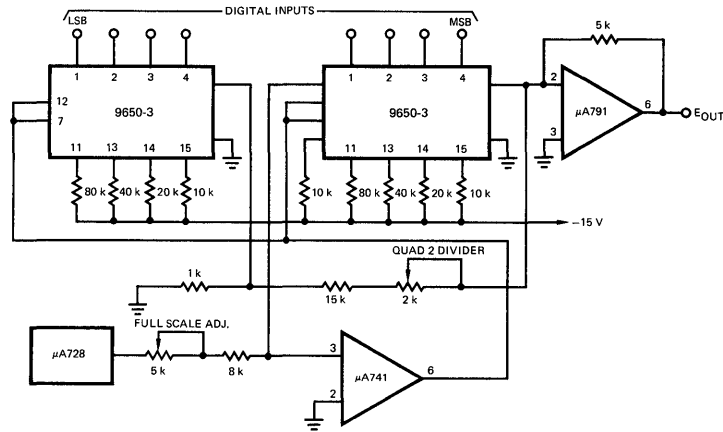
9650 KITS TO BUILD D/A – A/D CONVERTERS

TEMPERATURE RANGE	TYPE			
	-55°C to +125°C	9650-1	9650-2	9650-3
0°C to +70°C	9650-1C	9650-2C	9650-3C	
Accuracy to	NO. OF UNITS			
	8 Bits	0	0	2
	10 Bits	0	1	2
	12 Bits	1	1	1

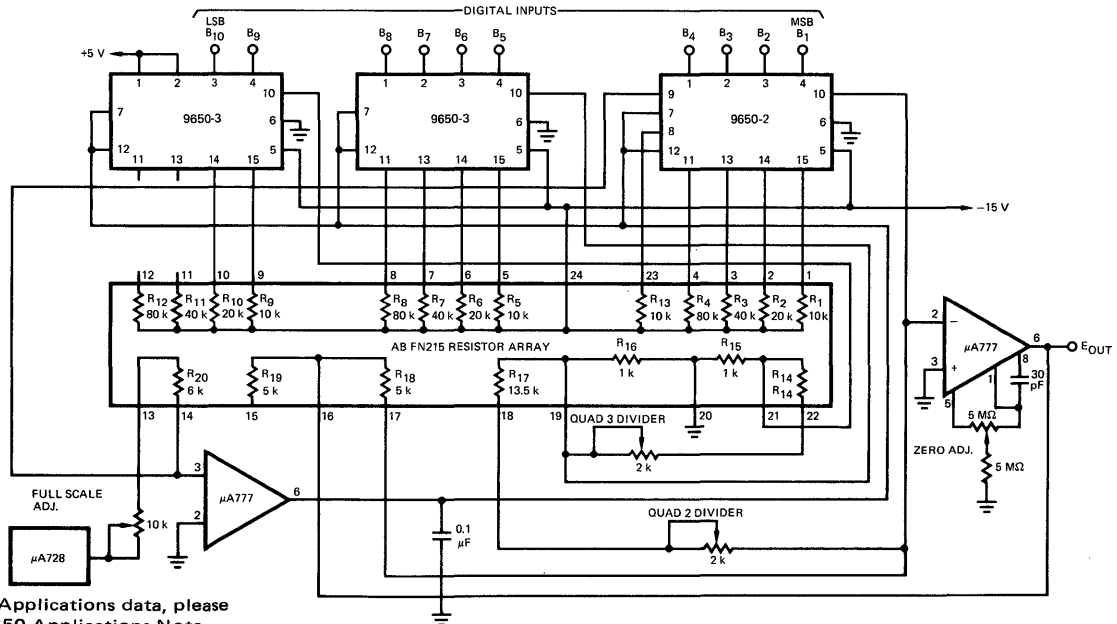
TYPICAL APPLICATIONS †
VOLTAGE TO FREQUENCY CONVERTER



8-BIT D/A CONVERTER



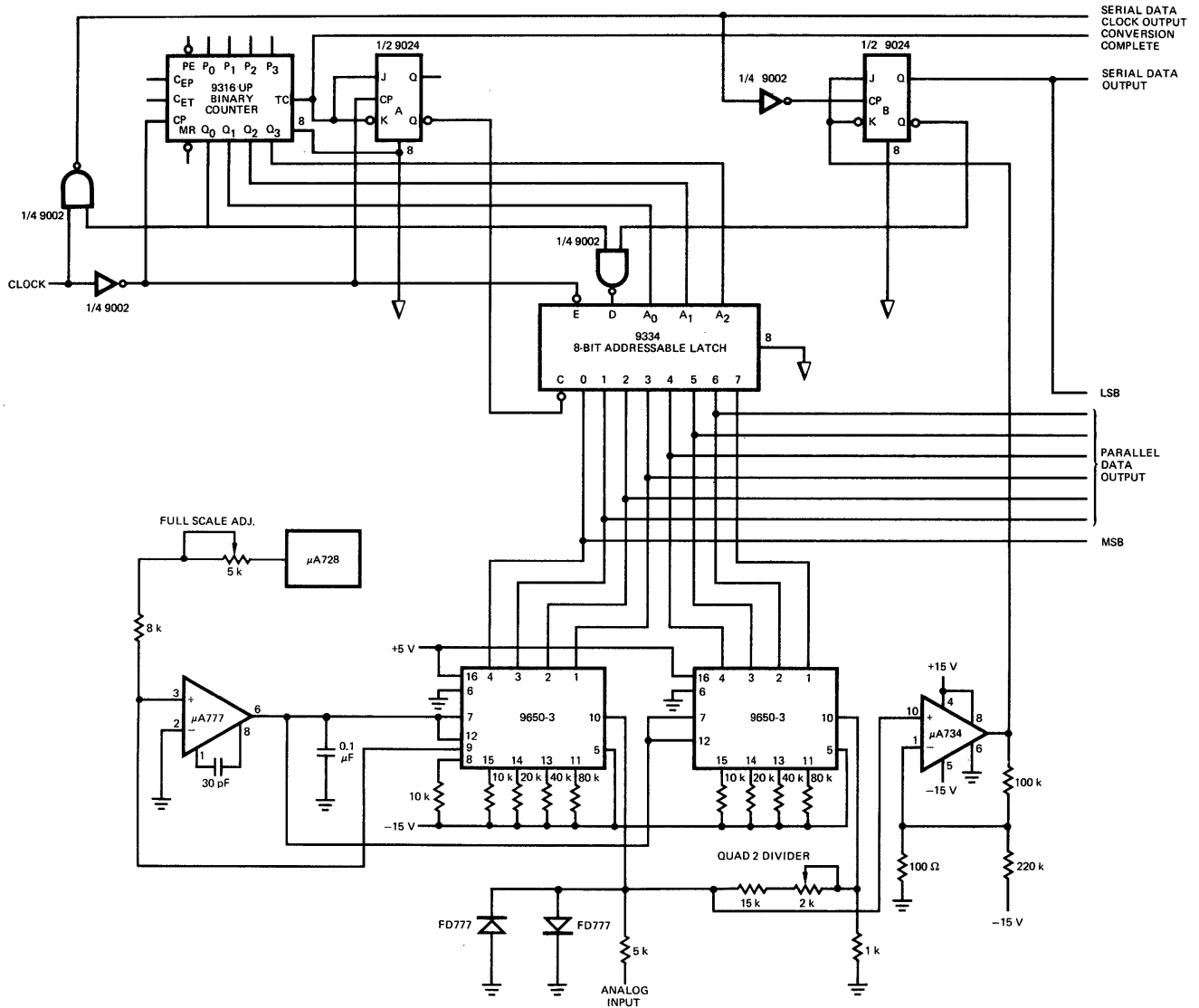
10-BIT D/A CONVERTER



† For complete Applications data, please request our 9650 Applications Note.

TYPICAL APPLICATIONS (cont'd)†

8-BIT A/D CONVERTER

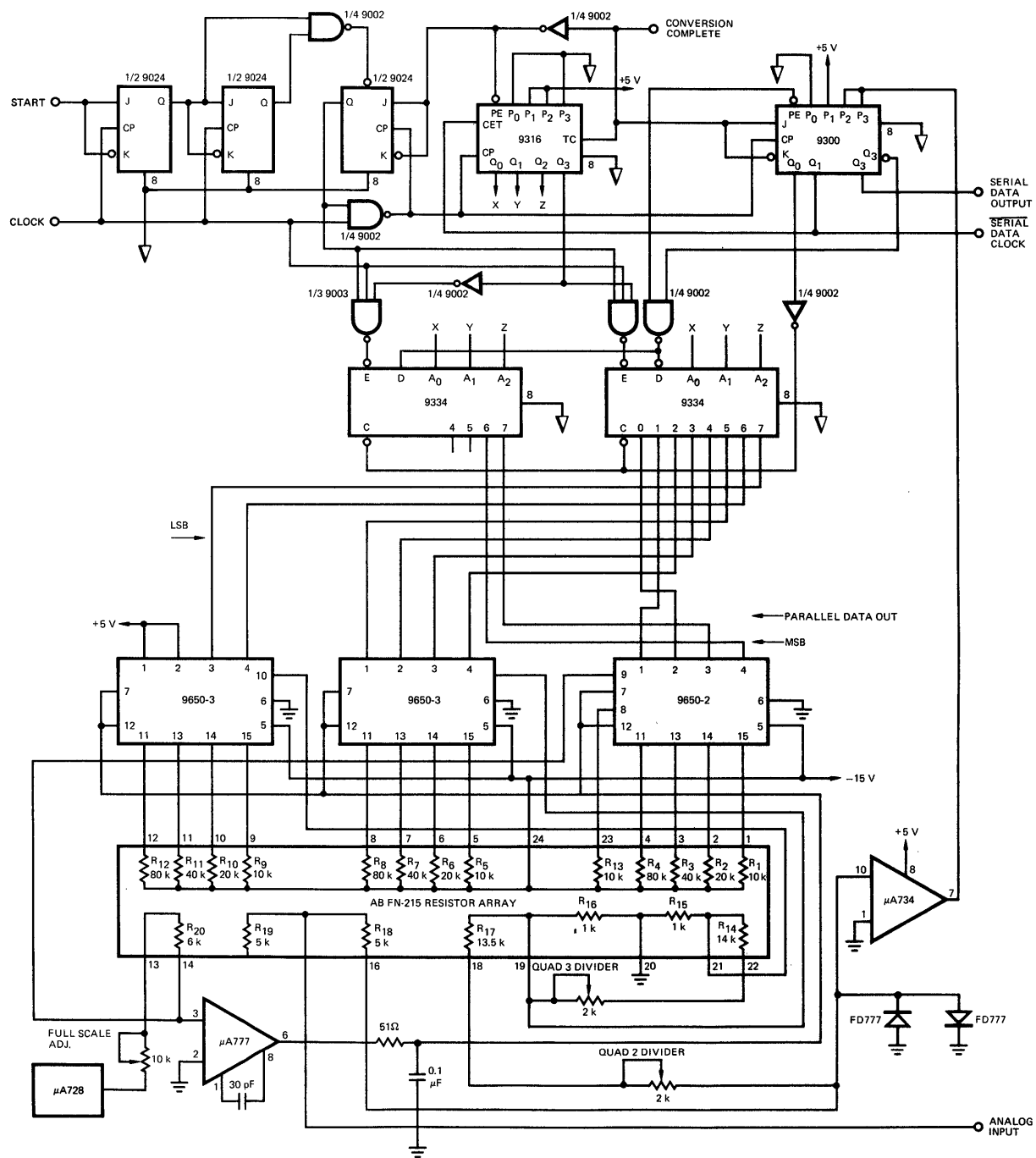


† For complete Applications data, please request our 9650 Applications Note.

NOTE: Digital gnd. indicated by ∇
 Analog gnd. indicated by \equiv

TYPICAL APPLICATIONS (cont'd)†

10-BIT A/D CONVERTER

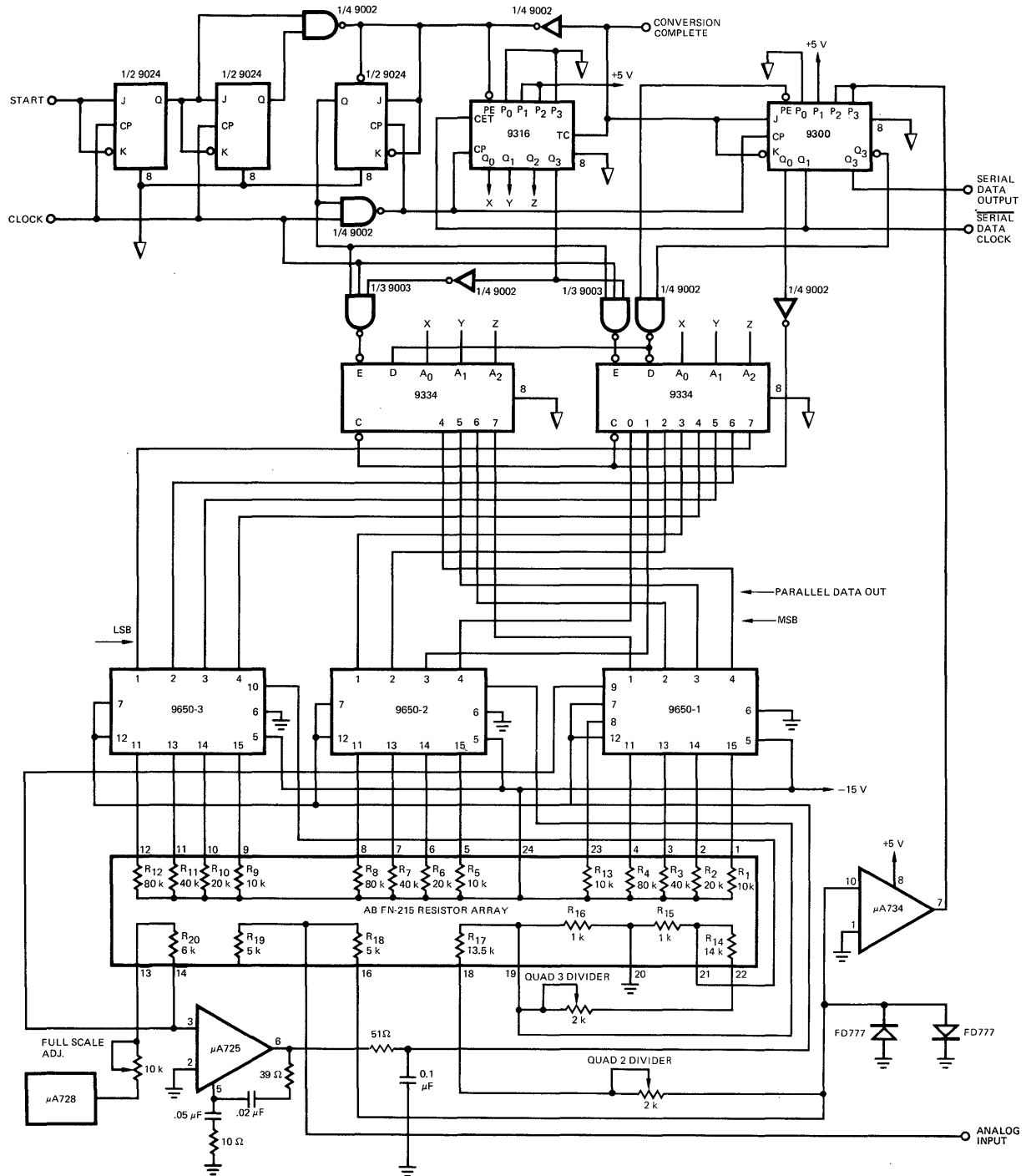


† For complete Applications data, please request our 9650 Applications Note.

NOTE: Digital gnd. indicated by ∇
 Analog gnd. indicated by \equiv

TYPICAL APPLICATIONS (cont'd)†

12-BIT A/D CONVERTER



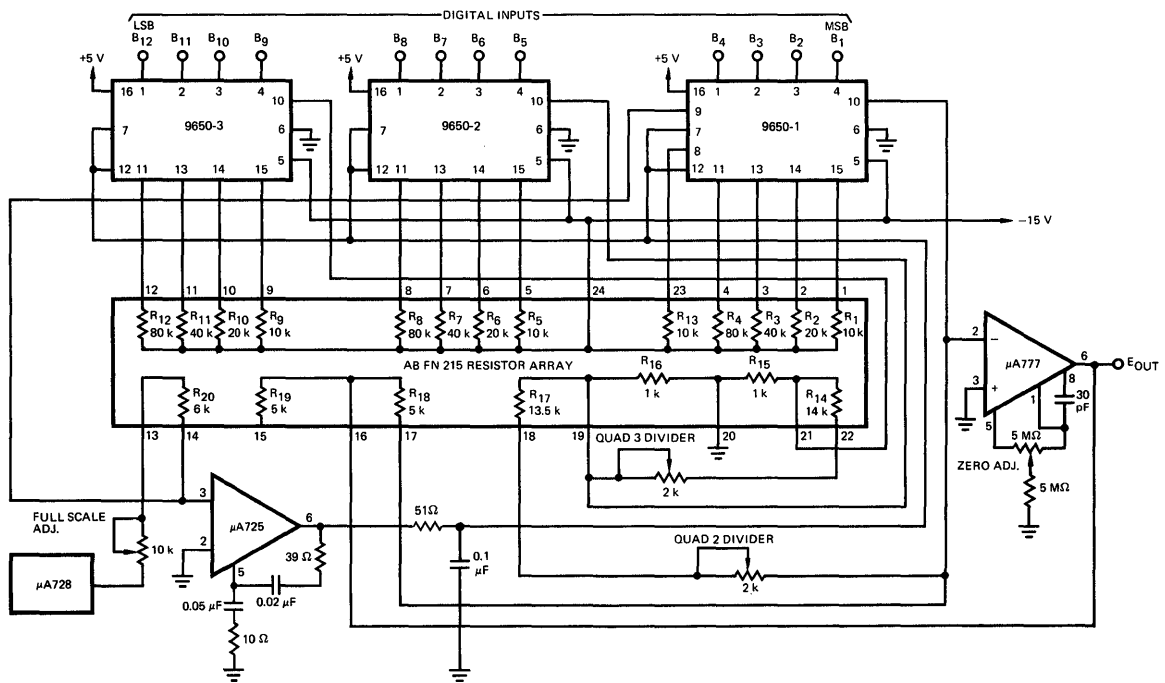
NOTE: Digital gnd. indicated by ∇

Analog gnd. indicated by \perp

† For complete Applications data, please request our 9650 Applications Note.

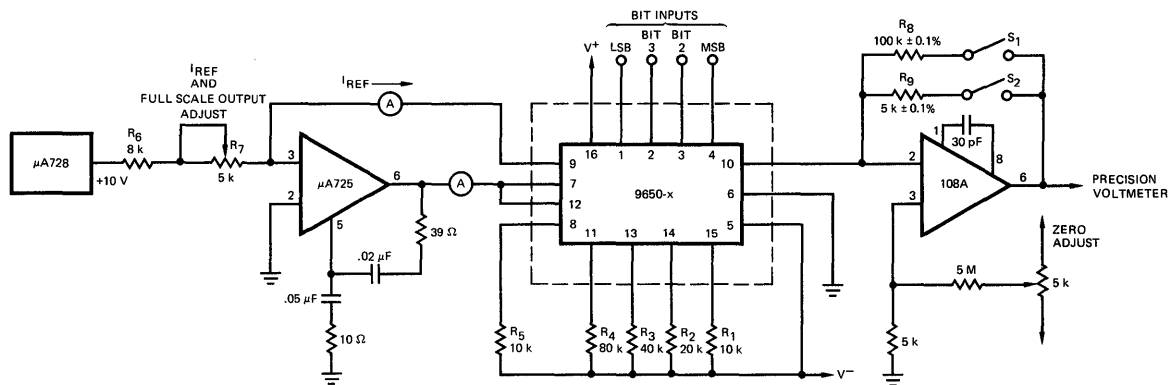
TYPICAL APPLICATIONS (cont'd)†

12-BIT D/A CONVERTER



† For complete Applications data, please request our 9650 Applications Note.

TYPICAL DC TEST CIRCUIT



NOTES:

- Required resistor ratio tolerances of R₁ - R₅ to test the various grades are as follows:
 9650A & 9650E, R₅ to R₂ to R₁ - ±0.005%, R₃ to R₁ - ±0.01%, R₄ to R₁ - ±0.02%.
 9650 & 9650C, R₅ to R₂ to R₁ - ±0.025%, R₃ to R₁ - ±0.05%, R₄ to R₁ - ±0.1%.
 9650B & 9650L, R₅ to R₂ to R₁ - ±0.1%, R₃ to R₁ - ±0.2%, R₄ to R₁ - ±0.4%.
- S₁ closed and S₂ open for output current (all Bits off) tests only.

55107A • 75107A • 55108A • 75108A

DUAL LINE RECEIVERS

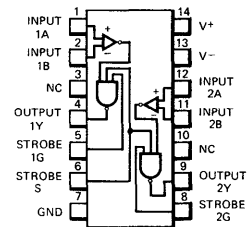
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55107A/75107A and 55108A/75108A are high speed, two-channel Line Receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is $\pm 3V$ but can be increased to $\pm 15V$ by the use of input attenuators. Separate or common strobes are available. The 55107A/75107A circuit features an active pull-up (totem pole output). The 55108A/75108A circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the 55109/75109 and 55110/75110 line drivers. The 55107A/75107A and 55108A/75108A line receivers are useful in high speed balanced, unbalanced and party line transmission systems and as data comparators.

- HIGH SPEED
- STANDARD SUPPLY VOLTAGES
- DUAL CHANNELS
- HIGH COMMON-MODE REJECTION RATIO
- HIGH INPUT IMPEDANCE
- HIGH INPUT SENSITIVITY
- INPUT COMMON-MODE VOLTAGE RANGE OF $\pm 3V$
- SEPARATE OR COMMON STROBES
- TTL OR DTL DRIVE CAPABILITY
- WIRED-OR OUTPUT CAPABILITY
- HIGH DC NOISE MARGINS
- STROBE INPUT CLAMP DIODES

CONNECTION DIAGRAM 14-LEAD DIP

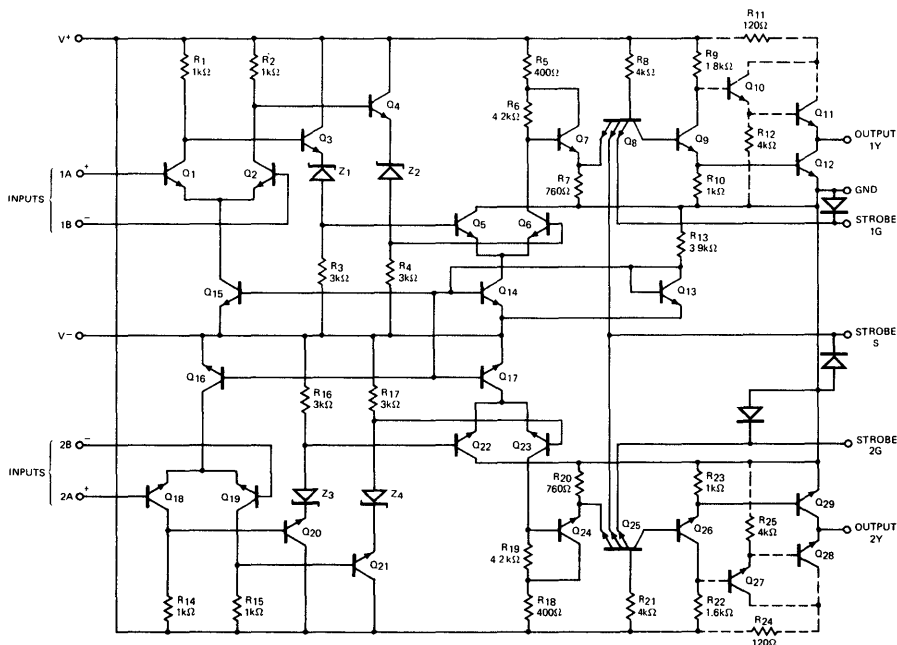
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
55107A	SN55107AJ
75107A	SN75107AJ
75107A	SN75107AN
55108A	SN55108AJ
75108A	SN75108AJ
75108A	SN75108AN

EQUIVALENT CIRCUIT



NOTE: Components shown with dashed lines are applicable to the 55107A and 75107A only.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 55107A • 75107A • 55108A • 75108A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	±7V
Internal Power Dissipation (Note 3)	670 mW
Differential Input Voltage (Note 2)	±6V
Common Mode Input Voltage (Note 1)	±5V
Strobe Input Voltage (Note 1)	5.5V
Operating Temperature Range	
55107A/108A	-55°C to +125°C
75107A/108A	0°C to +70°C
Storage Temperature Range	
Hermetic DIP (SN55/75107AJ, SN55/75108AJ)	-65°C to +150°C
Molded DIP (SN75107AN, SN75108AN)	-55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 Seconds) SN55/75107AJ, SN55/75108AJ	300°C
Molded DIP (Soldering, 10 Seconds) SN75107AN, SN75108AN	260°C

Notes on the following page

55107A • 75107A

ELECTRICAL CHARACTERISTICS [$+4.5\text{ V} \leq V_S \leq \pm 5.5\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted, (Note 4)]

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input HIGH Current	$V_{DIFF} = 0.5V, V_{CM} = -3V\text{ to }+3V$		30	75	μA
Input LOW Current	$V_{DIFF} = -2V, V_{CM} = -3V\text{ to }+3V$			-10	μA
Gate Input HIGH Current	$V_{GATE} = 2.4V$			40	μA
	$V_{GATE} = V^+$			1.0	mA
Gate Input LOW Current	$V_{GATE} = 0.4V$			-1.6	mA
Strobe Input HIGH Current	$V_{STROBE} = 2.4V$			80	μA
	$V_{STROBE} = V^+$			2.0	mA
Strobe Input LOW Current	$V_{STROBE} = 0.4V$			-3.2	mA
Output HIGH Voltage	$I_L = -400\mu A, V_{CM} = -3V\text{ to }+3V$	2.4			V
Output LOW Voltage	$I_{SINK} = 16mA, V_{CM} = -3V\text{ to }+3V$			0.4	V
Short-Circuit Output Current	$V_O = 0$ (Note 5)	-18		-70	mA
Positive Supply Current	$V_O = V_{OH}, I_L = 0, T_A = 25^\circ C$		18	30	mA
Negative Supply Current	$V_O = V_{OH}, I_L = 0, T_A = 25^\circ C$		-8.4	-15	mA

AC CHARACTERISTICS ($V^+ = +5V, V^- = -5V, R_L = 390\Omega, C_L = 50pF, T_A = 25^\circ C$ See Test Circuit)

t _{PLH} (D)			17	25	ns
t _{PHL} (D)			17	25	ns
t _{PLH} (S)			10	15	ns
t _{PHL} (S)			10	15	ns

55108A • 75108A

ELECTRICAL CHARACTERISTICS [$\pm 4.5\text{ V} \leq V_S \leq \pm 5.5\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted, (Note 4)]

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input HIGH Current	$V_{DIFF} = 0.5V, V_{CM} = -3V\text{ to }+3V$		30	75	μA
Input LOW Current	$V_{DIFF} = -2V, V_{CM} = -3V\text{ to }+3V$			-10	μA
Gate Input HIGH Current	$V_{GATE} = 2.4V$			40	μA
	$V_{GATE} = V^+$			1.0	mA
Gate Input LOW Current	$V_{GATE} = 0.4V$			-1.6	mA
Strobe Input HIGH Current	$V_{STROBE} = 2.4V$			80	μA
	$V_{STROBE} = V^+$			2.0	mA
Strobe Input LOW Current	$V_{STROBE} = 0.4V$			-3.2	mA
Output LOW Voltage	$I_{SINK} = 16mA, V_{CM} = -3V\text{ to }+3V$			0.4	V
Output HIGH Current	$V_{OUT} = V^+$			250	μA
Positive Supply Current	$V_O = V_{OH}, I_L = 0, T_A = 25^\circ C$		18	30	mA
Negative Supply Current	$V_O = V_{OH}, I_L = 0, T_A = 25^\circ C$		-8.4	-15	mA

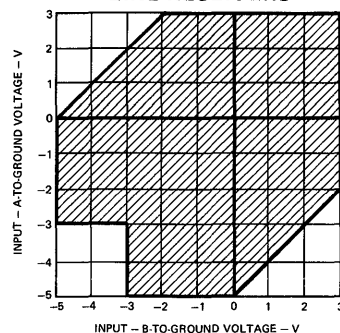
AC CHARACTERISTICS ($V^+ = +5V, V^- = -5V, R_L = 390\Omega, C_L = 15pF, T_A = 25^\circ C$ See Test Circuit)

t _{PLH} (D)			19	25	ns
t _{PHL} (D)			19	25	ns
t _{PLH} (S)			13	20	ns
t _{PHL} (S)			13	20	ns

TRUTH TABLE

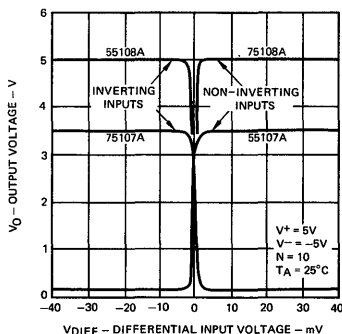
DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25 \text{ mV}$	L or H	L or H	H
$-25 \text{ mV} < V_{ID} < 25 \text{ mV}$	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25 \text{ mV}$	L or H	L	H
	L	L or H	H
	H	H	L

RECOMMENDED COMBINATIONS OF INPUT VOLTAGE FOR LINE RECEIVERS

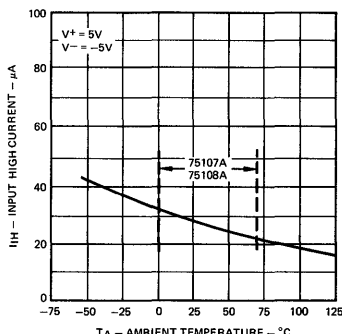


TYPICAL PERFORMANCE CURVES

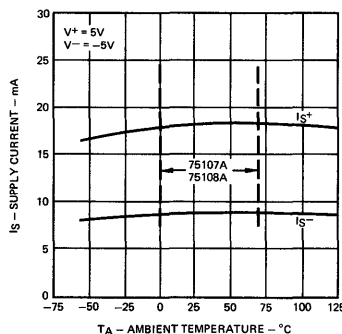
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



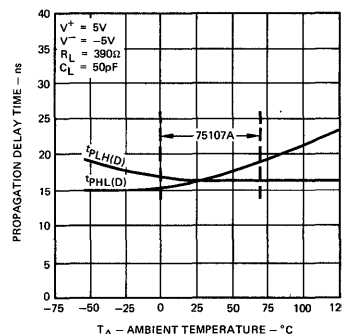
INPUT HIGH CURRENT INTO 1A OR 2A AS A FUNCTION OF AMBIENT TEMPERATURE



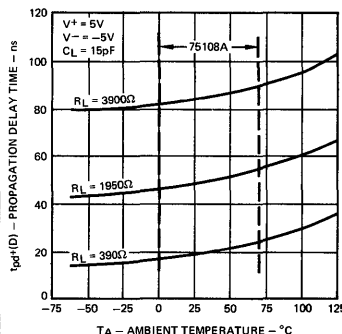
HIGH LOGIC LEVEL SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



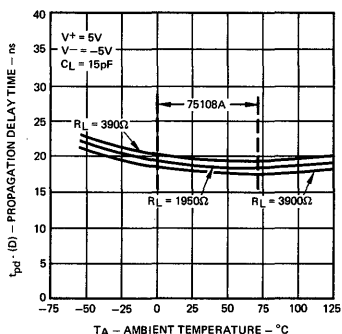
55107A, 75107A PROPAGATION DELAY TIME (DIFFERENTIAL INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



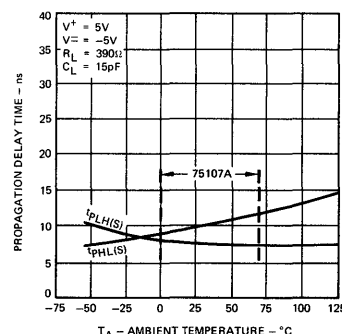
55108A, 75108A PROPAGATION DELAY TIME LOW-TO-HIGH LEVEL (DIFFERENTIAL INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



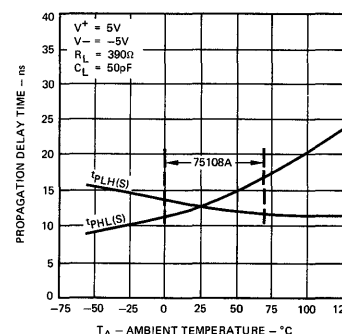
55108A, 75108A PROPAGATION DELAY TIME HIGH-TO-LOW LEVEL (DIFFERENTIAL INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



55107A, 75107A PROPAGATION DELAY TIME (STROBE INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



55108A, 75108A PROPAGATION DELAY TIME (STROBE INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE

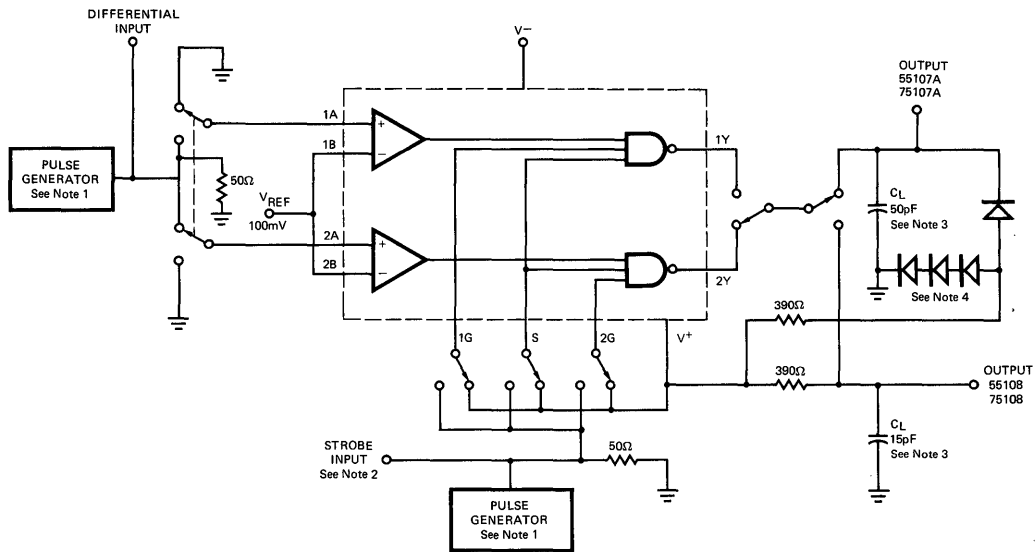


NOTES:

1. These voltages are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (-) terminal.
3. Rating applies to 70°C ambient temperature. Above 70°C derate at 8.3 mW/°C.
4. Specifications apply from 0°C to 70°C for 75107A and 75108A. Guaranteed supply voltage range is from ±4.75 V to ±5.25 V for 75107A and 75108A.
5. Note more than one (1) output should be shorted at a time.

SWITCHING CHARACTERISTICS

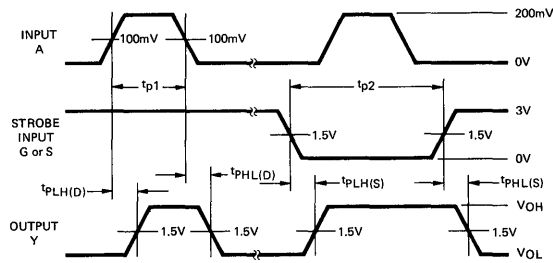
AC TEST CIRCUIT



NOTES:

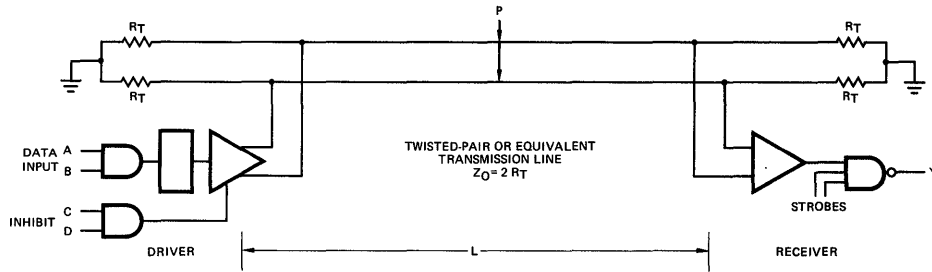
1. The pulse generators have the following characteristics: $Z_{out} = 50 \Omega$, $t_r = t_f = 10 \pm 5 \text{ ns}$, $t_{p1} = 500 \text{ ns}$, $PRR = 1 \text{ MHz}$, $t_{p2} = 1 \mu\text{s}$, $PRR = 500 \text{ kHz}$.
2. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

VOLTAGE WAVEFORMS



APPLICATION

BASIC BALANCED-LINE TRANSMISSION SYSTEM



The 55107A/75107A dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately $(30+1.3L)$ ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

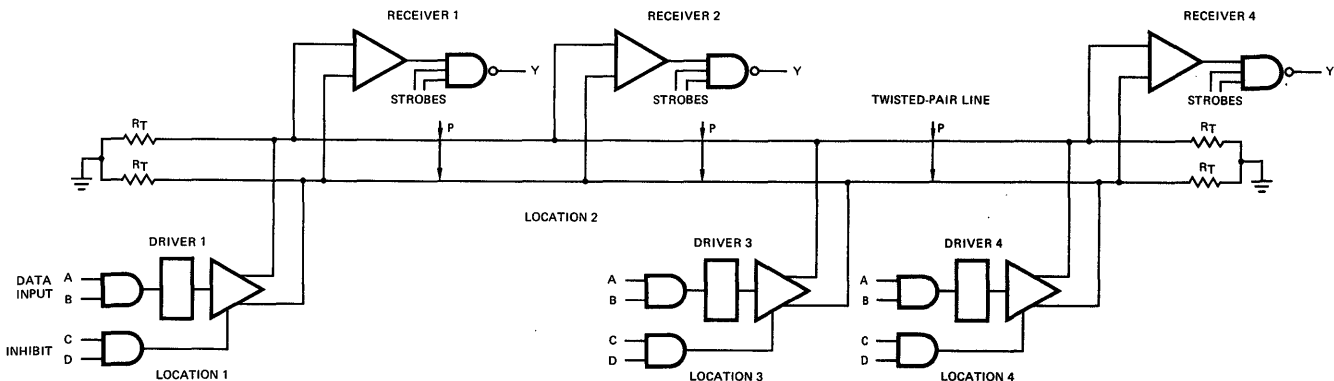
$$V_{DIFF} \approx 1/2 I_{O(on)} \cdot R_T$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

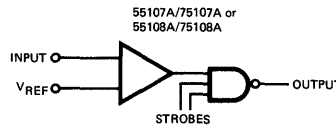
$$V_{DIFF} \approx I_{O(on)} \cdot R_T$$

DATA-BUS OR PARTY-LINE SYSTEM



The strobe feature of the receivers and the inhibit feature of the drivers allow the 55107A/75107A dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The 55107A/75107A device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

APPLICATION (Cont'd)
UNBALANCED OR SINGLE-LINE SYSTEMS



The 55107A/75107A dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

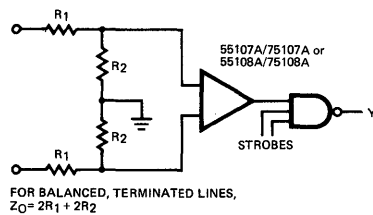
The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of -3.0 V to $+3.0$ V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

PRECAUTIONS IN THE USE OF 55/75107A AND 55/75108A DUAL LINE RECEIVERS

The following precaution should be observed when using or testing 55107A/75107A line circuits:

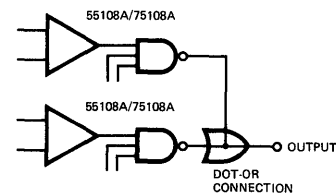
When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between -3.0 V and $+3.0$ V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

INCREASING COMMON-MODE INPUT VOLTAGE RANGE OF RECEIVER



The 55107A/75107A and 55108A/75108A line receivers feature a common-mode input voltage range of ± 3.0 V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common-mode range can be extended by the use of external input attenuators. Common-mode input voltages can in this way be reduced to ± 3.0 V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

55108A/75108A DOT-OR OUTPUT CONNECTIONS



The 55108A/75108A line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other 55108A/75108A outputs. This allows a level of logic to be implemented without additional logic delay.

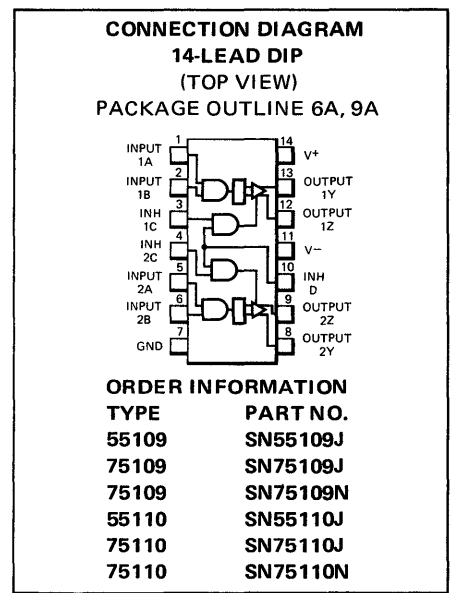
55109 • 75109 • 55110 • 75110

DUAL LINE DRIVERS

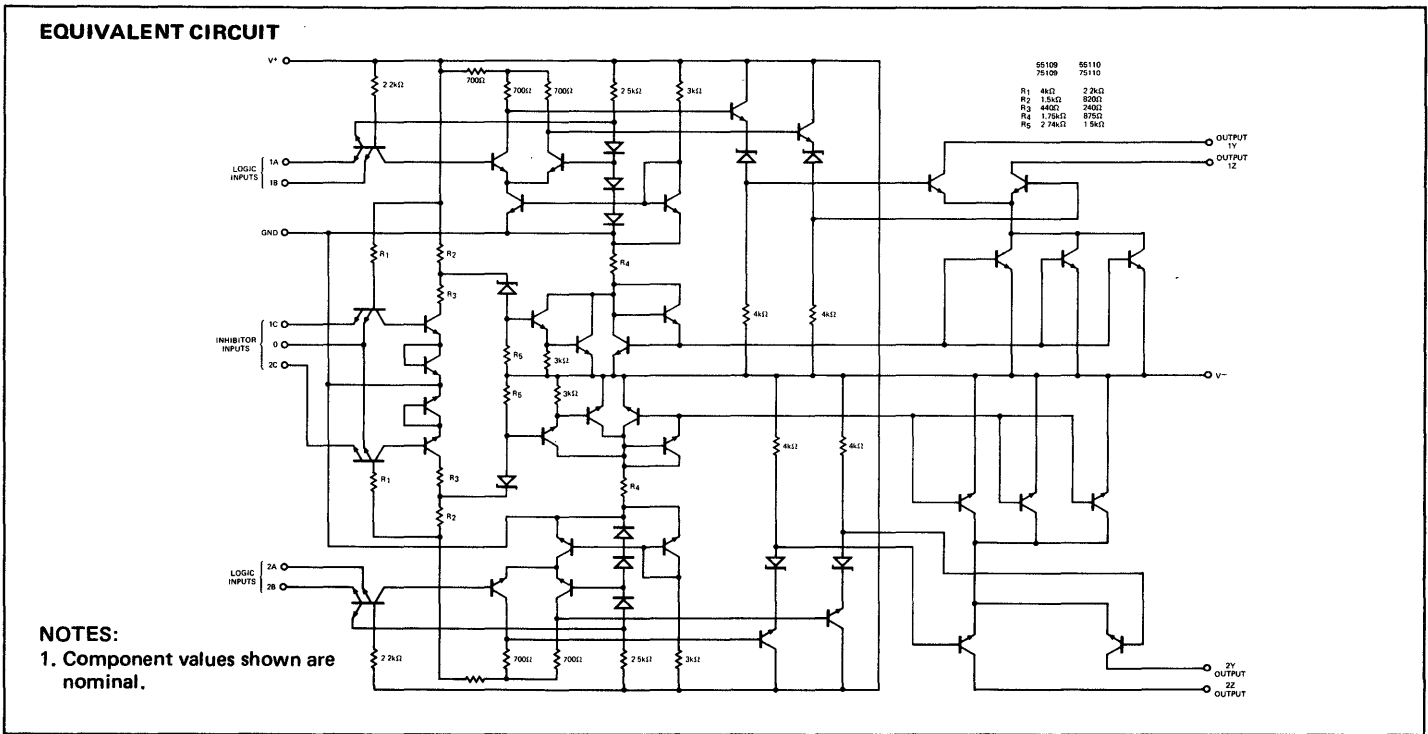
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55109/75109 and 55110/75110 are Dual Line Drivers featuring independent channels with common supply voltage and ground terminals. The major difference between the 55109/75109 and the 55110/75110 drivers is the output-current specification. The output current is nominally 6 mA for the 55109/75109 and 12 mA for the 55110/75110. The driver circuits have a constant output that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off by appropriate logic levels at the inhibit inputs. The circuit also features an inhibit input that is common to both drivers, providing more circuit versatility. The common-mode voltage range of the driver outputs is -3.0 V to $+10\text{ V}$, which allows a common-mode voltage on the line without affecting the driver performance. For application information see 55107A • 75107A • 55108A • 75108A data sheet.

- HIGH SPEED
- STANDARD SUPPLY VOLTAGES
- DUAL CHANNELS
- TTL INPUT COMPATIBILITY
- CURRENT-MODE OUTPUT (6mA or 12mA TYPICAL)
- HIGH OUTPUT IMPEDANCE
- HIGH COMMON-MODE OUTPUT VOLTAGE RANGE (-3V to 10V)
- INHIBITOR AVAILABLE FOR DRIVER SELECTION



6



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V ₊ (See Note 1)	7 V
Supply Voltage V ₋ (See Note 1)	-7 V
Logic and Inhibitor Input Voltages (See Note 1)	5.5 V
Common-Mode Output Voltage (See Note 1)	-5 to 12 V
Operating Free-Air Temperature Range	
55109/55110	-55°C to +125°C
75109/75110	0°C to +70°C
Storage Temperature Range	
Hermetic DIP (SN55/75109J, SN55/75110J)	-65°C to +150°C
Molded DIP (SN75109N, SN75110N)	-55°C to +125°C
Lead Temperature	
Hermetic DIP (soldering, 60 seconds)	300°C
Molded DIP (soldering, 10 seconds)	260°C

Notes on the following pages.

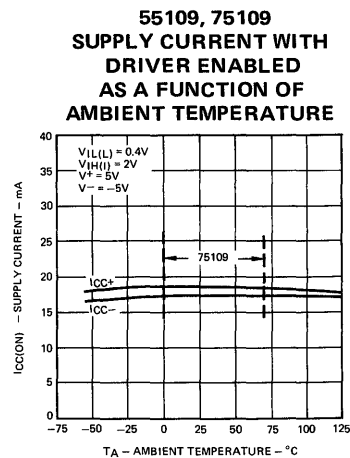
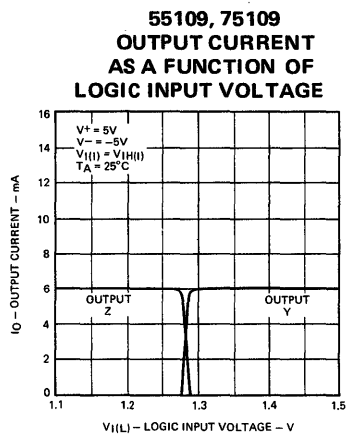
55109 • 75109

ELECTRICAL CHARACTERISTICS [$\pm 4.5 \text{ V} \leq V_S \leq \pm 5.5 \text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, (Note 2) V₊ = Max., V₋ = Max. unless otherwise specified]

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input HIGH Current	V _{IN} = 2.4 V			40	μA
	V _{IN} = MAX. V ₊			1.0	mA
Input LOW Current	V _{IN} = 0.4 V			-3.0	mA
Inhibit Input HIGH Current	V _{INHIBIT} = 2.4 V			40	μA
	V _{INHIBIT} = MAX. V ₊			1.0	mA
Inhibit Input LOW Current	V _{INHIBIT} = 0.4 V			-3.0	mA
Common-Inhibit HIGH Current	V _{INHIBIT} = 2.4 V			80	μA
	V _{INHIBIT} = MAX. V ₊			2.0	mA
Common-Inhibit LOW Current	V _{INHIBIT} = 0.4 V			-6.0	mA
ON-STATE Output Current	V ₊ = MAX., V ₋ = MAX.			7.0	mA
	V ₊ = MIN., V ₋ = MAX.	3.5			mA
OFF-STATE Output Current	V ₊ = MIN., V ₋ = MIN.			100	μA
I _{CC} + (ON) Supply Current with Driver Enabled	V _{IN} = 0.4 V, V _{INHIBIT} = 2.0 V		18	30	mA
I _{CC} - (ON) Supply Current with Driver Enabled	V _{IN} = 0.4 V, V _{INHIBIT} = 2.0 V		-18	-30	mA
I _{CC} + (OFF) Supply Current with Driver Inhibited	V _{IN} = 0.4 V, V _{INHIBIT} = 0.4 V		18		mA
I _{CC} - (OFF) Supply Current with Driver Inhibited	V _{IN} = 0.4 V, V _{INHIBIT} = 0.4 V		-10		mA

AC CHARACTERISTICS [V₊ = 5 V, V₋ = -5 V, T_A = 25°C (See Test Circuit)]

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
t _{PLH} (L)	Propagation Delay Time (Logic Inputs)		9.0	15	ns
t _{PHL} (L)	Propagation Delay Time (Logic Inputs)		9.0	15	ns
t _{PLH} (I)	Propagation Delay Time (Inhibitor Inputs)		16	25	ns
t _{PHL} (I)	Propagation Delay Time (Inhibitor Inputs)		13	25	ns



RECOMMENDED OPERATING CONDITIONS (Note 3)

	55109 55110			75109 75110			UNIT
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
V+ Positive Supply Voltage (Note 1)	4.5	5.0	5.5	4.75	5.0	5.25	V
V- Negative Supply Voltage (Note 1)	-5.5	-5.0	-4.5	-5.25	-5.0	-4.75	V
Positive Common Mode Output Voltage (Note 1)	0		10	0		10	V
Negative Common Mode Output Voltage (Note 1)	-3.0		0	-3.0		0	V

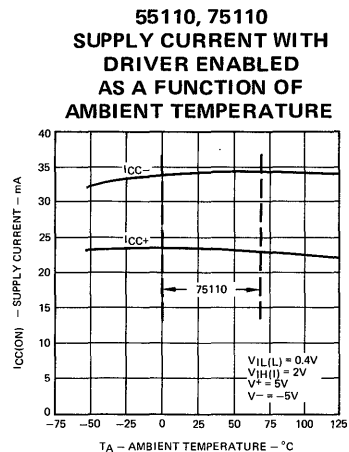
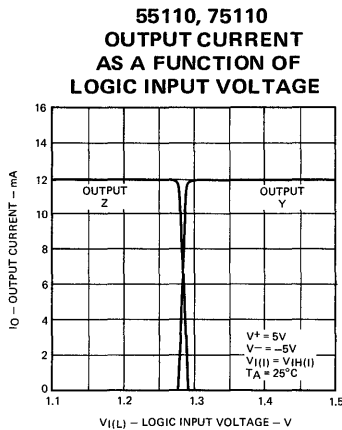
55110 • 75110

ELECTRICAL CHARACTERISTICS [$\pm 4.5\text{ V} \leq V_S \leq \pm 5.5\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, (Note 2) V+ = Max., V- = Max. unless otherwise specified]

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input HIGH Current	V _{IN} = 2.4 V			40	μA
	V _{IN} = Max. V+			1.0	mA
Input LOW Current	V _{IN} = 0.4 V			-3.0	mA
	V _{INHIBIT} = 2.4 V			40	μA
Inhibit Input HIGH Current	V _{INHIBIT} = Max. V+			1.0	mA
	V _{INHIBIT} = 0.4 V			-3.0	mA
Common-Inhibit Input HIGH Current	V _{INHIBIT} = 2.4 V			80	μA
	V _{INHIBIT} = Max. V+			2.0	mA
Common-Inhibit Input LOW Current	V _{INHIBIT} = 0.4 V			-6.0	mA
	V+ = Max., V- = Max			15	mA
ON-STATE Output Current	V+ = Min., V- = Max.	6.5			mA
	V+ = Min., V- = Min.			100	μA
I _{CC+} (ON) Supply Current with Driver Enabled	V _{IN} = 0.4 V, V _{INHIBIT} = 2.0 V		23	35	mA
I _{CC-} (ON) Supply Current with Driver Enabled	V _{IN} = 0.4 V, V _{INHIBIT} = 2.0 V		-34	-50	mA
I _{CC+} (OFF) Supply Current with Driver Inhibited	V _{IN} = 0.4 V, V _{INHIBIT} = 0.4 V		21		mA
I _{CC-} (OFF) Supply Current with Driver Inhibited	V _{IN} = 0.4 V, V _{INHIBIT} = 0.4 V		-17		mA

AC CHARACTERISTICS [V+ = 5 V, V- = -5 V, T_A = 25°C (See Test Circuit)]

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
t _{PLH} (L)	Propagation Delay Time (Logic Inputs)		9.0	15	ns
t _{PHL} (L)	Propagation Delay Time (Logic Inputs)		9.0	15	ns
t _{PLH} (I)	Propagation Delay Time (Inhibitor Inputs)		16	25	ns
t _{PHL} (I)	Propagation Delay Time (Inhibitor Inputs)		13	25	ns

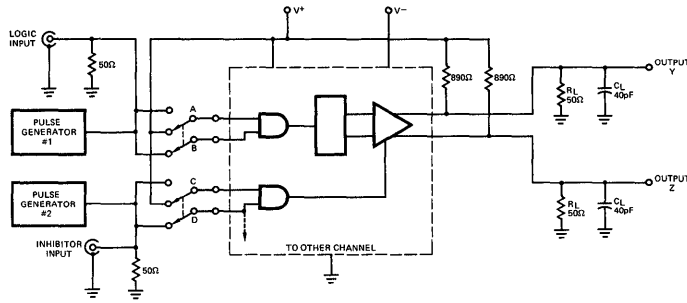


NOTES:

- These voltage values are with respect to the network ground terminal.
- Specifications apply from 0°C to +70°C for the 75109 and 75110. Guaranteed supply voltage range is $\pm 4.75\text{ V}$ to $\pm 5.25\text{ V}$ for the 75109 and 75110.
- When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

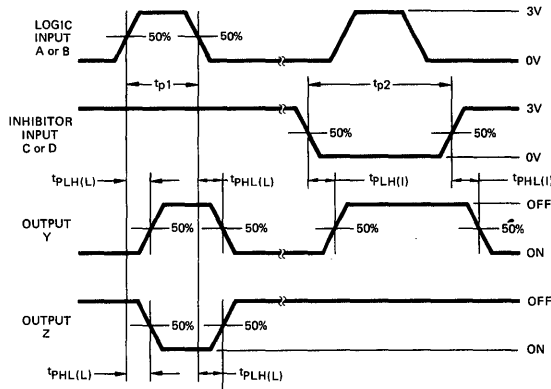
SWITCHING CHARACTERISTICS

TEST CIRCUIT



- NOTES: 1. The pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 10 \pm 5ns$, $t_{p1} = 500ns$, $PRR = 1MHz$, $t_{p2} = 1\mu s$, $PRR = 500kHz$.
 2. C_L includes probe and jig capacitance.
 3. For simplicity, only one channel and the inhibitor connections are shown.

VOLTAGE WAVEFORMS

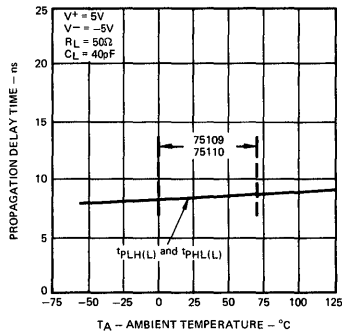


TRUTH TABLE

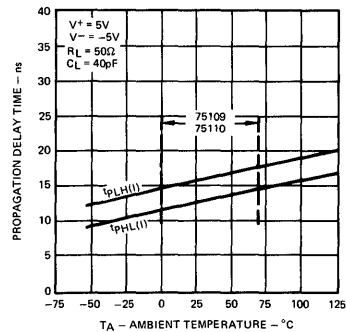
Logic Inputs		Inhibit Inputs		Outputs		
A	B	C	D	Y	Z	
X	X	L	X	OFF	OFF	INHIBITED
X	X	X	L	OFF	OFF	INHIBITED
L	X	H	H	ON	OFF	
X	L	H	H	ON	OFF	
H	H	H	H	OFF	ON	

H = HIGH Input $\geq V_{IH} \geq 2.0$ Volts
 L = LOW Input $\leq V_{IL} \leq 0.8$ Volts
 X = Either HIGH or LOW
 OFF = Output Transistor is OFF
 ON = Output Transistor is ON

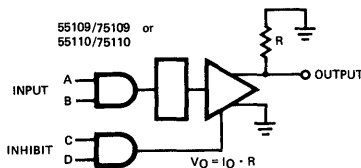
PROPAGATION DELAY TIME (LOGIC INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



PROPAGATION DELAY TIME (INHIBITOR INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



APPLICATIONS



A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and cross-talk problems. For large signal swings, the high output current (12 mA) of the 55110/75110 is recommended. Drivers may be paralleled for higher current. The unused driver output must be tied to ground. The following precaution should be observed when using or testing 55/75109 and 55/75110 dual line drivers.

When only one driver in a package is being used, the outputs of the other driver must either be grounded or inhibited in order to prevent excess power dissipation.

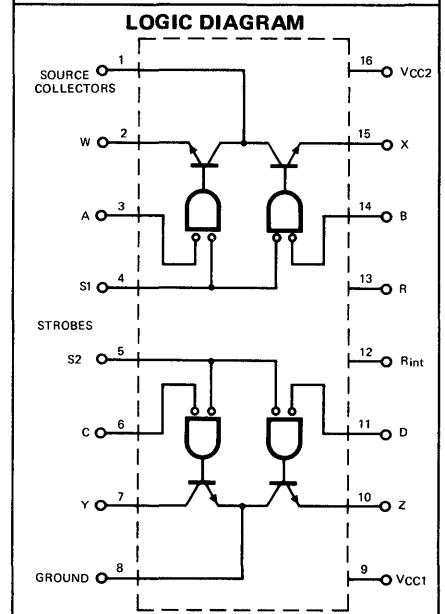
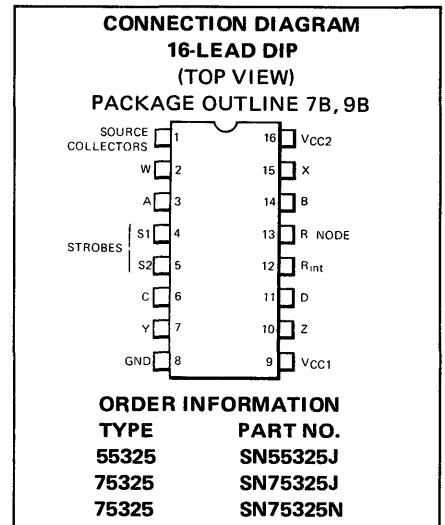
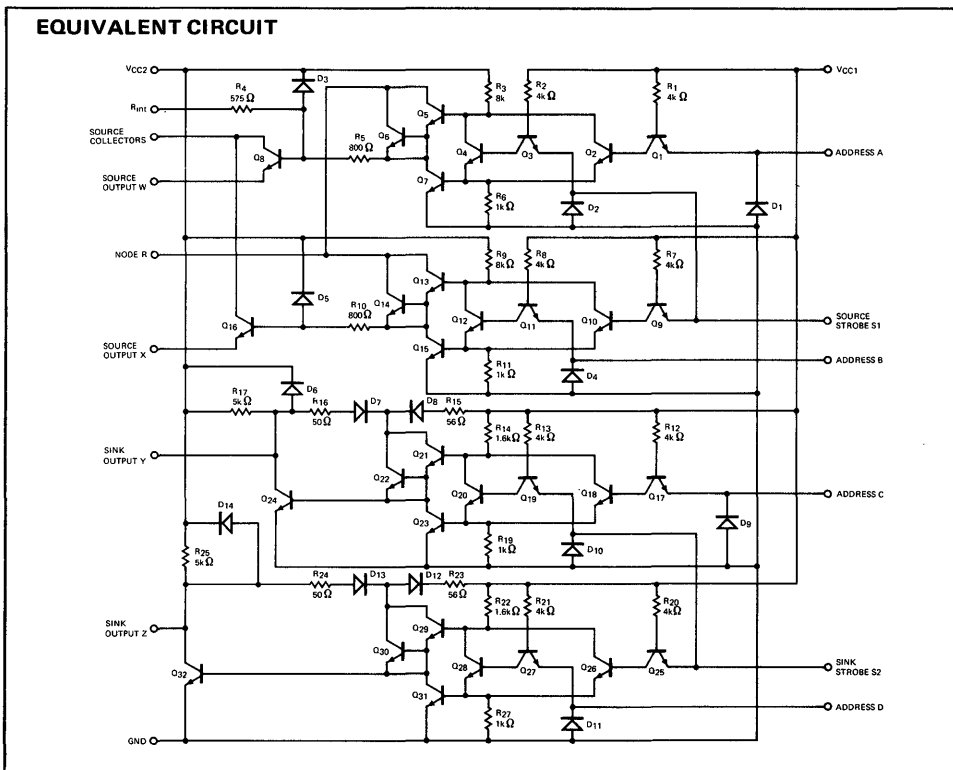
55325/75325 MEMORY DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The 55325 and 75325 are Memory Drivers for use in magnetic memories constructed on a silicon chip using the Fairchild Planar* process. The device contains four 600 mA switches, two source switches and two sink switches that can be selected by the appropriate logic input and appropriate strobe. The device has adequate base drive to source currents up to 375 mA with V_{CC2} of 15 V or 600 mA with V_{CC2} voltage of 24 V. In applications requiring drive to source currents greater than 375 mA, an external resistor may be used to regulate the source base current to within $\pm 5\%$ and reduce the power dissipation to allow higher source currents at higher ambient temperatures.

Internal voltage surge protection of each of the output sink transistors is provided for switching inductive loads.

- 600 mA OUTPUT CAPABILITY
- FAST SWITCH TIMES
- OUTPUT SHORT-CIRCUIT CURRENT
- DUAL SINK AND DUAL SOURCE OUTPUTS
- MINIMUM TIME SKEW BETWEEN ADDRESS AND OUTPUT CURRENT RISE
- 24 V CAPABILITY
- TTL OR DTL COMPATIBLE
- SOURCE BASE DRIVE EXTERNALLY ADJUSTABLE
- INPUT CLAMP DIODES



POSITIVE LOGIC TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS (Note 3)			
SOURCE	SINK	SOURCE	SINK	SOURCE	SINK	W	X	Y	Z
A	B	C	D	S1	S2				
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	H	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = HIGH level, L = LOW level, X = irrelevant

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 55325 • 75325

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC1} (Note 1)	7.0 V
Supply Voltage V_{CC2} (Note 2)	25 V
Input Voltage (Any Address or Strobe Input)	5.5 V
Storage Temperature Range	
Hermetic DIP (SN55325J, SN75325J)	-65°C to +150°C
Molded DIP (SN75325N)	-55°C to +125°C
Operating Temperature Range	
Hermetic DIP	
Military (SN55325J)	-55°C to +125°C
Commercial (SN75325J)	0°C to + 70°C
Molded DIP (SN75325N)	0°C to + 70°C
Internal Power Dissipation (Note 2)	800 mW
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C

55325

ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C unless otherwise specified, T_A = 25°C for typical values)

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input HIGH Voltage	V_{IH}	Fig. 1 & 2		2.0			V
Input LOW Voltage	V_{IL}	Fig. 3 & 4				0.8	V
Input Clamp Diode Voltage	V_{CD}	$V_{CC1} = 4.5\text{ V}, V_{CC2} = 24\text{ V}$ $I_{IN} = -10\text{ mA}, T_A = 25^\circ\text{C}$ Fig. 5		-1.3		-1.7	V
Source-collectors Terminal Off-state Current	I_{OFF}	$V_{CC1} = 4.5\text{ V}, V_{CC2} = 24\text{ V}$ Fig. 1	Full Range			500	μA
			$T_A = 25^\circ\text{C}$	3.0	150	μA	
Sink Output HIGH Voltage	V_{OH}	$V_{CC1} = 4.5\text{ V}, V_{CC2} = 24\text{ V}$ $I_O = 0$, Fig. 2		19		23	V
Saturation Voltage	Source Outputs	V_{sat}	$V_{CC1} = 4.5\text{ V}, V_{CC2} = 15\text{ V}$ $R_L = 24\Omega, I_{source} \approx -600\text{ mA}$ See Note 3, 4 & Fig. 4	Full Range		0.9	V
				$T_A = 25^\circ\text{C}$	0.43	0.7	V
	Sink Outputs		$V_{CC1} = 4.5\text{ V}, V_{CC2} = 15\text{ V}$ $R_L = 24\Omega, I_{sink} \approx 600\text{ mA}$ See Note 3, 4 & Fig. 3	Full Range		0.9	V
				$T_A = 25^\circ\text{C}$	0.43	0.7	V
Input Current at Maximum Input Voltage	Address Inputs	I_{IN}	$V_{CC1} = 5.5\text{ V}, V_{CC2} = 24\text{ V}$ $V_{IN} = 5.5\text{ V}$, Fig. 5			1.0	mA
	Strobe Inputs					2.0	mA
Input HIGH Current	Address Inputs	I_{IH}	$V_{CC1} = 5.5\text{ V}, V_{CC2} = 24\text{ V}$ $V_{IN} = 2.4\text{ V}$, Fig. 5		3.0	40	μA
	Strobe Inputs				6.0	80	μA
Input LOW Current	Address Inputs	I_{IL}	$V_{CC1} = 5.5\text{ V}, V_{CC2} = 24\text{ V}$ $V_{IN} = 0.4\text{ V}$, Fig. 5		-1.0	-1.6	mA
	Strobe Inputs				-2.0	-3.2	mA
Supply Current, All Sources and Sinks Off	From V_{CC1}	$I_{CC(off)}$	$V_{CC1} = 5.5\text{ V}, V_{CC2} = 24\text{ V}$ $T_A = 25^\circ\text{C}$, Fig. 6		14	22	mA
	From V_{CC2}				7.5	20	mA
Supply Current from V_{CC1} , Either Sink On	I_{CC1}	$V_{CC1} = 5.5\text{ V}, V_{CC2} = 24\text{ V}$ $I_{sink} = 50\text{ mA}, T_A = 25^\circ\text{C}$ Fig. 7		55	70	mA	
Supply Current from V_{CC2} , Either Source On	I_{CC2}	$V_{CC1} = 5.5\text{ V}, V_{CC2} = 24\text{ V}$ $I_{source} = -50\text{ mA}, T_A = 25^\circ\text{C}$ Fig. 8		32	50	mA	

NOTES:

1. Voltage values are with respect to network ground terminal.
2. For operation of 55325 above 70°C free air temperature, refer to Dissipation Derating Curve, Figure 13.
3. Not more than one output is to be on at any one time.
4. Parameters measured using the following pulse techniques; $t_W = 200\ \mu\text{s}$, duty cycle ≤ 2%.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 55325 • 75325

75325

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$ for typical values unless otherwise specified)

PARAMETER		CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input HIGH Voltage		V_{IH}	Fig. 1 & 2	2.0			V
Input LOW Voltage		V_{IL}	Fig. 3 & 4			0.8	V
Input Clamp Diode Voltage		V_{CD}	$V_{CC1} = 4.5\text{ V}$, $V_{CC2} = 24\text{ V}$ $I_{IN} = -10\text{ mA}$, $T_A = 25^{\circ}\text{C}$ Fig. 5	-1.3	-1.7		V
Source-collectors Terminal Off-State Current		I_{OFF}	$V_{CC1} = 4.5\text{ V}$, $V_{CC2} = 24\text{ V}$ Fig. 1	Full Range	200		μA
				$T_A = 25^{\circ}\text{C}$	3.0	200	μA
Sink Output HIGH Voltage		V_{OH}	$V_{CC1} = 4.5\text{ V}$, $V_{CC2} = 24\text{ V}$ $I_O = 0$, Fig. 2	19	23		V
Saturation Voltage	Source Outputs	V_{sat}	$V_{CC1} = 4.5\text{ V}$, $V_{CC2} = 15\text{ V}$ $R_L = 24\Omega$, $I_{source} \approx -600\text{ mA}$ See Note 4 & Fig. 3	Full Range	0.9		V
				$T_A = 25^{\circ}\text{C}$	0.43	0.75	V
	Sink Outputs			Full Range	0.9		V
				$T_A = 25^{\circ}\text{C}$	0.75		
Input Current at Maximum Input Voltage	Address Inputs	I_{IN}	$V_{CC1} = 5.5\text{ V}$, $V_{CC2} = 24\text{ V}$ $V_{IN} = 5.5\text{ V}$, Fig. 5		1.0		mA
	Strobe Inputs				2.0		mA
Input HIGH Current	Address Inputs	I_{IH}	$V_{CC1} = 5.5\text{ V}$, $V_{CC2} = 24\text{ V}$ $V_{IN} = 2.4\text{ V}$, Fig. 5		3.0	40	μA
	Strobe Inputs				6.0	80	μA
Input LOW Current	Address Inputs	I_{IL}	$V_{CC1} = 5.5\text{ V}$, $V_{CC2} = 24\text{ V}$ $V_{IN} = 0.4\text{ V}$, Fig. 5		-1.0	-1.6	mA
	Strobe Inputs				-2.0	-3.2	mA
Supply Current, All Sources and Sinks Off	From V_{CC1}	$I_{CC(off)}$	$V_{CC1} = 5.5\text{ V}$, $V_{CC2} = 24\text{ V}$ $T_A = 25^{\circ}\text{C}$, Fig. 6		14	22	mA
	From V_{CC2}				7.5	20	mA
Supply Current from V_{CC1} , Either Sink On		I_{CC1}	$V_{CC1} = 5.5\text{ V}$, $V_{CC2} = 24\text{ V}$ $I_{sink} = 50\text{ mA}$, $T_A = 25^{\circ}\text{C}$ Fig. 7		55	70	mA
Supply Current from V_{CC2} , Either Source On		I_{CC2}	$V_{CC1} = 5.5\text{ V}$, $V_{CC2} = 24\text{ V}$ $I_{source} = -50\text{ mA}$, $T_A = 25^{\circ}\text{C}$ Fig. 8		32	50	mA

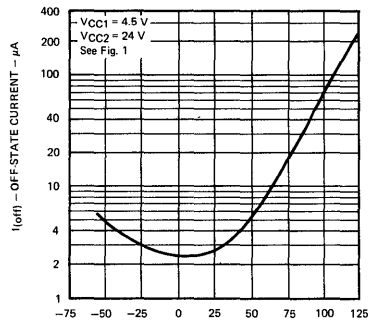
55325 • 75325

SWITCHING CHARACTERISTICS ($V_{CC1} = 5.0\text{ V}$, $T_A = 25^{\circ}\text{C}$, See Test Circuit Figures 9 and 10)

PARAMETER		TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNITS
t_{PLH}	Propagation Delay Time to Source Collectors	9	$V_{CC2} = 15\text{ V}$, $R_L = 24\Omega$ $C_L = 25\text{ pF}$		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Transition Time to Source Outputs	10	$V_{CC2} = 20\text{ V}$, $R_L = 1\text{ k}\Omega$ $C_L = 25\text{ pF}$		55		ns
t_{THL}					7.0		
t_{PLH}	Propagation Delay Time to Sink Outputs	9	$V_{CC2} = 15\text{ V}$, $R_L = 24\Omega$ $C_L = 25\text{ pF}$		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Transition Time to Sink Outputs	9	$V_{CC2} = 15\text{ V}$, $R_L = 24\Omega$ $C_L = 25\text{ pF}$		7.0	15	ns
t_{THL}					9.0	20	
t_s	Storage Time to Sink Outputs	9	$V_{CC2} = 15\text{ V}$, $R_L = 24\Omega$ $C_L = 25\text{ pF}$		15	30	ns

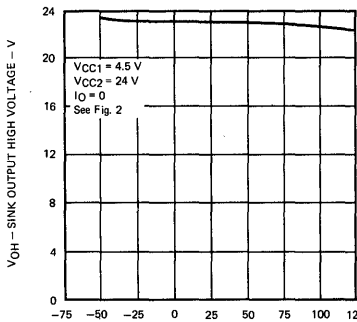
TYPICAL PERFORMANCE CURVES

OFF-STATE CURRENT INTO SOURCE COLLECTORS AS A FUNCTION OF AMBIENT TEMPERATURE



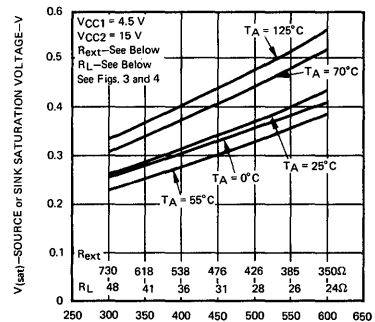
TA - AMBIENT TEMPERATURE - °C

SINK OUTPUT HIGH VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



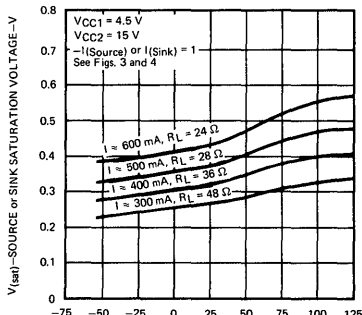
TA - AMBIENT TEMPERATURE - °C

SOURCE OR SINK SATURATION VOLTAGE AS A FUNCTION OF SOURCE CURRENT OR SINK CURRENT



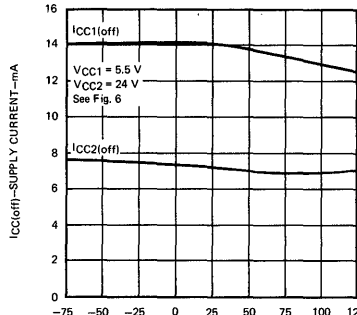
-I(source) or I(sink) - SOURCE CURRENT or SINK CURRENT - mA

SOURCE OR SINK SATURATION VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



TA - AMBIENT TEMPERATURE - °C

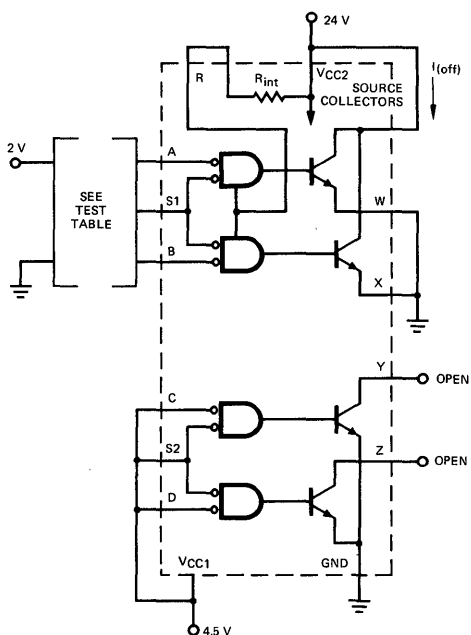
SUPPLY CURRENT, ALL SOURCES AND SINKS OFF AS A FUNCTION OF AMBIENT TEMPERATURE



TA - AMBIENT TEMPERATURE - °C

PARAMETER MEASUREMENT INFORMATION

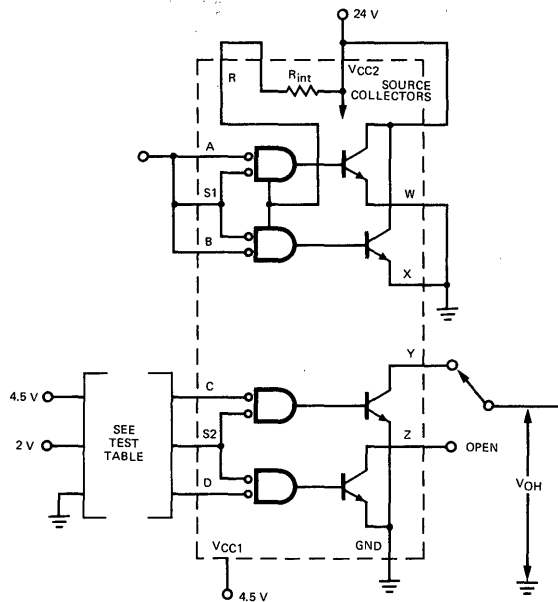
DC TEST CIRCUITS†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

Fig. 1 I(OFF) AND VIH



TEST TABLE

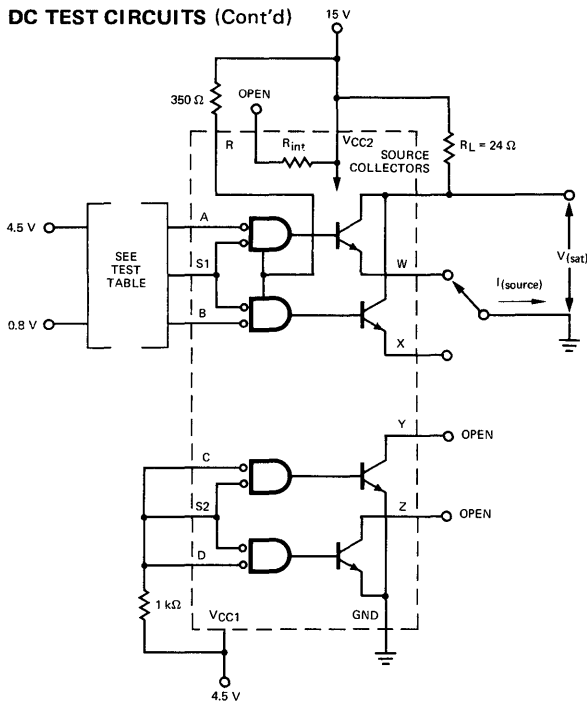
C	D	S2	Y	Z
2 V	4.5 V	GND	VOH	OPEN
GND	4.5 V	2 V	VOH	OPEN
4.5 V	2 V	GND	OPEN	VOH
4.5 V	GND	2 V	OPEN	VOH

Fig. 2 VIH AND VOH

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

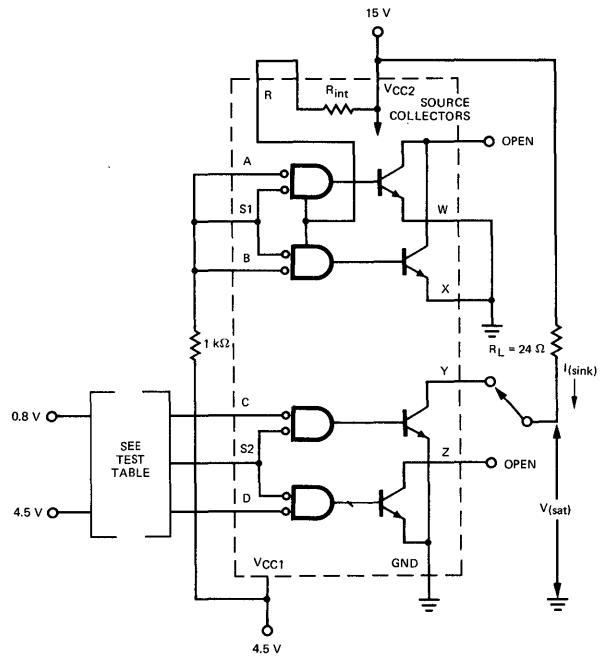
DC TEST CIRCUITS (Cont'd)



TEST TABLE

A	B	S1	W	X
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

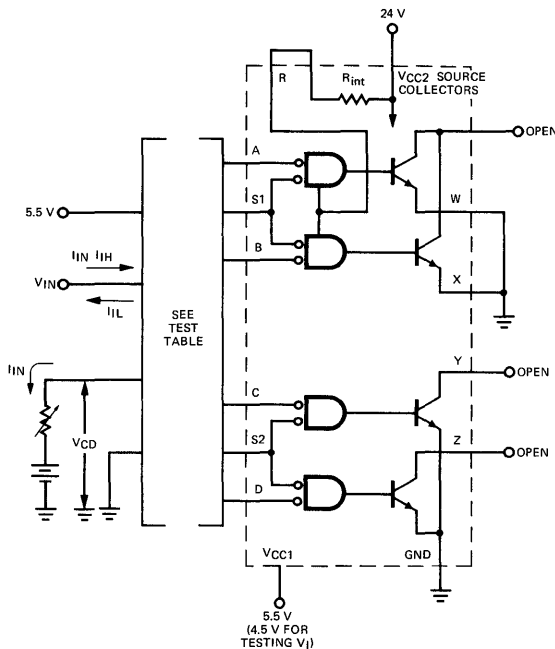
Fig. 3 V_{IL} AND SOURCE $V_{(sat)}$ (Note 4)



TEST TABLE

C	D	S2	Y	Z
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

Fig. 4 V_{IL} AND SINK $V_{(sat)}$ (Note 4)



TEST TABLES

I_I, I_{IH}

APPLY $V_{IN} = 5.5 V$, MEASURE I_{IN}	GROUND	APPLY 5.5 V
APPLY $V_{IN} = 2.4 V$, MEASURE I_{IH}		
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY $V_{IN} = 0.4 V$, MEASURE I_{IL}	APPLY 5.5 V
APPLY $I_{IN} = -10 mA$, MEASURE V_{CD}	
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

Fig. 5 $V_{IN}, V_{CD}, I_{IN}, I_{IH},$ AND I_{IL}

† Arrows indicate actual direction of current flow.

DC TEST CIRCUITS (Cont'd)

PARAMETER MEASUREMENT INFORMATION

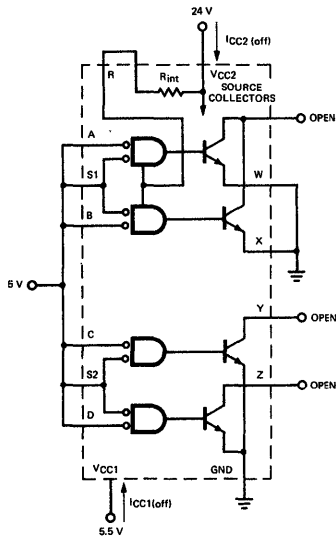
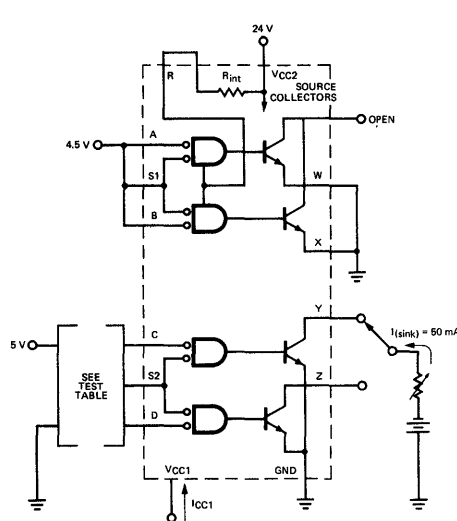
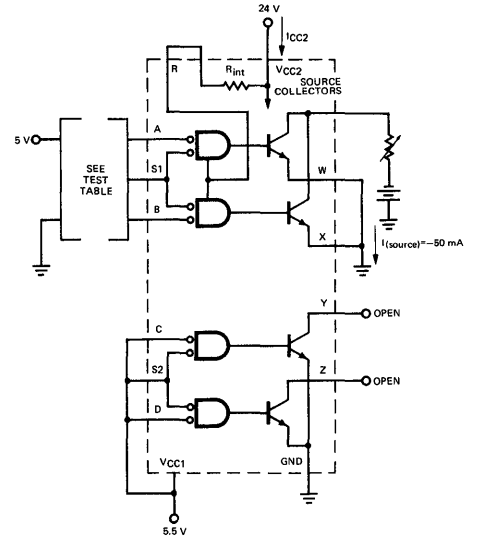


Fig. 6 I_{CC1}(OFF) AND I_{CC2}(OFF)



TEST TABLE				
C	D	S2	Y	Z
GND	5 V	GND	I _(sink)	OPEN
5 V	GND	GND	OPEN	I _(sink)

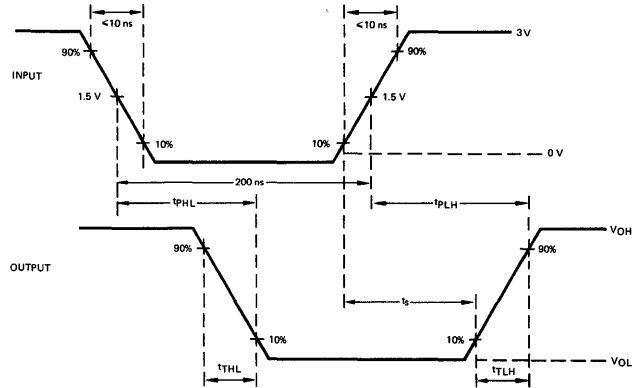
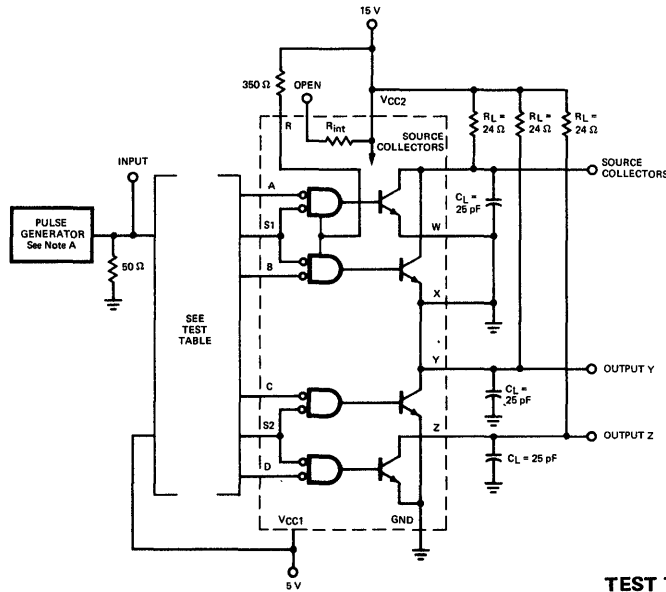
Fig. 7 I_{CC1}, EITHER SINK ON



TEST TABLE		
A	B	S1
GND	5 V	GND
5 V	GND	GND

Fig. 8 I_{CC2}, EITHER SOURCE ON

SWITCHING CHARACTERISTICS



VOLTAGE WAVEFORMS

TEST TABLE

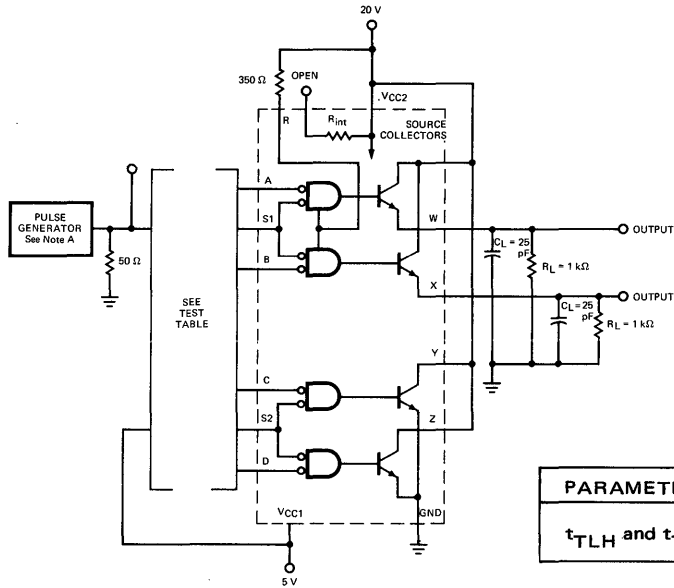
PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t _{PLH} and t _{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t _{PLH} , t _{PHL} , t _{TLH} , t _{THL} , and t _s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

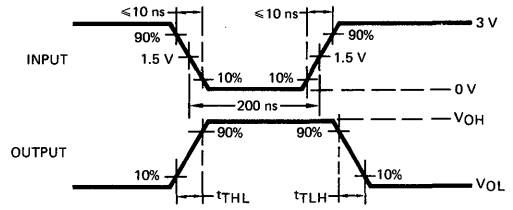
Fig. 9 SWITCHING TIMES

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION (Cont'd)
SWITCHING CHARACTERISTICS (Cont'd)



VOLTAGE WAVEFORMS



TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2

NOTES: A. The pulse generator has the following characteristics: $Z_{out} = 50 \Omega$, duty cycle $\leq 1\%$.
B. C_L includes probe and jig capacitance.

Fig. 10 TRANSITION TIMES OF SOURCE OUTPUTS

APPLICATIONS

In memory-drive applications the 75325 (or for full-temperature operation, the 55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 11. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, 9311 No. 1 must be set to 3 (with mode select HIGH), enabling source X of 75325 No. 2 to drive lines 12 through 15, and 9311 No. 2 must be set to 2, providing a sink at Y of 75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from HIGH to LOW. The size of such a matrix is limited only by the number of drive-lines that a source sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver.

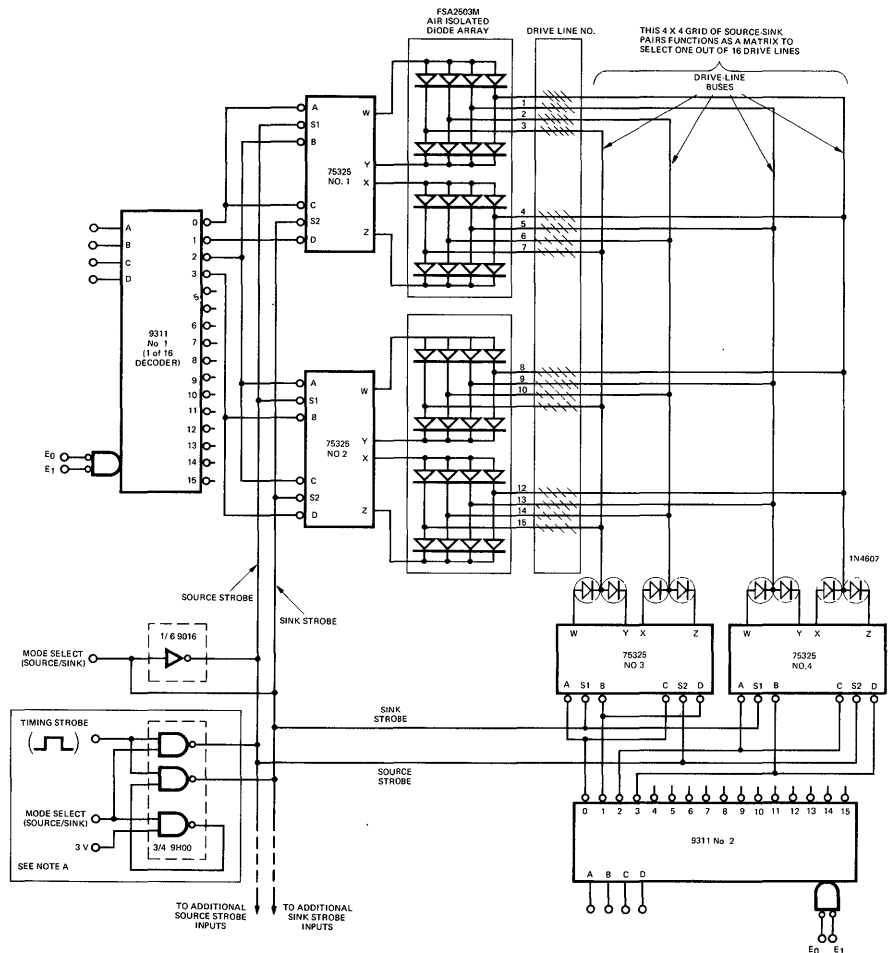


Fig. 11 75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

NOTE A: This optional mode-select and timing-strobe technique can be used in place of the 9N40 mode-select and 9311 timing-strobe when minimum time skew is desired.

APPLICATIONS (Cont'd)

EXTERNAL RESISTOR CALCULATION — A typical magnetic-memory word drive requirement is shown in Figure 12. A source-output transistor of one 75325 delivers load current (I_L). The sink-output transistor of another 75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16 [V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6 [V_{CC2(min)} - V_S - 2.9]} \quad \text{where: } R_{ext} \text{ is in } k\Omega, \quad \text{(Equation 1)}$$

$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
 V_S is the source output voltage in volts with respect to ground,
 I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{R_{ext}} \approx \frac{I_L}{16} [V_{CC2(min)} - V_S - 2] \quad \text{where: } P_{R_{ext}} \text{ is in mW.} \quad \text{(Equation 2)}$$

After solving for R_{ext} , the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94 I_L \quad \text{where: } I_{CS} \text{ is in mA.} \quad \text{(Equation 3)}$$

As an example, let $V_{CC2(min)} = 20$ V and $V_L = 3$ V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16 (20 - 3 - 2.2)}{500 - 1.6 (20 - 3 - 2.9)} = 0.5 \text{ } k\Omega$$

and from Equation 2,

$$P_{R_{ext}} \approx \frac{500}{16} [20 - 3 - 2] \approx 470 \text{ mW}$$

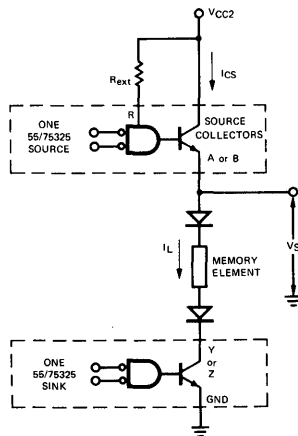
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94 (500) \approx 470 \text{ mA}$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L .

TYPICAL APPLICATION DATA

EXTERNAL RESISTOR CALCULATION (Cont'd)



NOTES: A. For clarity, partial logic diagrams of two 75325's are shown.
 B. Source and sink shown are in different packages.

Fig. 12

THERMAL INFORMATION

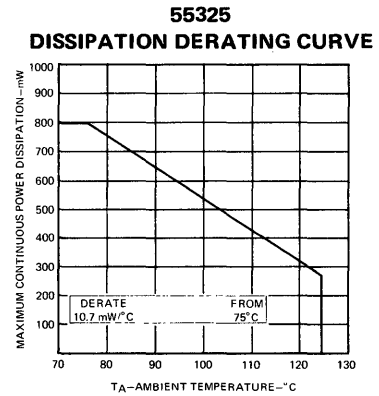


Fig. 13

7524 • 7525

TWO CHANNEL CORE MEMORY SENSE AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

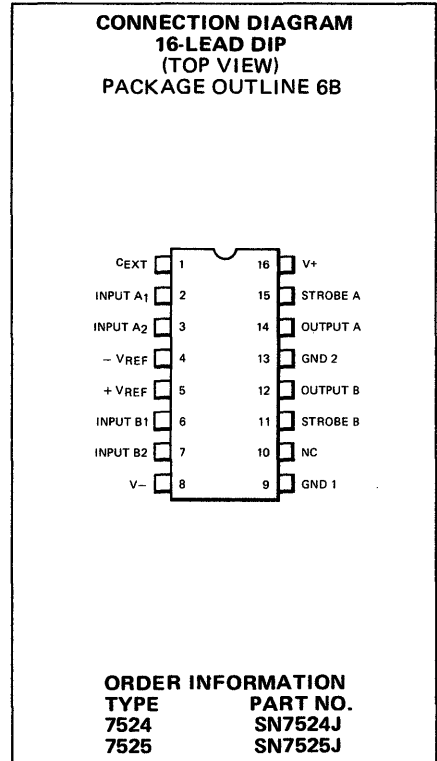
GENERAL DESCRIPTION — The 7524 and 7525 are Two Channel Core Memory Sense Amplifiers constructed on a silicon chip using the patented Fairchild Planar* epitaxial process. They can be used for small (1K to 8K words) memories as well as larger memory systems. The devices are suitable for small core sizes facilitating very fast memory cycle times. The 7524 and 7525 feature tight threshold accuracy, fast response time, and independent strobe selection. Unit to unit variations are minimized so that individual adjustments of the threshold and strobe timing are not necessary.

All logic inputs and outputs are fully TTL compatible. The 7524 and 7525 can be combined with the Fairchild MSI Quad Latch 9314 to provide complete memory data register capability.

- ± 2 mV THRESHOLD VARIATION
- 25 ns PROPAGATION DELAY
- DUAL INDEPENDENT STROBES
- TTL COMPATIBLE

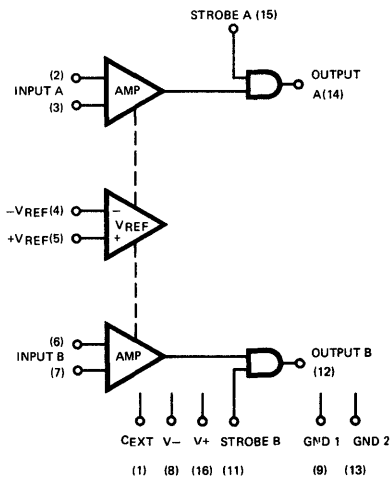
ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	± 5.0 V
Supply Voltage	± 7.0 V
Logic Input Voltage	$+5.5$ V
Power Dissipation	730 mW
Storage Temperature	
Hermetic DIP (SN7524J, SN7524J)	-65°C to $+150^{\circ}\text{C}$
Molded DIP (SN7524N, SN7525N)	-55°C to $+125^{\circ}\text{C}$
Operating Temperature	0°C to $+70^{\circ}\text{C}$
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	$+300^{\circ}\text{C}$
Molded DIP (Soldering, 10 seconds)	$+260^{\circ}\text{C}$
Signal Input	± 3.0 V
Reference Input	± 3.0 V



6

BLOCK DIAGRAM



FAIRCHILD LINEAR INTEGRATED CIRCUITS • 7524 • 7525

7524 • 7525

ELECTRICAL CHARACTERISTICS ($V_+ = 5.0\text{ V}$, $V_- = -5.0\text{ V}$, 0°C to $+70^\circ\text{C}$ either amplifier unless otherwise specified).

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
7524					
Differential Input Threshold Voltage	$V_{\text{ref}} = 15\text{ mV}$	11		19	mV
	$V_{\text{ref}} = 40\text{ mV}$	36		44	mV
7525					
Differential Input Threshold Voltage	$V_{\text{ref}} = 15\text{ mV}$	8.0		22	mV
	$V_{\text{ref}} = 40\text{ mV}$	33		47	mV

The following specifications apply to either the 7524 or the 7525:

Threshold Voltage Range	Minimum		10		mV
	Maximum		50		mV
Threshold Uncertainty			± 2.0		mV
Differential Input Bias Current	$V_{\text{IN D}} = 0\text{ mV}$		15	75	μA
Differential Input Offset Current	$V_{\text{IN D}} = 0\text{ mV}$		1.0		μA
Differential Input Impedance	$f = 1.0\text{ kHz}$		2.5		$\text{k}\Omega$
Positive Supply Current	$T_A = 25^\circ\text{C}$, $V^+ = 5.25\text{ V}$, $V^- = -5.25\text{ V}$		25	40	mA
Negative Supply Current	$T_A = 25^\circ\text{C}$, $V^+ = 5.25\text{ V}$, $V^- = -5.25\text{ V}$		10	20	mA
Output Short-Circuit Current	$V^+ = 5.25\text{ V}$, $V^- = -5.25\text{ V}$	2.1		3.5	mA

LOGIC INPUT/OUTPUT CONDITIONS (See Fig. 2)

Output HIGH Voltage	1 Load = $400\ \mu\text{A}$ $V_{\text{IN}(1)}$ Strobe = 2.0 V $V_{\text{IN}(0)}$ Strobe = 0.8 V $V^+ = 4.75\text{ V}$, $V^- = -4.75\text{ V}$	2.4	3.9		V
Output LOW Voltage	1 Sink = 16 mA $V_{\text{IN}(0)}$ Strobe = 0.8 V $V^+ = 4.75\text{ V}$, $V^- = -4.75\text{ V}$		0.25	0.4	V
Input HIGH Voltage (Strobe Inputs)	$V_{\text{IN}(0)}$ Strobe = 0.8 V $V^+ = 4.75\text{ V}$, $V^- = -4.75\text{ V}$	2.0			V
Input LOW Voltage (Strobe Inputs)	$V_{\text{IN}(1)}$ Strobe = 2.0 V $V^+ = 4.75\text{ V}$, $V^- = -4.75\text{ V}$			0.8	V
Input LOW Current (Strobe Inputs)	$V_{\text{IN}(0)}$ Strobe = 0.4 V $V^+ = 5.25\text{ V}$, $V^- = -5.25\text{ V}$		-1.0	-1.6	mA
Input HIGH Current (Strobe Inputs)	$V_{\text{IN}(1)}$ Strobe = 2.4 V $V^+ = 5.25\text{ V}$, $V^- = -5.25\text{ V}$			40	μA
	$V_{\text{IN}(1)}$ Strobe = V^+ $V^+ = 5.25\text{ V}$, $V^- = -5.25\text{ V}$			1.0	mA

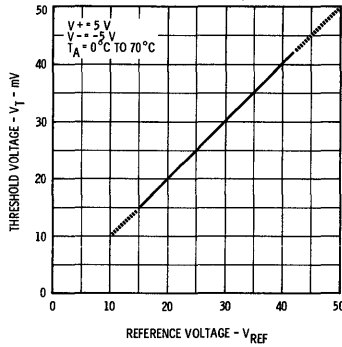
AC CHARACTERISTICS

$T_A = 25^\circ\text{C}$

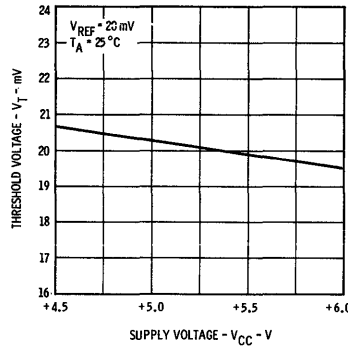
Common Mode Input Firing Voltage	$t_r = t_f \leq 15\text{ ns}$ $t_p = 50\text{ ns}$		± 3.0		V
Differential Input Overload Recovery Time	$V_{\text{IN}} + 2.0\text{ V}$, $t_r = t_f = 20\text{ ns}$		20		ns
Common Mode Input Overload Recovery Time	$V_{\text{IN CM}} = \pm 2.0\text{ V}$, $t_r = t_f = 20\text{ ns}$		20		ns
Input to Output Delay (See Figure 1)	$t_{\text{pd}}(1)\text{ D}$		25	40	ns
	$t_{\text{pd}}(0)\text{ D}$		35		ns
Strobe to Output Delay (See Figure 1)	$t_{\text{pd}}(1)\text{ Strobe}$		15	30	ns
	$t_{\text{pd}}(0)\text{ Strobe}$		25		ns

TYPICAL PERFORMANCE CURVES FOR 7524 AND 7525

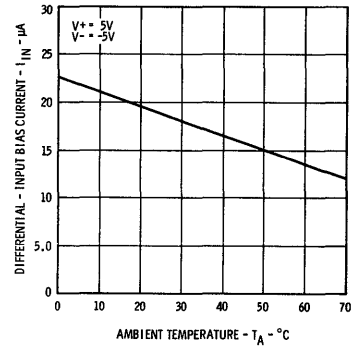
THRESHOLD VOLTAGE AS A FUNCTION OF REFERENCE VOLTAGE



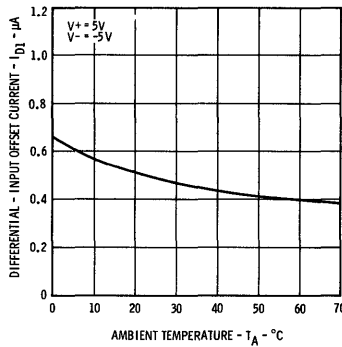
THRESHOLD VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



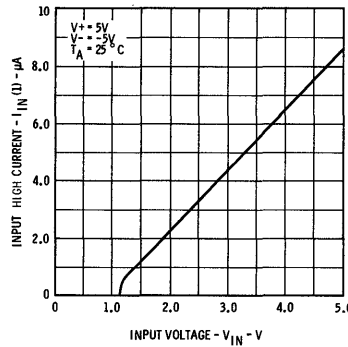
DIFFERENTIAL INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



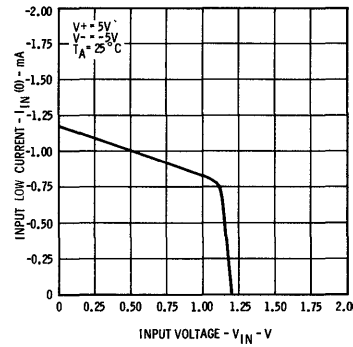
DIFFERENTIAL INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



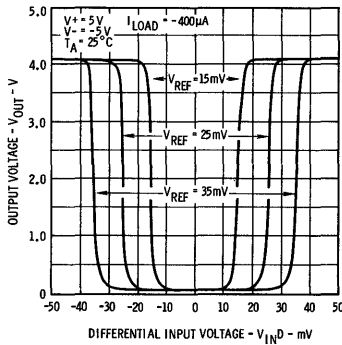
INPUT HIGH CURRENT AS A FUNCTION OF INPUT VOLTAGE



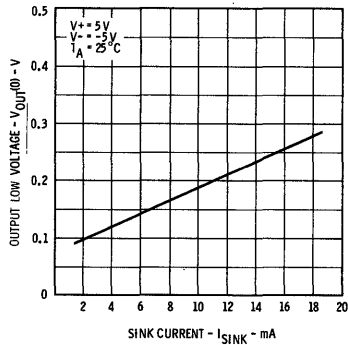
INPUT LOW CURRENT AS A FUNCTION OF INPUT VOLTAGE



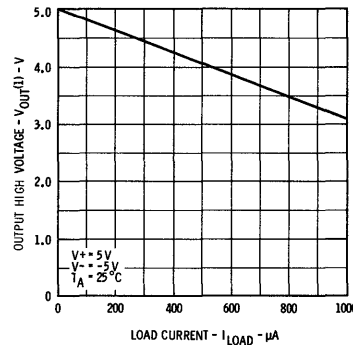
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



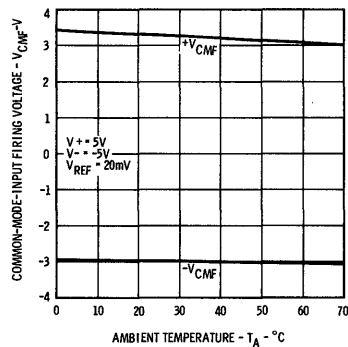
OUTPUT LOW VOLTAGE AS A FUNCTION OF SINK CURRENT



OUTPUT HIGH VOLTAGE AS A FUNCTION OF LOAD CURRENT

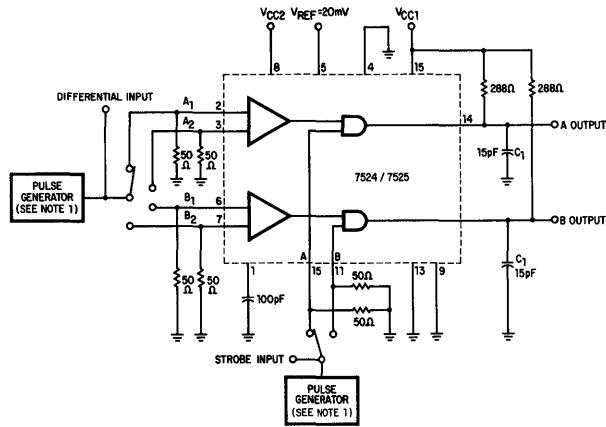


COMMON-MODE FIRING VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

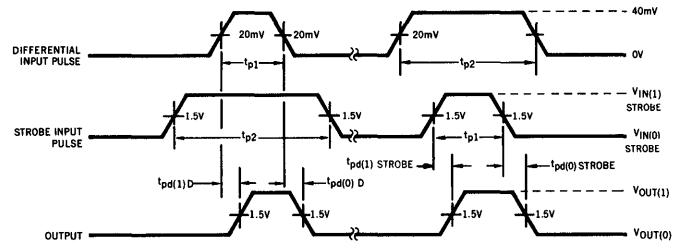


PROPAGATION DELAY

TEST CIRCUITS



VOLTAGE WAVEFORMS

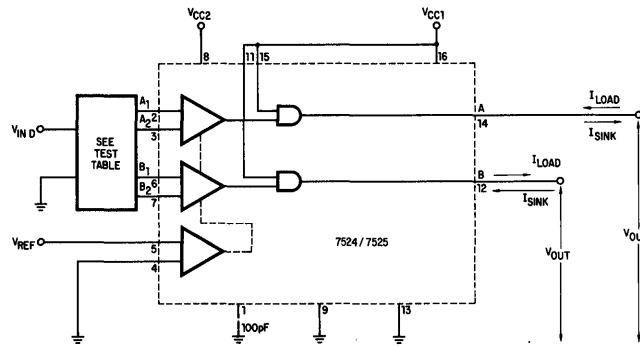


NOTES:

1. Pulse generators have the following characteristics:
 $Z_{OUT} = 50 \Omega$, $t_r = t_f = 15 (\pm 5) \text{ ns}$, $t_{p1} = 100 \text{ ns}$, $t_{p2} = 300 \text{ ns}$,
 $PRR = 1 \text{ MHz}$.
2. Strobe input pulse is applied to Strobe A when inputs $A_1 - A_2$ are being tested and to Strobe B when inputs $B_1 - B_2$ are being tested.
3. C_1 includes probe and jig capacitance.

Fig. 1

DC TEST



TEST TABLE

TYPE	INPUTS	V_{ref}	$V_{IN D}$	OUTPUT		
				V_{OUT}	I_{sink}	I_{load}
7524	$A_1 - A_2$ or $B_1 - B_2$	15 mV	< 11 mV	$\leq 0.4 \text{ V}$	16 mA	—
	$A_1 - A_2$ or $B_1 - B_2$	15 mV	> 19 mV	$\geq 2.4 \text{ V}$	—	-400 μA
	$A_1 - A_2$ or $B_1 - B_2$	40 mV	< 36 mV	$\leq 0.4 \text{ V}$	16 mA	—
	$A_1 - A_2$ or $B_1 - B_2$	40 mV	> 44 mV	$\geq 2.4 \text{ V}$	—	-400 μA
7525	$A_1 - A_2$ or $B_1 - B_2$	15 mV	< 8 mV	$\leq 0.4 \text{ V}$	16 mA	—
	$A_1 - A_2$ or $B_1 - B_2$	15 mV	> 22 mV	$\geq 2.4 \text{ V}$	—	-400 μA
	$A_1 - A_2$ or $B_1 - B_2$	40 mV	< 33 mV	$\leq 0.4 \text{ V}$	16 mA	—
	$A_1 - A_2$ or $B_1 - B_2$	40 mV	> 47 mV	$\geq 2.4 \text{ V}$	—	-400 μA

Fig. 2

75450A • 75451A • 75452 • 75453 • 75454 75460A • 75461A • 75462A • 75463A • 75464A

DUAL PERIPHERAL DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 75450A, 75451A, 75452, 75453, and 75454 are Dual General Purpose Interface Drivers that convert TTL and DTL logic levels to high current drive capability. The 75450A features two TTL NAND gates and two uncommitted transistors. The 75451A, 75452, 75453 and 75454 feature two standard series 74 TTL gates in AND, NAND, OR and NOR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

The 75460A series are functionally interchangeable with the 75450 series and are recommended for use in applications requiring a minimum collector to emitter breakdown voltage of 60 V.

The 75450 series and 75460A series offer flexibility in designing high speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- HIGH SPEED SWITCHING
- HIGH OUTPUT CURRENT CAPABILITY
- UNCOMMITTED COLLECTOR OUTPUT DEVICES FOR HIGH OUTPUT VOLTAGE CAPABILITY
- TTL OR DTL INPUT COMPATIBILITY
- INPUT CLAMP DIODES
- +5 VOLT SUPPLY VOLTAGE

ABSOLUTE MAXIMUM RATINGS

	75450A	75460A	75451A 75452 75453 75454	75461A 75462A 75463A 75464A
Supply Voltage, V_{CC}	7 V	7 V	7 V	7 V
Input Voltage (See Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage (See Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (See Note 6)	35 V	65 V		
Collector to Substrate Voltage (See Note 6)	35 V	65 V		
Collector-base Voltage	35 V	65 V		
Collector-emitter Voltage (See Note 3)	30 V	60 V		
Emitter-base Voltage	5 V	5 V		
Output Voltage (See Notes 1 and 4)			30 V	60 V
Continuous Collector Current (See Note 5)	300 mA	300 mA		
Continuous Output Current (See Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (See Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Free-Air Temperature Range	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
Storage Temperature Range				
Molded DIP	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C
Hermetic DIP	-65°C to 150°C	-65°C to 150°C	-65°C to 150°C	-65°C to 150°C
Lead Temperature				
Molded DIP (Soldering, 10 seconds)	260°C	260°C	260°C	260°C
Hermetic DIP (Soldering, 30 seconds)	300°C	300°C	300°C	300°C

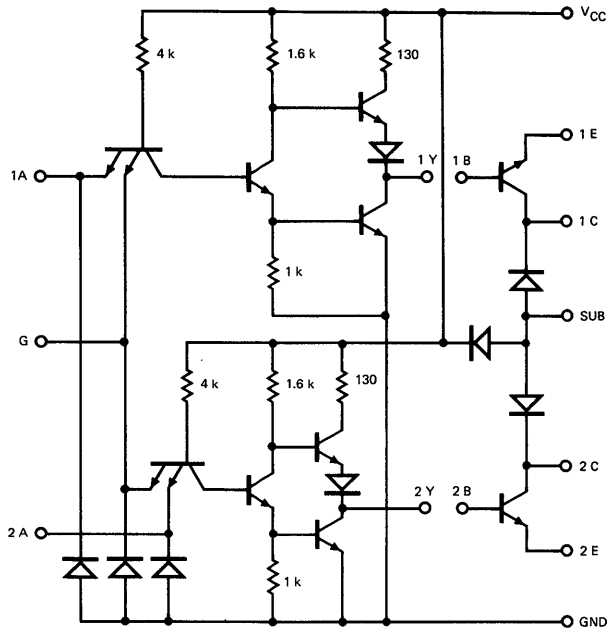
NOTES:

1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω .
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 75450A and 75460A only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 70°C ambient temperature, derate linearly at 8.3 mW/°C.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

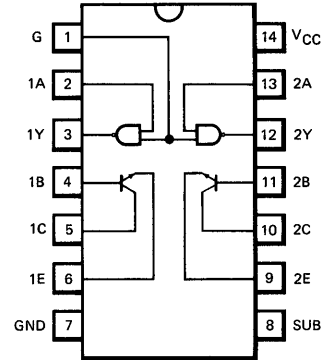
75450A
DUAL POSITIVE-AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A



LOGIC FUNCTION

Positive Logic: $Y = \overline{AG}$ (gate only)
 $C = AG$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
75450A	SN75450AJ
75450A	SN75450AN

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to 70°C , unless otherwise noted)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	1		2			V
V_{IL}	Input LOW Voltage	2				0.8	V
V_{CD}	Input Clamp Diode Voltage	3	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	Output HIGH Voltage	2	$V_{CC} = 4.75 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.3		V
V_{OL}	Output LOW Voltage	1	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	Input A	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1	mA
		Input G		2			
I_{IH}	Input HIGH Current	Input A	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
		Input G		80			
I_{IL}	Input LOW Current	Input A	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$			-1.6	mA
		Input G		-3.2			
I_{OS}	Short-Circuit Output Current‡	5	$V_{CC} = 5.25 \text{ V}$	-18		-55	mA
I_{CCH}	Supply Current, Output HIGH	6	$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		2	4	mA
I_{CCL}	Supply Current, Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		6	11	

†All typical values at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

‡Not more than one output should be shorted at a time.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75450A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted) Cont'd.

Output Transistors

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100\ \mu\text{A}$ $I_E = 0$	35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	$I_C = 100\ \mu\text{A}$ $R_{BE} = 500\ \Omega$	30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 100\ \mu\text{A}$ $I_C = 0$	5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 8)	$V_{CE} = 3\text{ V}$, $I_C = 100\text{ mA}$, $T_A = 25^\circ\text{C}$	25			
		$V_{CE} = 3\text{ V}$, $I_C = 300\text{ mA}$, $T_A = 25^\circ\text{C}$	30			
		$V_{CE} = 3\text{ V}$, $I_C = 100\text{ mA}$, $T_A = 0^\circ\text{C}$	20			
		$V_{CE} = 3\text{ V}$, $I_C = 300\text{ mA}$, $T_A = 0^\circ\text{C}$	25			
$V_{BE(sat)}$	Base-Emitter Voltage (Note 8)	$I_B = 10\text{ mA}$, $I_C = 100\text{ mA}$		0.85	1	V
		$I_B = 30\text{ mA}$, $I_C = 300\text{ mA}$		1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 8)	$I_B = 10\text{ mA}$, $I_C = 100\text{ mA}$		0.25	0.4	V
		$I_B = 30\text{ mA}$, $I_C = 300\text{ mA}$		0.5	0.7	

†All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

Note 8: These parameters must be measured using pulse techniques. $t_w = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

AC CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		20		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8		ns

Output Transistors

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS‡	MIN.	TYP.	MAX.	UNIT
t_d	Delay Time	13	$I_C = 200\text{ mA}$, $I_{B(1)} = 20\text{ mA}$, $I_{B(2)} = -40\text{ mA}$, $V_{BE(off)} = -1\text{ V}$, $C_L = 15\text{ pF}$, $R_L = 50\ \Omega$		8		ns
t_r	Rise Time				12		ns
t_s	Storage Time				7		ns
t_f	Fall Time				6		ns

Gates and Transistors Combined

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS‡	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_C = 200\text{ mA}$, $C_L = 15\text{ pF}$, $R_L = 50\ \Omega$		40		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

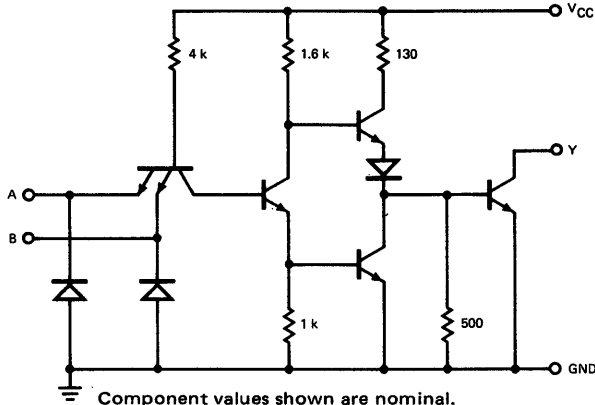
‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

6

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75451A
DUAL POSITIVE-AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



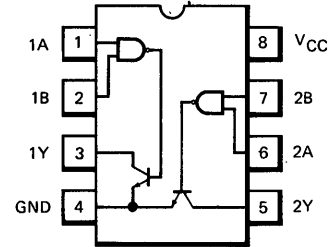
Component values shown are nominal.
All resistor values in ohms.

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = HIGH Level, L = LOW Level

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



Positive Logic: Y = AB

ORDER INFORMATION

TYPE PART NO.
75451A SN75451AP

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to 70°C , unless otherwise noted)

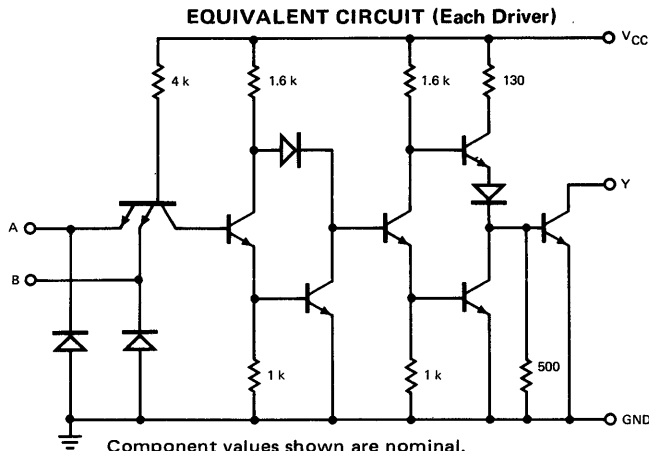
SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	Output HIGH Current	7	$V_{CC} = 4.75 \text{ V}$, $V_{OH} = 30 \text{ V}$ $V_{IH} = 2 \text{ V}$			100	μA
V_{OL}	Output LOW Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$		0.25	0.4	V
			$V_{CC} = 4.75 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	Input HIGH Current	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Input LOW Current	8	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		7.0	11	mA
I_{CCL}	Supply Current, Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		52	65	mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		45		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

75452
DUAL POSITIVE-NAND PERIPHERAL DRIVER



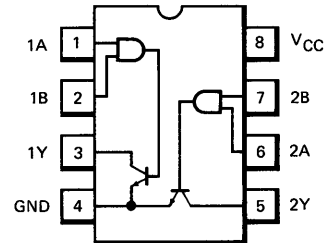
Component values shown are nominal.
All resistor values in ohms.

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = HIGH Level, L = LOW Level.

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



Positive Logic: $Y = \overline{AB}$

ORDER INFORMATION

TYPE PART NO.
75452 SN75452P

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	Output HIGH Current	7	$V_{CC} = 4.75 \text{ V}$, $V_{OH} = 30 \text{ V}$, $V_{IL} = 0.8 \text{ V}$			100	μA
V_{OL}	Output LOW Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 100 \text{ mA}$		0.25	0.4	V
			$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 300 \text{ mA}$		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	Input HIGH Current	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Input LOW Current	8	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		11	14	mA
I_{CCL}	Supply Current, Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		56	71	mA

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

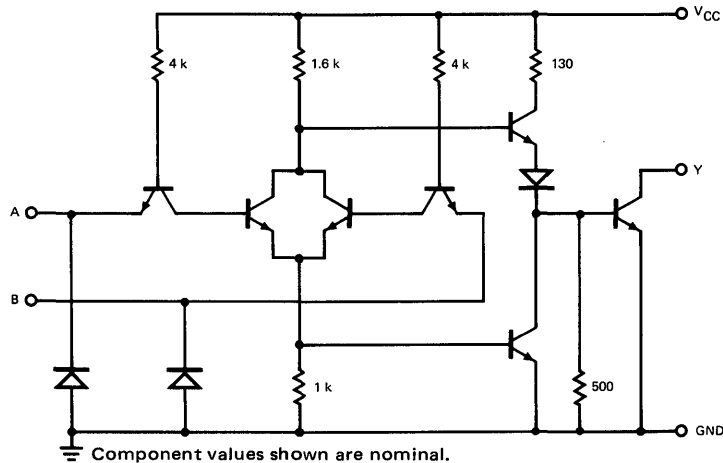
AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		50		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				35		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75453
DUAL POSITIVE-OR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



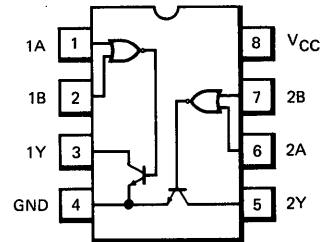
Component values shown are nominal.
All resistor values in ohms.

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = HIGH Level, L = LOW Level

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



Positive Logic: $Y = A + B$

ORDER INFORMATION

TYPE PART NO.
75453 SN75453P

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to 70°C , unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	Output HIGH Current	7	$V_{CC} = 4.75 \text{ V}$, $V_{OH} = 30 \text{ V}$ $V_{IH} = 2 \text{ V}$			100	μA
V_{OL}	Output LOW Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$		0.25	0.4	V
			$V_{CC} = 4.75 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	Input HIGH Current	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Input LOW Current	8	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		8.0	11	mA
I_{CCL}	Supply Current, Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		54	68	mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

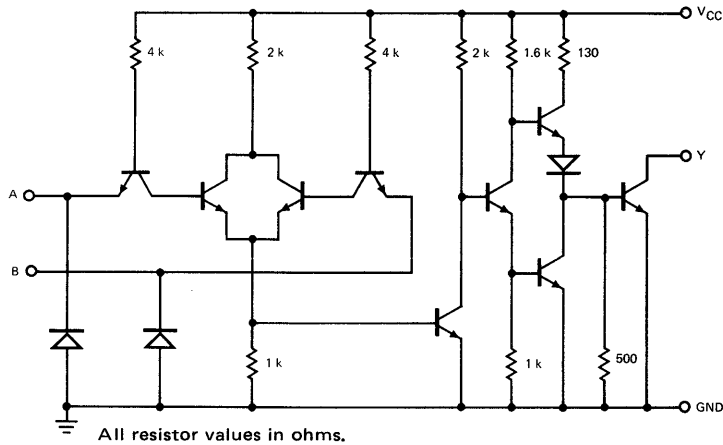
AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		35		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75454
DUAL POSITIVE-NOR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



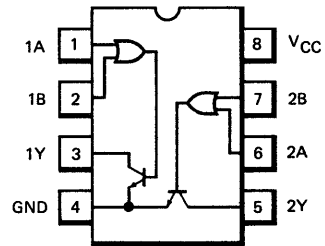
All resistor values in ohms.

TRUTH TABLE

A	B	Y	
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

CONNECTION DIAGRAM
8-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 9T



Positive Logic: $Y = \overline{A + B}$

ORDER INFORMATION

TYPE PART NO.
75454 SN75454P

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	Output HIGH Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{OH} = 30 \text{ V}$, $V_{IL} = 0.8 \text{ V}$			100	μA
V_{OL}	Output LOW Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 100 \text{ mA}$		0.25	0.4	V
			$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 300 \text{ mA}$		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	Input HIGH Current	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Input LOW Current	8	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		13	17	mA
I_{CCL}	Supply Current Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		61	79	mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$)

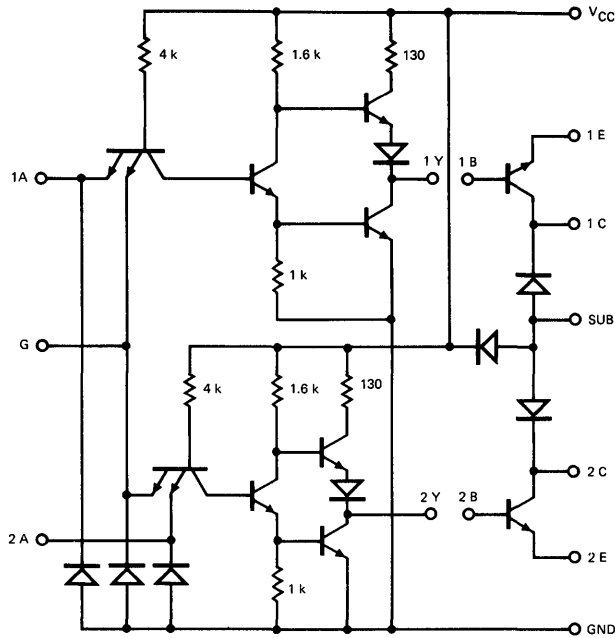
SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		50		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75460A

DUAL POSITIVE-AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



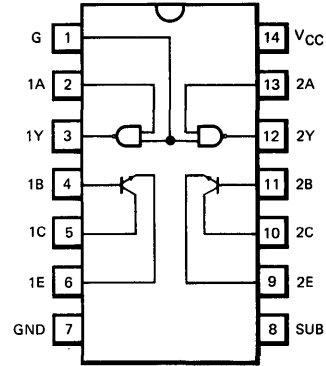
All resistor values in ohms.

CONNECTION DIAGRAM

14-LEAD DIP

(TOP VIEW)

PACKAGE OUTLINE 6A, 9A



LOGIC FUNCTION

Positive Logic: $Y = \overline{AG}$ (gate only)
 $C = AG$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
75460A	SN75460AJ
75460A	SN75460AN

75460A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	1		2			V
V_{IL}	Input LOW Voltage	2				0.8	V
V_{CD}	Input Clamp Diode Voltage	3	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	Output HIGH Voltage	2	$V_{CC} = 4.75 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.3		V
V_{OL}	Output LOW Voltage	1	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	Input A	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1	mA
		Input G		2			
I_{IH}	Input HIGH Current	Input A	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
		Input G		80			
I_{IL}	Input LOW Current	Input A	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$			-1.6	mA
		Input G		-3.2			
I_{OS}	Short-Circuit Output Current‡	5	$V_{CC} = 5.25 \text{ V}$	-18		-55	mA
I_{CCH}	Supply Current, Output HIGH	6	$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		2	4	mA
I_{CCL}	Supply Current, Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		6	11	

†All typical values at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡Not more than one output should be shorted at a time.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75460A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to 70°C , unless otherwise noted) Cont'd.

Output Transistors

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100 \mu\text{A}$ $I_E = 0$	65			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	$I_C = 100 \mu\text{A}$ $R_{BE} = 500 \Omega$	60			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 100 \mu\text{A}$ $I_C = 0$	5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 8)	$V_{CE} = 3 \text{ V}$, $I_C = 100 \text{ mA}$, $T_A = 25^\circ \text{C}$	25			
		$V_{CE} = 3 \text{ V}$, $I_C = 300 \text{ mA}$, $T_A = 25^\circ \text{C}$	30			
		$V_{CE} = 3 \text{ V}$, $I_C = 100 \text{ mA}$, $T_A = 0^\circ \text{C}$	20			
		$V_{CE} = 3 \text{ V}$, $I_C = 300 \text{ mA}$, $T_A = 0^\circ \text{C}$	25			
$V_{BE(sat)}$	Base-Emitter Voltage (Note 8)	$I_B = 10 \text{ mA}$, $I_C = 100 \text{ mA}$		0.85	1	V
		$I_B = 30 \text{ mA}$, $I_C = 300 \text{ mA}$		1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 8)	$I_B = 10 \text{ mA}$, $I_C = 100 \text{ mA}$		0.25	0.4	V
		$I_B = 30 \text{ mA}$, $I_C = 300 \text{ mA}$		0.5	0.7	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

Note 8: These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

75460A

AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		20		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8		ns

Output Transistors

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS‡	MIN.	TYP.	MAX.	UNIT
t_d	Delay Time	13	$I_C = 200 \text{ mA}$, $I_{B(1)} = 20 \text{ mA}$, $I_{B(2)} = -40 \text{ mA}$, $V_{BE(off)} = -1 \text{ V}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		8		ns
t_r	Rise Time				12		ns
t_s	Storage Time				7		ns
t_f	Fall Time				6		ns

Gates and Transistors Combined

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS‡	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_C = 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		40		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

‡ Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

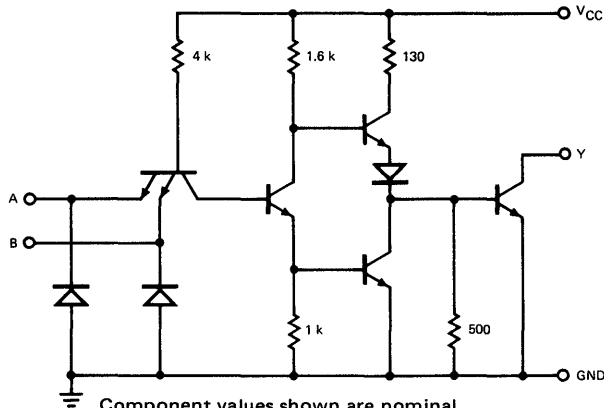
6

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75461A

DUAL POSITIVE-AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



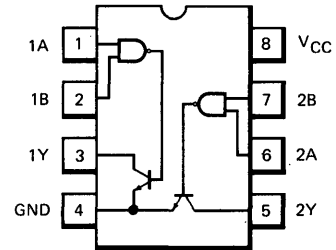
Component values shown are nominal.
All resistor values in ohms.

TRUTH TABLE

A	B	Y	
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

**CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T**



Positive Logic: Y = AB

ORDER INFORMATION

TYPE PART NO.
75461A SN75461AP

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to 70°C , unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	Output HIGH Current	7	$V_{CC} = 4.75 \text{ V}$, $V_{OH} = 60 \text{ V}$ $V_{IH} = 2 \text{ V}$			100	μA
V_{OL}	Output LOW Voltage	7	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 100 \text{ mA}$, $V_{IL} = 0.8 \text{ V}$		0.25	0.4	V
			$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 300 \text{ mA}$, $V_{IL} = 0.8 \text{ V}$		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	Input HIGH Current	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Input LOW Current	8	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		7.0	11	mA
I_{CCL}	Supply Current, Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		52	65	mA

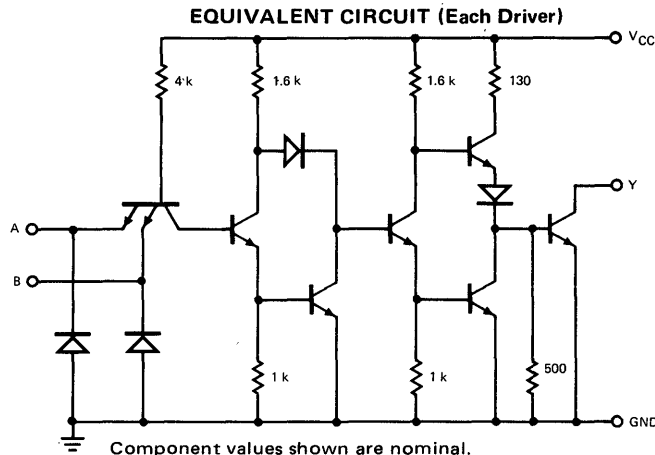
†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		45		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75462A
DUAL POSITIVE-NAND PERIPHERAL DRIVER



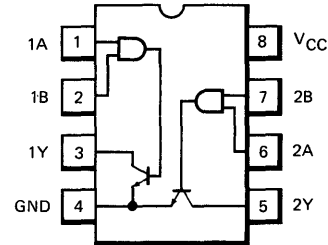
Component values shown are nominal.
All resistor values in ohms.

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = HIGH Level, L = LOW Level.

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



Positive Logic: $Y = \overline{AB}$

ORDER INFORMATION

TYPE PART NO.
75462A SN75462AP

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to 70°C , unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	Output HIGH Current	7	$V_{CC} = 4.75 \text{ V}$, $V_{OH} = 60 \text{ V}$ $V_{IL} = 0.8 \text{ V}$			100	μA
V_{OL}	Output LOW Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 100 \text{ mA}$		0.25	0.4	V
			$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 300 \text{ mA}$		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	Input HIGH Current	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Input LOW Current	8	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		11	14	mA
I_{CCL}	Supply Current, Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		56	71	mA

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

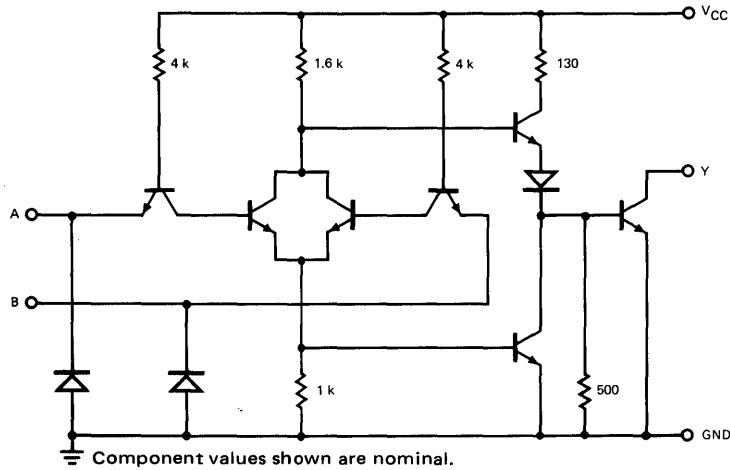
AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		50		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				35		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75463A
DUAL POSITIVE-OR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



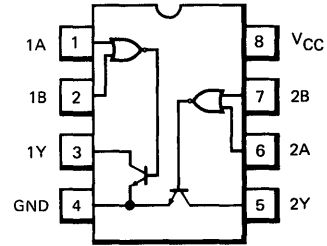
Component values shown are nominal.
All resistor values in ohms.

TRUTH TABLE

A	B	Y	
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



Positive Logic: $Y = A + B$

ORDER INFORMATION

TYPE PART NO.
75463A SN75463AP

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to 70°C , unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	Output HIGH Current	7	$V_{CC} = 4.75 \text{ V}$, $V_{OH} = 60 \text{ V}$ $V_{IH} = 2 \text{ V}$			100	μA
V_{OL}	Output LOW Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$		0.25	0.4	V
			$V_{CC} = 4.75 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	Input HIGH Current	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Input LOW Current	8	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		8.0	11	mA
I_{CCL}	Supply Current, Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		54	68	mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

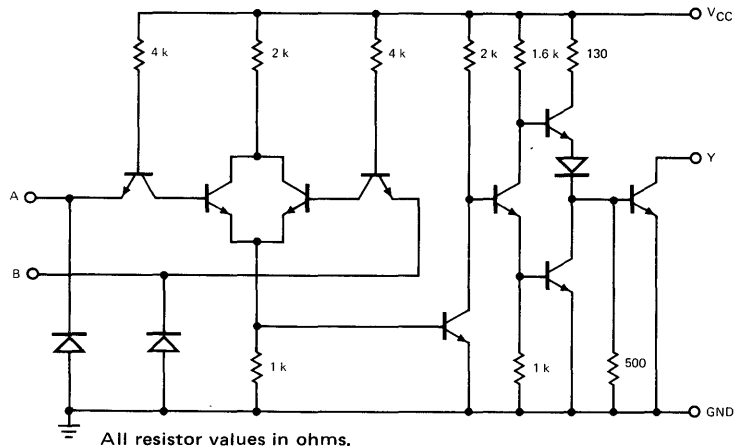
AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		35		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75450/75460A SERIES

75464A DUAL POSITIVE-NOR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



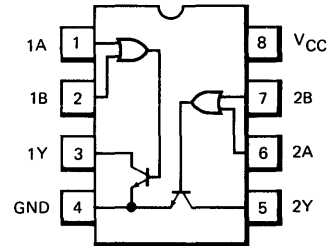
All resistor values in ohms.

TRUTH TABLE

A	B	Y	
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

**CONNECTION DIAGRAM
8-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 9T**



Positive Logic: $Y = \overline{A + B}$

ORDER INFORMATION

TYPE	PART NO.
75464A	SN75464AP

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to 70°C , unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.†	MAX.	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	$V_{CC} = 4.75 \text{ V}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	Output HIGH Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{OH} = 60 \text{ V}$ $V_{IL} = 0.8 \text{ V}$			100	μA
V_{OL}	Output LOW Voltage	7	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 100 \text{ mA}$		0.25	0.4	V
			$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 300 \text{ mA}$		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	Input HIGH Current	9	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Input LOW Current	8	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	$V_{CC} = 5.25 \text{ V}$, $V_I = 0 \text{ V}$		13	17	mA
I_{CCL}	Supply Current Output LOW		$V_{CC} = 5.25 \text{ V}$, $V_I = 5 \text{ V}$		61	79	mA

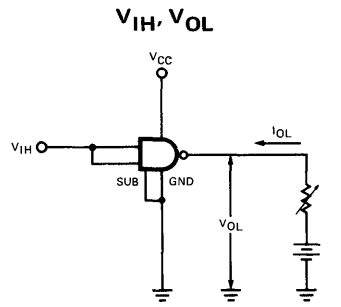
† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

AC CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$)

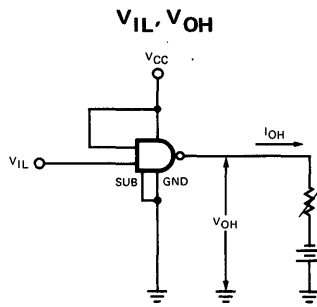
SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		50		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25		ns
t_{TLH}	Transition Time, Output LOW to HIGH				10		ns
t_{THL}	Transition Time, Output HIGH to LOW				12		ns

PARAMETER MEASUREMENT INFORMATION

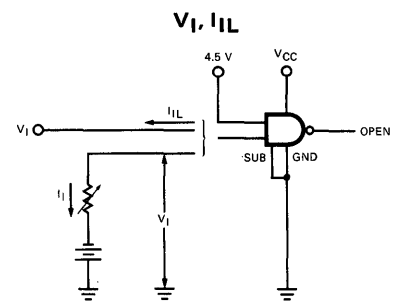
DC TEST CIRCUIT†



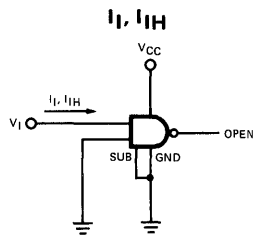
Both inputs are tested simultaneously.
Fig. 1



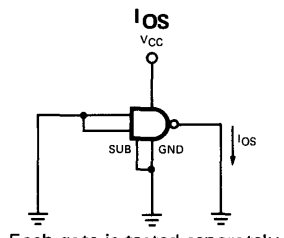
Each input is tested separately.
Fig. 2



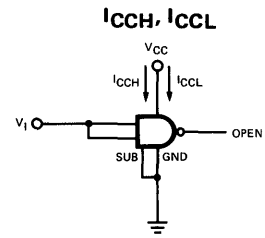
Each input is tested separately.
Fig. 3



Each input is tested separately.
Fig. 4



Each gate is tested separately.
(75450A and 75460A only)
Fig. 5



Both gates are tested simultaneously.
Fig. 6

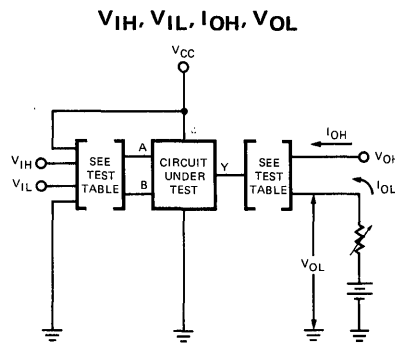
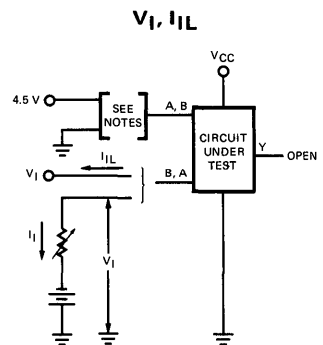


Fig. 7

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
75451A 75461A	VIH VIL	VIH VCC	VOH IOL	IOH VOL
75452 75462A	VIH VIL	VIH VCC	VOH IOH	VOL IOH
75453 75453A	VIH VIL	GND VIL	VOH IOL	IOH VOL
75454 75454A	VIH VIL	GND VIL	IOL VOH	VOL IOH

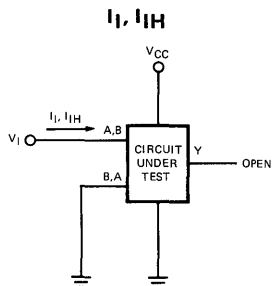
NOTE: Each input is tested separately.



NOTES:

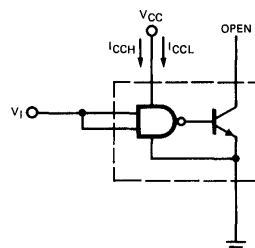
- A. Each input is tested separately.
- B. When testing 75453/75463A and 75454/75454A, input not under test is grounded. For all other circuits it is at 4.5 V.

Fig. 8



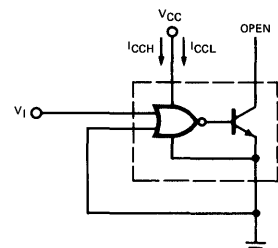
Each input is tested separately.
Fig. 9

ICCH, ICCL FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.
Fig. 10

ICCH, ICCL FOR OR, NOR CIRCUITS



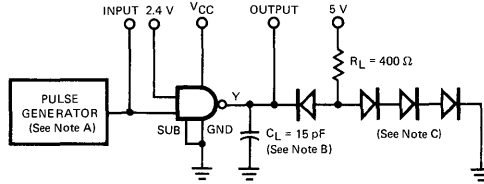
Both gates are tested simultaneously.
Fig. 11

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

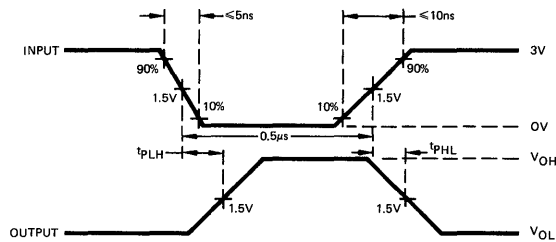
AC CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

PROPAGATION DELAY TIMES, EACH GATE (75450A, 75460A ONLY)
TEST CIRCUIT



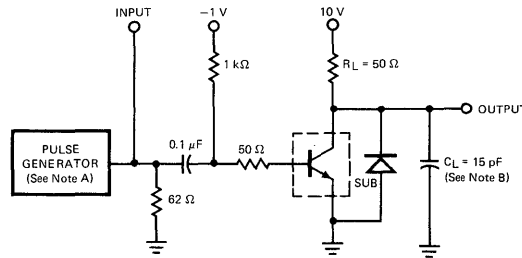
VOLTAGE WAVEFORMS



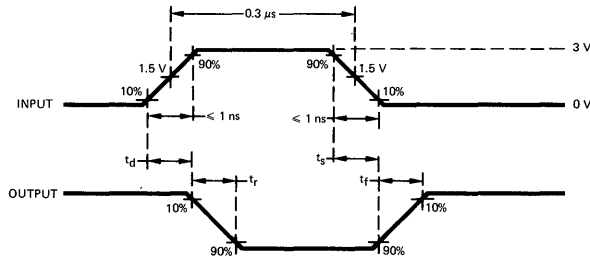
- NOTES: A The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50 \Omega$.
 B C_L include probe and jig capacitance.
 C All diodes are FD777.

Fig. 12

SWITCHING TIMES, EACH TRANSISTOR (75450A, 75460A ONLY)
TEST CIRCUIT



VOLTAGE WAVEFORMS



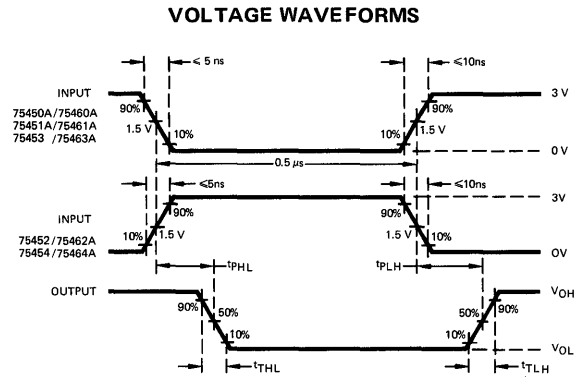
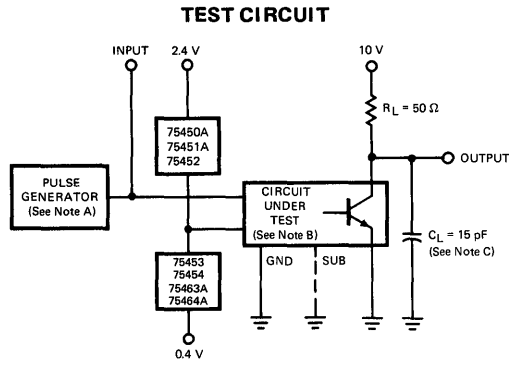
- NOTES: A. The pulse generator has the following characteristics: duty cycle $\le 1\%$, $Z_{out} \approx 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Fig. 13

AC CHARACTERISTICS (Cont'd)

PARAMETER MEASUREMENT INFORMATION

SWITCHING TIMES OF COMPLETE DRIVERS



- NOTES: A. The pulse generator has the following characteristics: PRR - 1 MHz, $Z_{out} \approx 50 \Omega$.
 B. When testing 75450A, connect output Y to transistor base and ground the substrate terminal.
 C. C_L includes probe and jig capacitance.

Fig. 14

TYPICAL PERFORMANCE CURVES FOR 75450 SERIES • 75460A SERIES

75450A • 75460A TTL GATE HIGH-LEVEL OUTPUT VOLTAGE AS A FUNCTION OF HIGH-LEVEL OUTPUT CURRENT

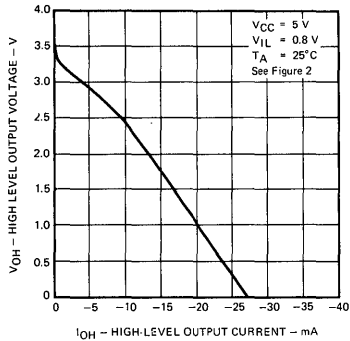


Fig. 15

75450A • 75460A TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT

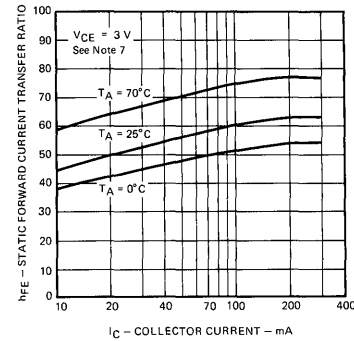


Fig. 16

75450A • 75460A TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT

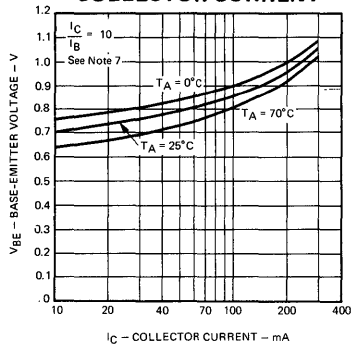


Fig. 17

TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT

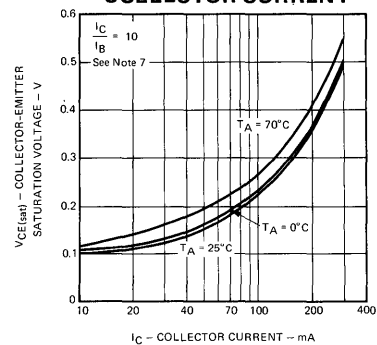


Fig. 18

NOTE 7. These parameters must be measured using pulse techniques. $t_W = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

TYPICAL APPLICATIONS

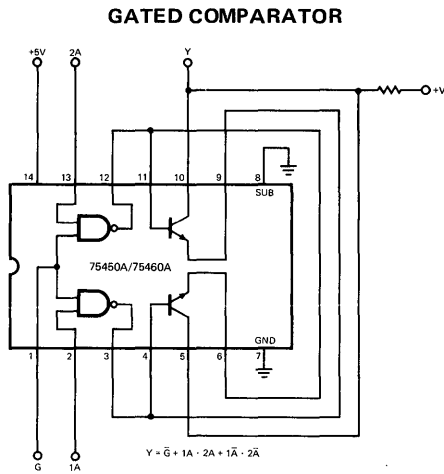


Fig. 19

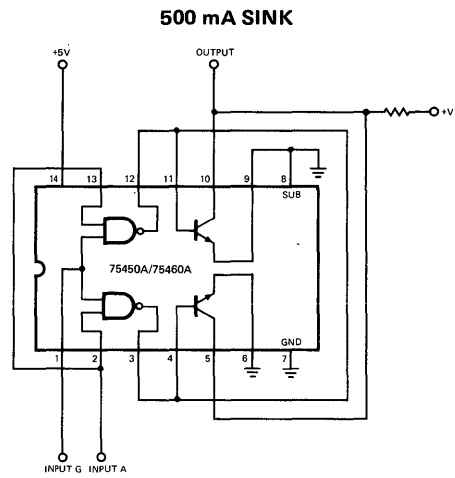


Fig. 20

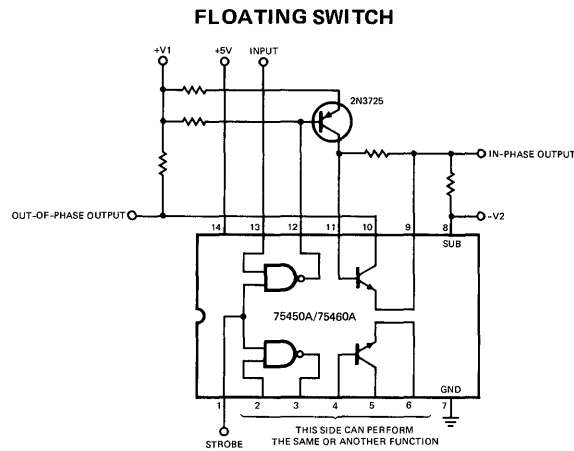


Fig. 21

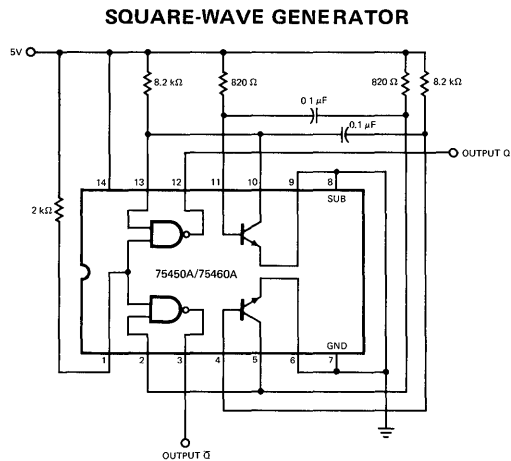
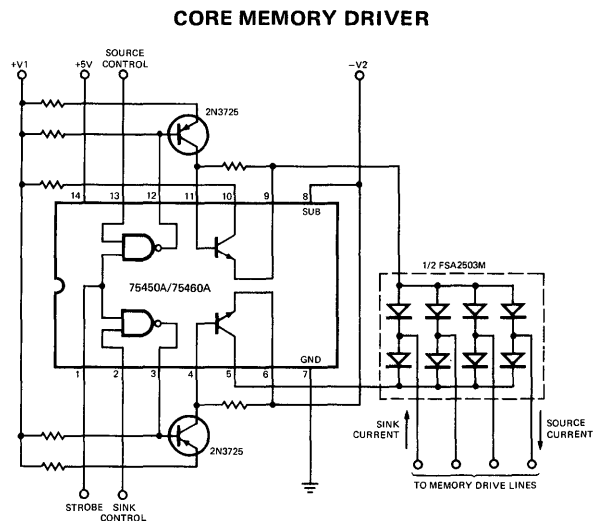


Fig. 22



Source and sink controls are activated by input HIGH voltages ($V_{IH} \geq 2V$).

Fig. 23

TYPICAL APPLICATIONS (Cont'd)

DUAL TTL-TO-MOS DRIVER

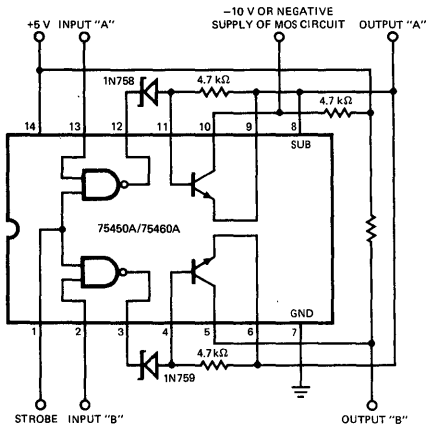


Fig. 24

DUAL MOS-TO-TTL DRIVER

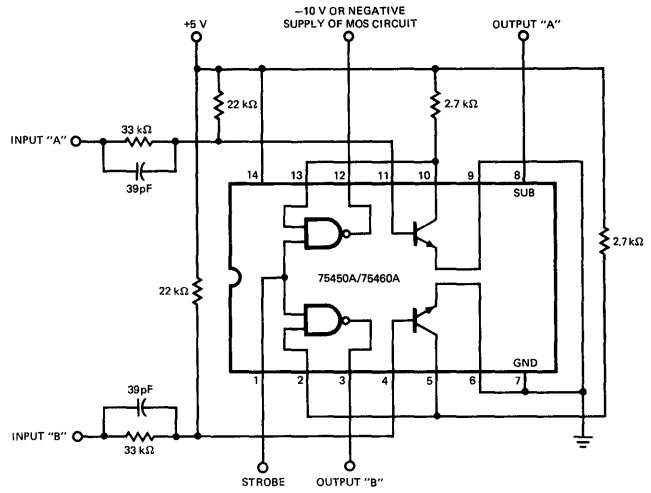
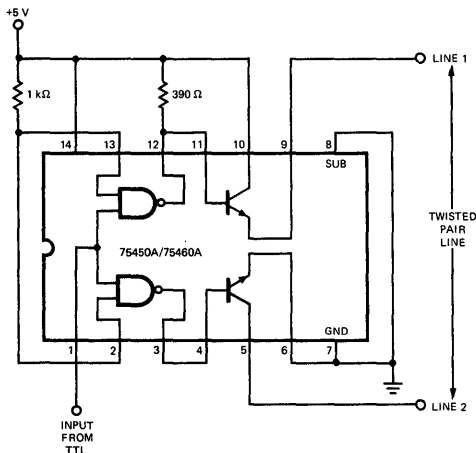


Fig. 25

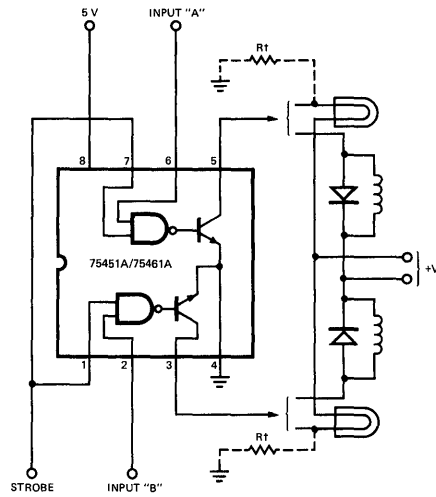
BALANCED LINE DRIVER



Termination is made at the receiving end as follows:
 Line 1 is terminated to ground through $Z_0/2$;
 Line 2 is terminated to +5 V through $Z_0/2$;
 where Z_0 is the line impedance.

Fig. 26

DUAL LAMP OR RELAY DRIVER



† Optional keep-alive resistors maintain off-state lamp current at $\approx 10\%$ to reduce surge current.
 Note: Clamp diodes across relay coils suppress reverse emf when relay is turned off.

Fig. 27

COMPLEMENTARY DRIVER

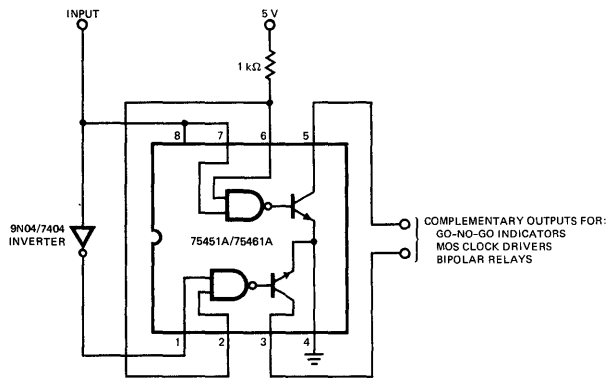


Fig. 28

TTL OR DTL POSITIVE LOGIC-LEVEL DETECTOR

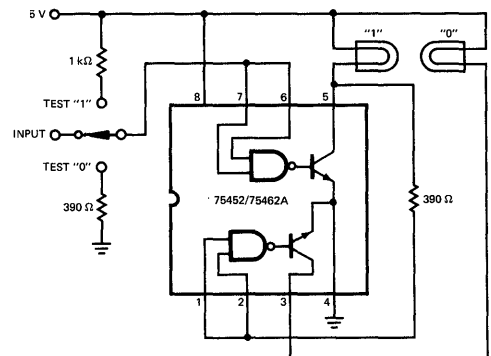
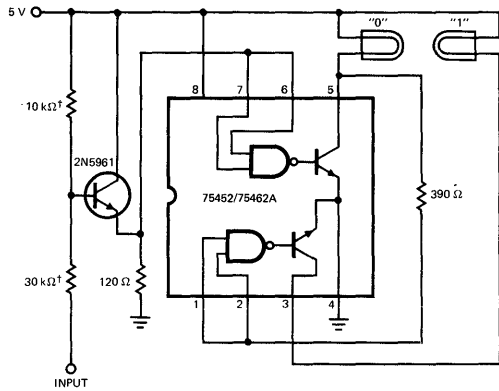


Fig. 29

TYPICAL APPLICATIONS (Cont'd)

MOS NEGATIVE-LOGIC-LEVEL DETECTOR



† The two input resistors must be adjusted for the level of MOS input.

Fig. 30

LOGIC SIGNAL COMPARATOR

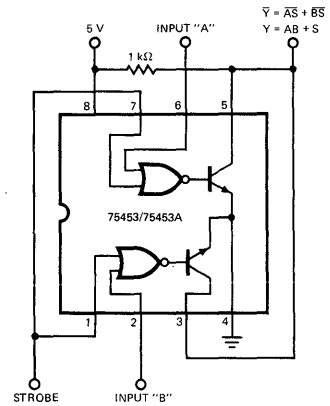
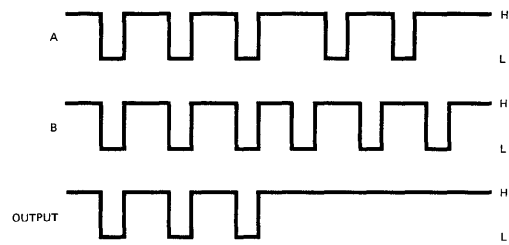
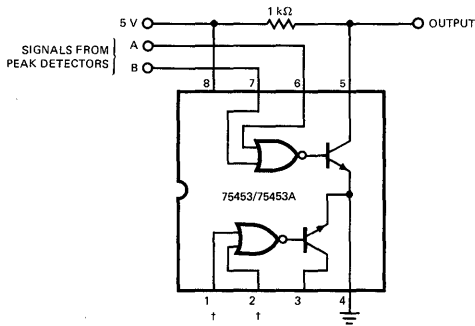


Fig. 31

IN-PHASE DETECTOR



Output LOW occurs only when inputs are low simultaneously.

† If inputs are unused, they should be connected to +5 V through a 1 kΩ resistor.

Fig. 32

MULTIFUNCTION LOGIC-SIGNAL COMPARATOR

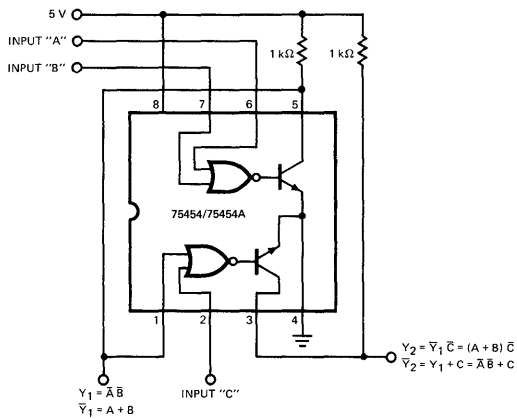
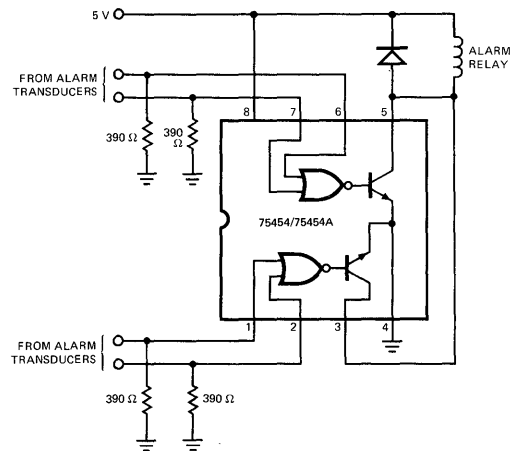


Fig. 33

ALARM DETECTOR



NOTE: 390 Ω resistors will increase sensitivity of inputs and consequently reduce the noise immunity of the device. The clamp diode across the relay coil suppresses the reverse emf of the relay coil when the relay is turned off.

Fig. 34

75491•75492

MOS TO LED SEGMENT AND DIGIT DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 75491 LED Quad Segment Driver interfaces MOS signals to common-cathode LED displays. High output current capability makes the device ideal in time multiplex systems using segment address or digit scan method of driving LED's to minimize the number of drivers required.

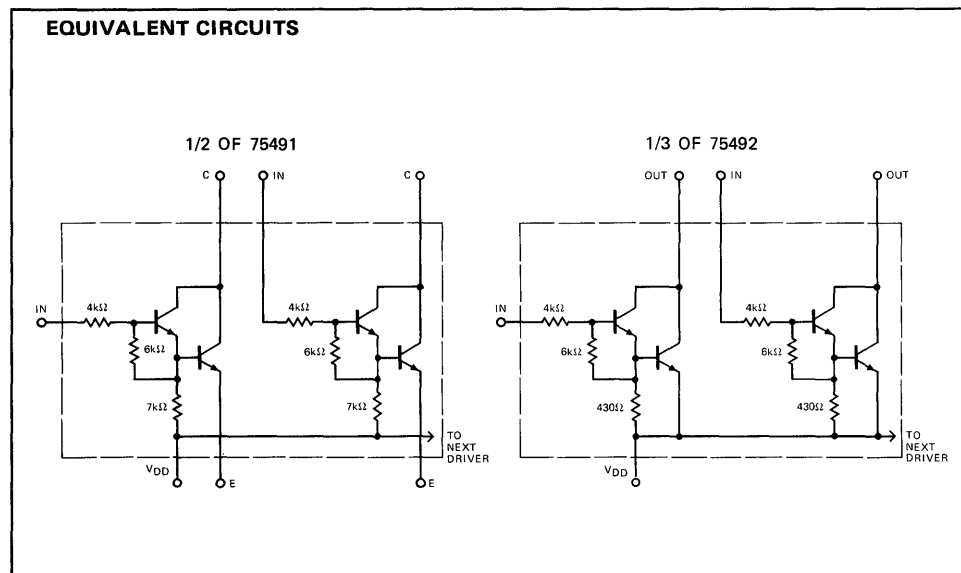
The 75492 Hex LED/Lamp Driver converts MOS signals to high output currents for LED display digit select or lamp select. The high output current capability makes the device ideal in time multiplex systems using segment address or digit scan method of driving LED's to minimize the number of drivers required.

74191

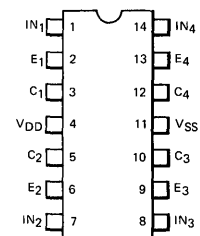
- 50mA SOURCE OR SINK CAPABILITY
- LOW INPUT CURRENTS FOR MOS COMPATIBILITY
- LOW STANDBY POWER
- FOUR HIGH GAIN DARLINGTON CIRCUITS

75492

- 250mA SINK CAPABILITY
- MOS COMPATIBLE
- LOW STANDBY POWER
- SIX HIGH GAIN DARLINGTON CIRCUITS



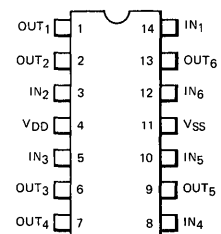
75491
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9A



ORDER INFORMATION

TYPE	PART NO.
75491	SN75491N

75492
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9A



ORDER INFORMATION

TYPE	PART NO.
75492	SN75492N

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75491 • 75492

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{SS} (Note 1)	10V
Input Voltage	V_{SS}
Collector Voltage (Note 2)	10V
Collector to Emitter Voltage (75491 Only)	10V
Collector to Input Voltage	10V
Emitter Voltage (75491 Only)	5.0V
Emitter to Input Voltage (75491 Only)	5.0V
V_{DD} to Input Voltage (Note 3)	5.0V
Continuous Collector Current	
75491	50 mA
75492	250 mA
Continuous V_{DD} Current (75492 Only)	600 mA
Continuous Total Power Dissipation	800 mW
Operating Temperature Range	0° C to 70° C
Storage Temperature Range	-55° C to +125° C
Lead Temperature (Soldering, 10 seconds)	260° C

NOTES

- V_{SS} terminal voltage is with respect to any other device terminal.
- Voltage values are with respect to V_{DD} terminal unless otherwise noted.
- With the exception of the inputs, the V_{DD} terminal must always be the most negative device voltage for proper operation.

75491 TRUTH TABLE

INPUT	OUTPUT E	OUTPUT C
L	L	H
H	H	L

75492 TRUTH TABLE

INPUT	OUTPUT
L	H
H	L

75491

ELECTRICAL CHARACTERISTICS ($V_{SS} = 10V$, unless otherwise specified)

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{CEL}	LOW Level Collector-to-Emitter Voltage	$V_{IN} = 8.5V$ through $1k\Omega$ $I_{OL} = 50mA$, $V_E = 5V$, $T_A = 25^\circ C$		0.9	1.2	V
		$V_{IN} = 8.5V$ through $1k\Omega$ $I_{OL} = 50mA$, $V_E = 5V$		0.9	1.5	V
I_{CH}	Collector HIGH Current	$V_{CH} = 10V$, $V_E = 0$, $I_{IN} = 40\mu A$			100	μA
		$V_{CH} = 10V$, $V_E = 0$, $V_{IN} = 0.7V$			100	μA
I_I	Input Current at Maximum Input Voltage	$V_{IN} = 10V$, $I_{OL} = 20mA$		2.0	3.0	mA
I_{ER}	Reverse Biased Emitter Current	$I_C = 0$, $V_{IN} = 0$, $V_E = 5V$			100	μA
I_{SS}	Supply Current				1.0	mA

AC CHARACTERISTICS ($V_{SS} = 7.5V$, $T_A = 25^\circ C$)

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
t_{PHL}	Propagation Delay Time	$R_L = 200\Omega$, $V_{IN} = 4.5V$		20		ns
t_{PLH}		$C_L = 15pF$, $V_E = 0$		100		ns

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 75491 • 75492

75492

ELECTRICAL CHARACTERISTICS ($V_{SS} = 10V$, unless otherwise specified)

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output LOW Voltage	$V_{IN} = 6.5V$ through $1k\Omega$ $I_{OL} = 250mA$, $T_A = 25^\circ C$		0.9	1.2	V
		$V_{IN} = 6.5V$ through $1k\Omega$ $I_{OL} = 250mA$		0.9	1.5	V
I_{OH}	Output HIGH Current	$V_{OH} = 10V$, $I_{IN} = 40\mu A$			200	μA
		$V_{OH} = 10V$, $V_{IN} = 0.5V$			200	μA
I_I	Input Current at Maximum Input Voltage	$V_{IN} = 10V$, $I_{OL} = 20mA$		2.0	3.0	mA
I_{SS}	Supply Current				1.0	mA

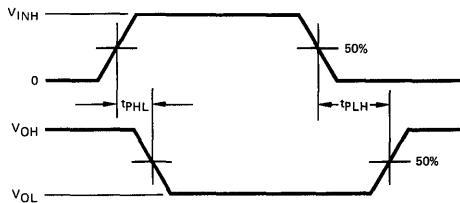
AC CHARACTERISTICS ($V_{SS} = 7.5V$, $T_A = 25^\circ C$)

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
t_{PHL}	Propagation Delay Time	$R_L = 39\Omega$, $V_{IN} = 7.5V$ $C_L = 15pF$		40		ns
t_{PLH}				600		ns

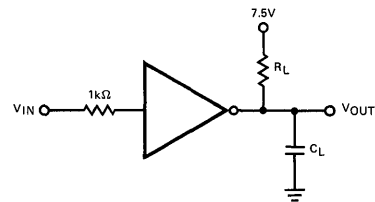
NOTE

All typical values are at $T_A = 25^\circ C$.

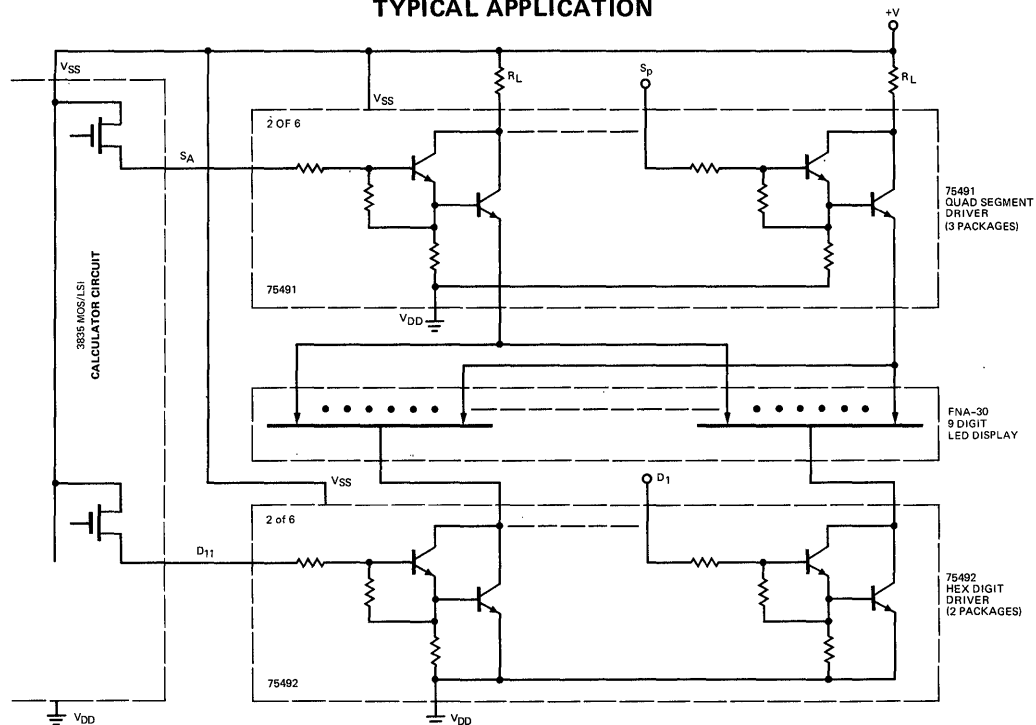
WAVEFORMS



TEST CIRCUIT



TYPICAL APPLICATION

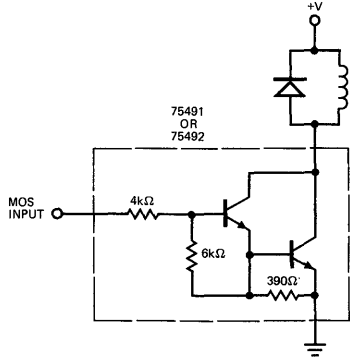


INTERFACING BETWEEN MOS CALCULATOR CIRCUIT AND LED MULTI-DIGIT DISPLAY

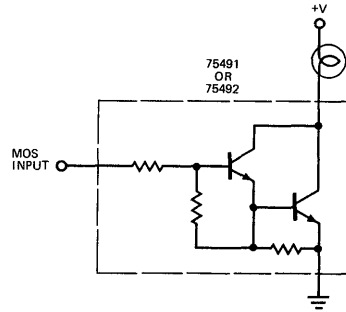
This example of time multiplexing the individual digits in a visible display minimizes display circuitry. Up to twelve digits of a seven-segment display plus decimal point may be displayed using only two 75491 and two 75492 drivers.

TYPICAL MOS INTERFACE APPLICATIONS

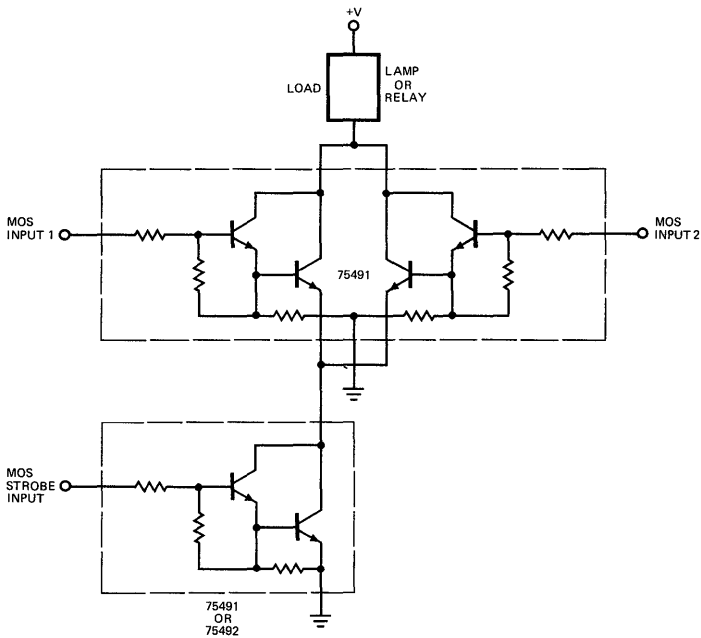
QUAD OR HEX
MOS RELAY DRIVER



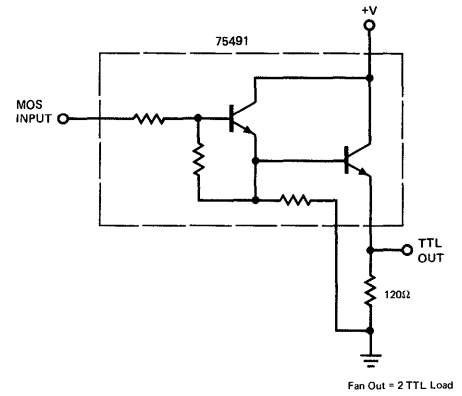
QUAD OR HEX
MOS LAMP DRIVER



MOS STROBED NOR DRIVER



MOS TO TTL LEVEL SHIFTER



Note: For the above applications, it is assumed that the ground pin on the 75491 is at the same potential as the most negative MOS power supply voltage.

8T13

DUAL SINGLE-ENDED LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 8T13 Dual Line Driver is designed for driving 50Ω to 500Ω coaxial cable, strip line, or twisted pair transmission lines. All inputs are TTL or DTL compatible and the emitter-follower outputs enable two or more drivers to operate on the same line in party line applications.

For a dual line driver to meet the IBM System/360 I/O Interface Specification, see 8T23 data sheet.

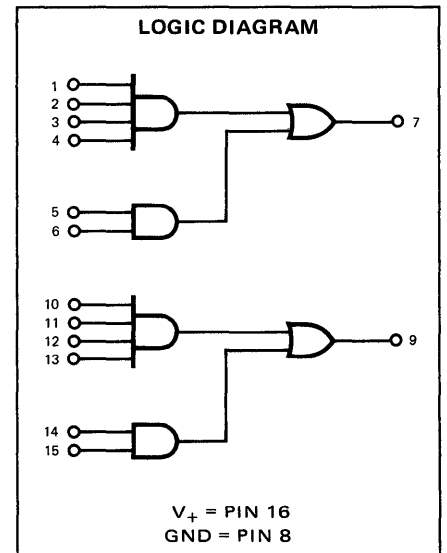
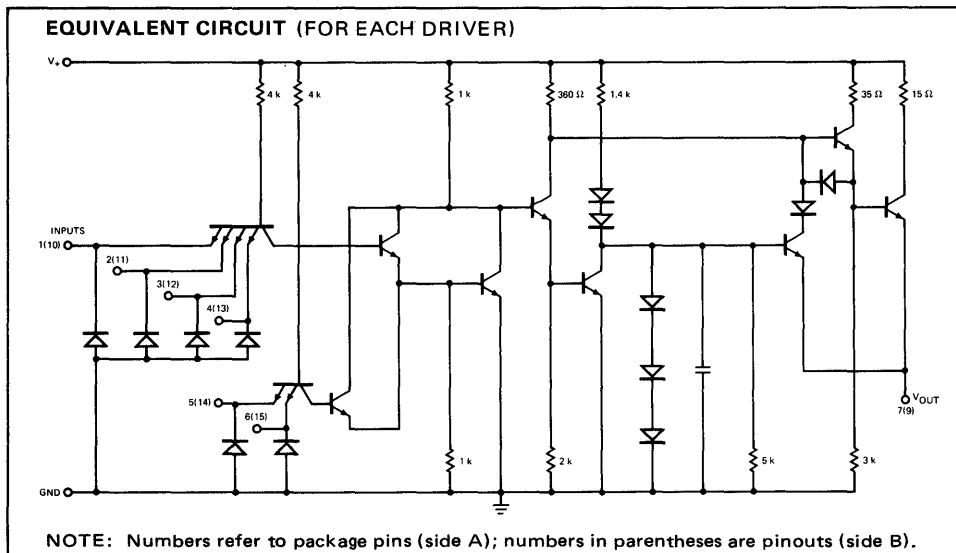
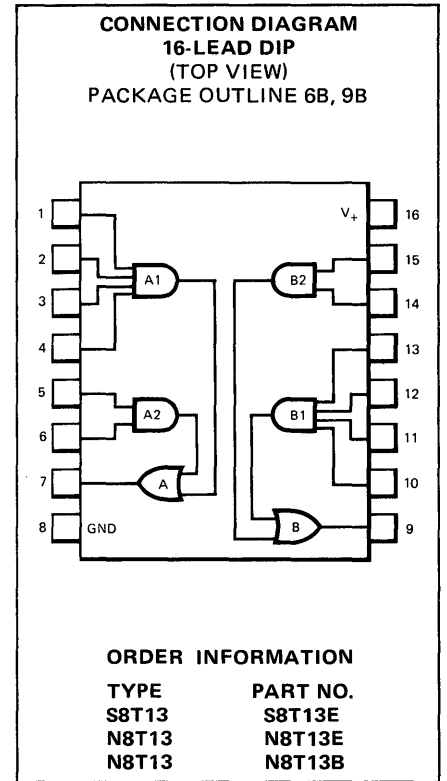
- HIGH OUTPUT DRIVE CAPABILITY
- HIGH SPEED
- INPUT CLAMP DIODES
- SINGLE 5 V SUPPLY OPERATION
- SHORT CIRCUIT PROTECTED

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	
Hermetic DIP (S8T13E, N8T13E)	-65° C to +150° C
Molded DIP (N8T13B)	-55° C to +125° C
Operating Temperature Range	
Military (S8T13)	-55° C to +125° C
Commercial (N8T13)	0° C to +75° C
Lead Temperatures	
Hermetic DIP (Soldering, 60 seconds)	300° C
Molded DIP (Soldering, 10 seconds)	260° C
Internal Power Dissipation (Note 2)	730 mW

NOTES:

1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 75° C. Above 75° C derate linearly at 8.3 mW/° C.



FAIRCHILD LINEAR INTEGRATED CIRCUIT • 8T13

ELECTRICAL CHARACTERISTICS FOR S8T13 ($V_+ = 5.0\text{ V} \pm 5\%$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (Note 3))

PARAMETER	TEST CONDITIONS				NOTES	LIMITS			UNITS
	AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN.	TYP.	MAX.	
	INPUT UNDER TEST	OTHER INPUTS							
Output HIGH Voltage	2.0 V	2.0 V	0.8 V	-75 mA	9	2.4			V
Output HIGH Leakage Current	0 V	0 V	0 V	3.0 V	10			500	μA
Output LOW Leakage Current	0.8 V	4.5 V	0 V	0.4 V				-800	μA
Input LOW Current	0.4 V	4.5 V				-0.1		-1.6	mA
Input HIGH Current	4.5 V	0 V						40	μA

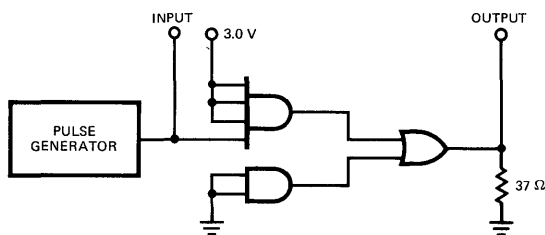
ELECTRICAL CHARACTERISTICS FOR S8T13 AND N8T13 ($V_+ = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$.)

PARAMETER	TEST CONDITIONS				NOTES	LIMITS			UNITS
	AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN.	TYP.	MAX.	
	INPUT UNDER TEST	OTHER INPUTS							
Turn On Delay, t_{PHH}					11, 15			20	ns
					12, 15		32		ns
Turn Off Delay, t_{PLL}					11, 15			20	ns
					12, 15		22		ns
Power/Current Consumption:									
Output LOW	0.8 V	0.8 V	0.8 V		14, 17			315/60	mW/mA
Output HIGH	2.0 V	2.0 V	2.0 V		14, 17			150/28	mW/mA
Input Latch Voltage	10 mA	0 V	0 V		13	5.5			V
Output HIGH Current	4.5 V	4.5 V	0 V	2.0 V	16	-100		-250	mA
Output Short Circuit	4.5 V	4.5 V	0 V	0 V	16			-30	mA
Input Clamp Diode Voltage	-12 mA							-1.5	V

NOTES:

3. Specifications apply $V_+ = 5.0\text{ V} \pm 5\%$ and 0°C to 75°C for N8T13.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. All measurements are taken with ground pin tied to zero volts.
6. Positive current is defined as into the terminal referenced.
7. Positive logic definition: "UP" Level = HIGH, "DOWN" Level = LOW.
8. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
9. Output source current is supplied through a resistor to ground.
10. With forced output voltage of 3 V no more than 500 μA will enter the driver when output is in LOW state. $V_+ = 0\text{ V}$.
11. $R_L = 37\ \Omega$ to ground.
12. Load is 37 Ω in parallel with 1000 pF.
13. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
14. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition.
15. Reference ac Test Figure and Pulse Requirements.
16. Reference "Typical Output Current as a function of Output Voltage Curve."
17. $V_+ = 5.25\text{ V}$. Power Consumption specified for both drivers in package.

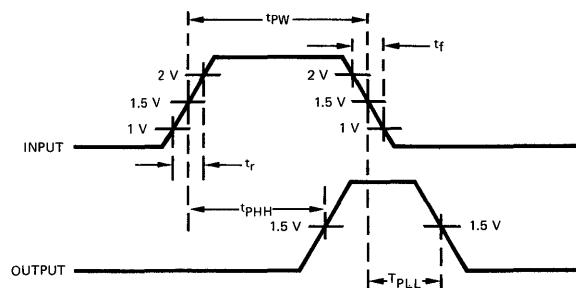
AC TEST CIRCUIT



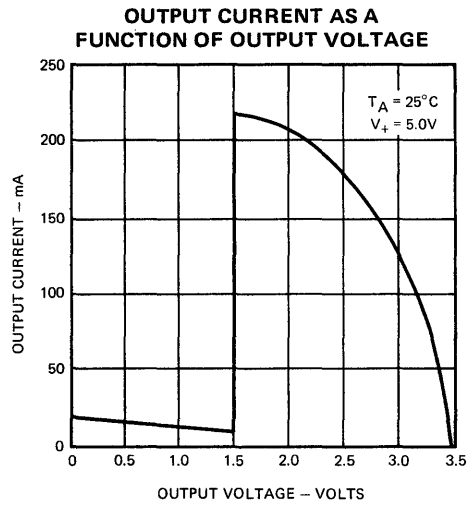
INPUT PULSE:

Amplitude = 3.0 V
 $t_{PW} = 40\text{ ns}$ (50% Duty Cycle)
 $t_r = t_f \leq 5\text{ ns}$ (10% and 90% measurement points)

VOLTAGE WAVEFORMS

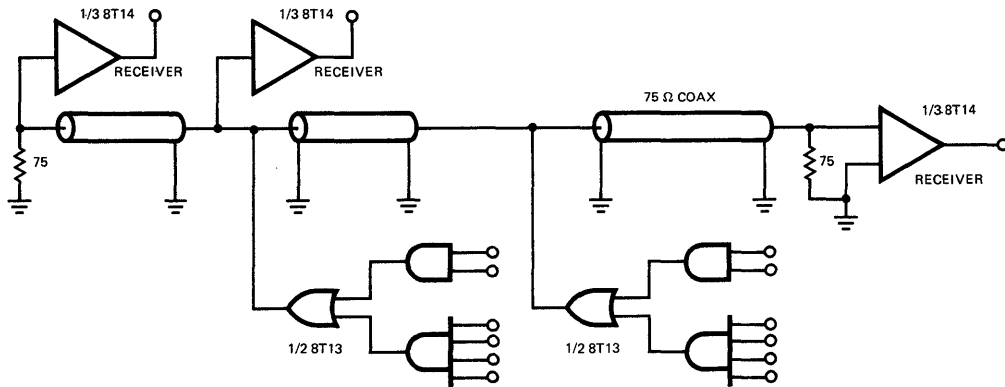


TYPICAL PERFORMANCE CURVE FOR S8T13 AND N8T13



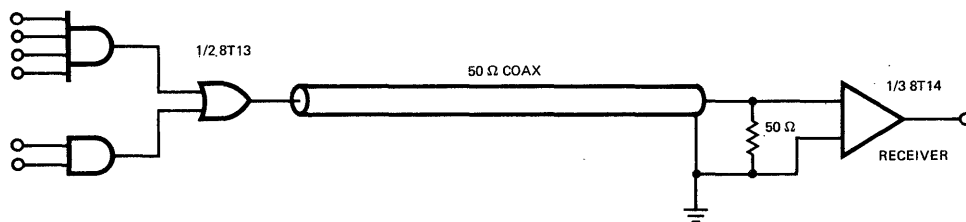
TYPICAL APPLICATIONS

75 Ω PARTY LINE (2 DRIVERS, 3 RECEIVERS)



Note: For party line operation, termination of each physical end of the line is recommended.

SIMPLEX OPERATION (1 DRIVER)



Note: For simplex operation, the line should be terminated only at the distant receiver site.

8T14

TRIPLE LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 8T14 Triple Line Receiver is designed to receive digital information from coaxial cable, strip line, or twisted pair single ended transmission lines. High input impedance ($\approx 30k\Omega$) presents minimal loading to the transmission lines in multiple receiver applications. The 8T14 has built in hysteresis which makes it ideal for such applications as Schmitt triggers, one-shots, and oscillators. Use the 8T24 triple line receiver where IBM System/360 I/O Interface Specification must be met.

- BUILT-IN INPUT THRESHOLD HYSTERESIS
- HIGH SPEED
- INDEPENDENT CHANNEL STROBING
- FANOUT OF 10 TTL LOADS
- SINGLE +5V SUPPLY OPERATION

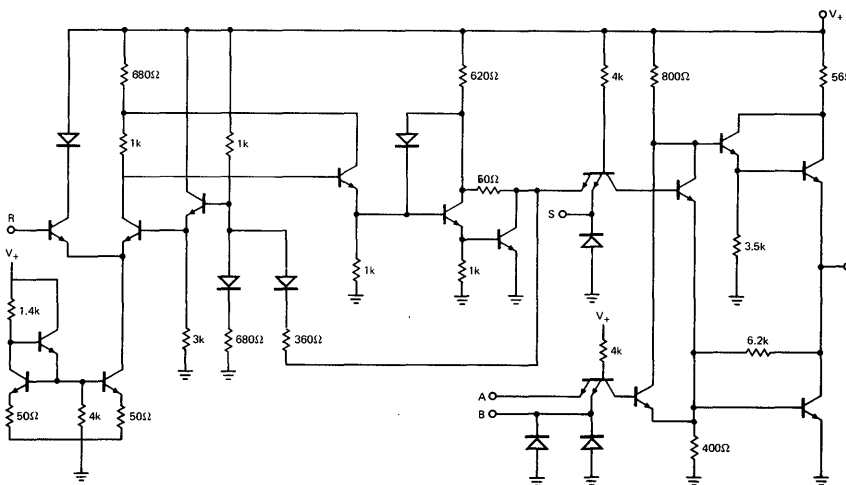
ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5V
Output Voltage (Note 1)	+7.0V
Supply Voltage (Note 1)	+7.0V
Storage Temperature Range	
Hermetic DIP (S8T14E, N8T14E)	-65°C to +150°C
Molded DIP (N8T14B)	-55°C to +125°C
Operating Temperature Range	
Military (S8T14)	-55°C to +125°C
Commercial (N8T14)	0°C to +75°C
Lead Temperatures	
Hermetic DIP (soldering, 60 seconds)	300°C
Molded DIP (soldering, 10 seconds)	260°C
Internal Power Dissipation (Note 2)	730mW

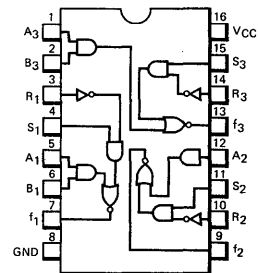
NOTES

1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3mW/°C.

EQUIVALENT CIRCUIT (EACH RECEIVER)



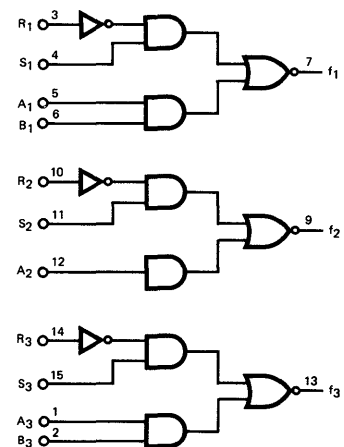
CONNECTION DIAGRAM
16-LEAD DIP
 (TOP VIEW)
 PACKAGE OUTLINE 6B, 9B



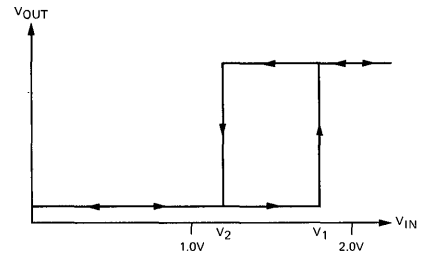
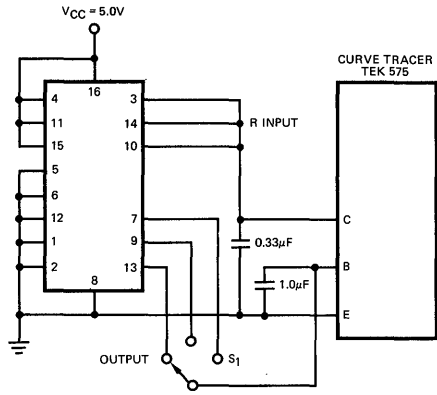
ORDER INFORMATION

TYPE	PART NO.
S8T14	S8T14E
N8T14	N8T14E
N8T14	N8T14B

LOGIC DIAGRAM



HYSTERESIS TEST CIRCUIT



Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Fig. 2.

- V_1 and V_2 must be between 0.8V minimum and 2.0V maximum.
- Hysteresis = $V_1 - V_2 \geq 0.3V$.

Fig. 1

Fig. 2

APPLICATIONS

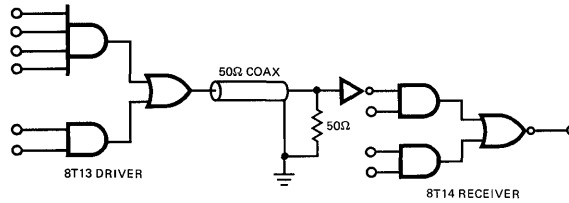
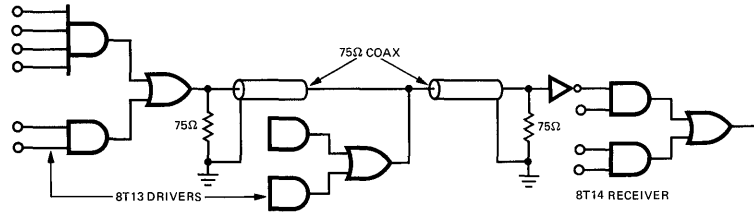


Fig. 3



If more than one driver/receiver pair is to be used on each transmission line, the line should be terminated at both ends as shown in Fig. 4

Fig. 4

SCHMITT TRIGGER APPLICATION

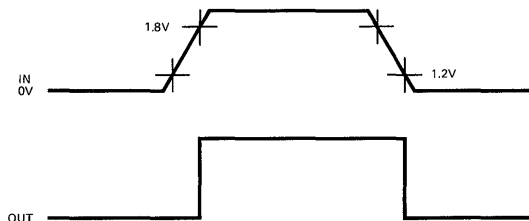
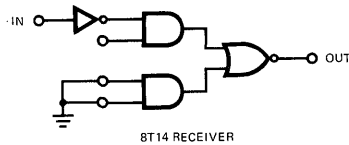


Fig. 5

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 8T14

ELECTRICAL CHARACTERISTICS ($V_+ = 5.0\text{ V} \pm 5\%$; $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ For S8T14 (Note 3))

PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
		R	S	A	B	OUTPUTS		MIN.	TYP.	MAX.	
Output HIGH Voltage		2.0V	4.5V	0V	0V	-800 μ A	10,16	2.6	3.5		V
		0V	0.8V	0V	0V	-800 μ A	10,16	2.6	3.5		V
Output LOW Voltage		0.8V	2.0V	0V	0V	16mA	11,15			0.4	V
		0V	0V	2.0V	2.0V	16mA	11,15			0.4	V
Input LOW Current	S _n	0V	0.4V					-0.1		-1.6	mA
	A _n	0V		0.4V				-0.1		-1.6	mA
	B _n				0.4V			-0.1		-1.6	mA
Input HIGH Current	R _n	3.8V								0.17	mA
	S _n	3.8V	4.5V							40	μ A
	A _n			4.5V	0V					40	μ A
	B _n			0V	4.5V					40	μ A
Hysteresis			4.5V	0V	0V		13,14	0.30	0.50		V

NOTE

3. Specifications apply from 0° C to + 75° C for N8T14.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_+ = 5.0\text{V}$)

PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
		R	S	A	B	OUTPUTS		MIN.	TYP.	MAX.	
Turn-on Propagation Delay t _{PHH}		V _{IN}	5.0V	0V	0V		18		20	30	ns
Turn-off Propagation Delay t _{PLL}		V _{IN}	5.0V	0V	0V		18		20	30	ns
Power/Current Consumption									315/60	380/72	mW/mA
Input Voltage Rating	S _n	3.8V	10mA	0V	0V			5.5			V
	A _n	0V	0V	10mA	0V			5.5			V
	B _n	0V	0V	0V	10mA			5.5			V
Output Short-Circuit Current		3.8V	0V	0V	0V	0V		-50		-100	mA
Input Clamp Voltage	S _n		-12mA							-1.5	V
	A _n			-12mA						-1.5	V
	B _n				-12mA					-1.5	V

NOTES

4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. All measurements are taken with ground pin tied to zero volts.
6. Positive current is defined as into the terminal referenced.
7. Positive current flow is defined as into the terminal referenced.
8. Positive Logic Definition: "UP" Level = "HIGH"; "DOWN" Level = "LOW".
9. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the clamp diodes on the S, A, and B inputs become forward biased.
10. Output source current is supplied through a resistor to ground.
11. Output sink current is supplied through a resistor to V_{CC}.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Hysteresis is defined as voltage difference between R input level at which output begins to go from LOW to HIGH state and level at which output begins to go from HIGH to LOW.
14. V₊ = 5.0V.
15. Previous condition is a HIGH output state.
16. Previous condition is a LOW output state.
17. V₊ = 5.25V.
18. Measured as time delay from R input going through 1.5V to the output going through 1.5V. (See 8T24 data sheet ac test circuit).

8T23

DUAL SINGLE-ENDED LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 8T23 Dual Line Driver is designed to meet the requirements of the IBM System/360 I/O Interface Specification for interface drivers. All inputs are TTL or DTL compatible. Logic has been incorporated to ensure that no spurious noise is generated on the transmission line during the power-up and power-down sequence. The outputs are protected from short circuits and have uncommitted emitter outputs which allows DOT-OR logic to be performed in party line data bus applications.

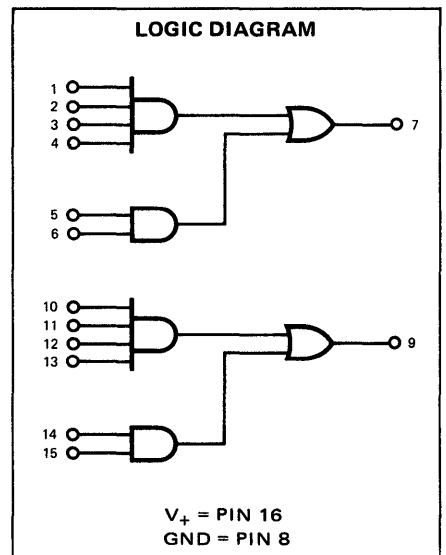
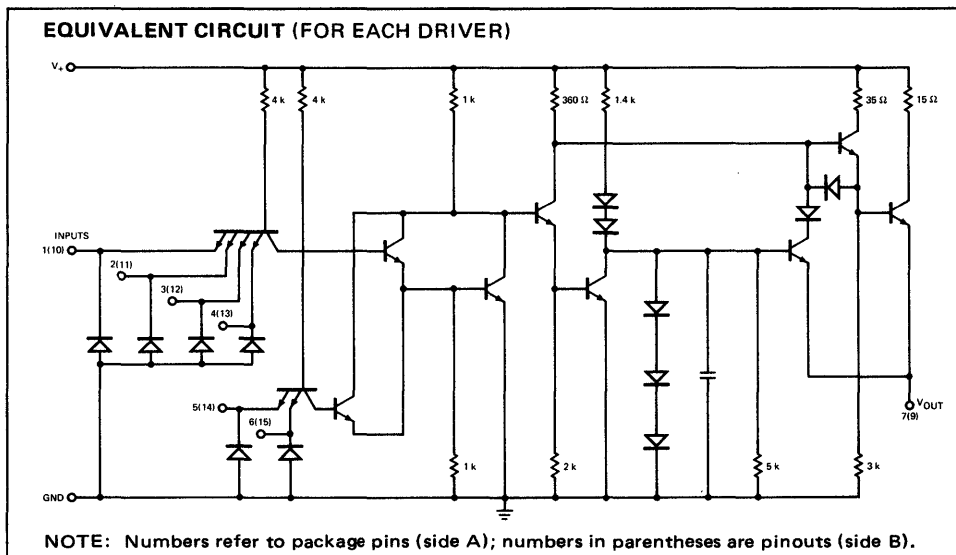
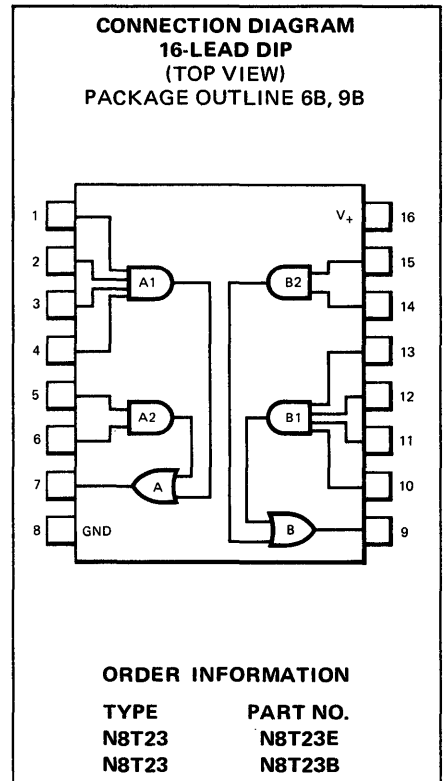
- $I_{OUT} = 59.3 \text{ mA AT } 3.11 \text{ V}$
- **UNCOMMITTED EMITTER OUTPUTS FOR PARTY LINE/WIRED-OR APPLICATIONS**
- **SHORT CIRCUIT PROTECTION**
- **SINGLE 5 V SUPPLY OPERATION**
- **AND-OR LOGIC CONFIGURATION**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	
Hermetic DIP (N8T23E)	-65° C to +150° C
Molded DIP (N8T23B)	-65° C to +125° C
Operating Temperature Range	0° C to +75° C
Lead Temperatures	
Hermetic DIP (Soldering, 60 seconds)	300° C
Molded DIP (Soldering, 10 seconds)	260° C
Internal Power Dissipation (Note 2)	730 mW

NOTES:

1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 70° C. Above 70° C derate linearly at 8.3 mW/° C.



FAIRCHILD LINEAR INTEGRATED CIRCUIT • 8T23

ELECTRICAL CHARACTERISTICS FOR N8T23 ($V_+ = 5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C}$ to $+75^\circ \text{C}$.)

CHARACTERISTICS	TEST CONDITIONS				NOTES	LIMITS			UNITS
	AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN.	TYP.	MAX.	
	INPUT UNDER TEST	OTHER INPUTS							
Output LOW Voltage	0.8 V	4.5 V	0 V	$-240 \mu\text{A}$	9			+0.15	V
Output HIGH Leakage Current	0 V	0 V	0 V	3.0 V	3, 16			40	μA
Input LOW Current	0.4 V	4.5 V				-0.1		-1.6	mA
Input HIGH Current	4.5 V	0 V						40	μA

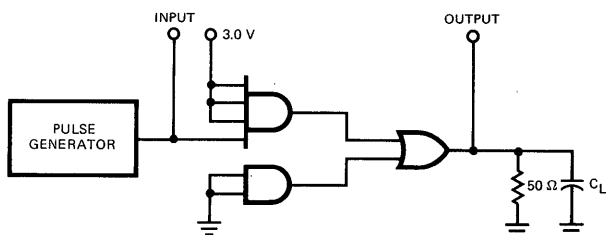
ELECTRICAL CHARACTERISTICS FOR N8T23 ($V_+ = 5.0 \text{ V}$, $T_A = 25^\circ \text{C}$.)

CHARACTERISTICS	TEST CONDITIONS				NOTES	LIMITS			UNITS
	AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN.	TYP.	MAX.	
	INPUT UNDER TEST	OTHER INPUTS							
Output HIGH Voltage	2.0 V	2.0 V	0.8 V	59.3 mA		3.11			V
Turn-On Delay t_{PHH}					10, 14 11, 14		12 15	20 25	ns
Turn-Off Delay t_{PLL}					10, 14 11, 14		12 20	20 35	ns
Power/Current Consumption:									
Output LOW	0.8 V	0.8 V	0.8 V		13, 17			315/60	mW/mA
Output HIGH	2.0 V	2.0 V	2.0 V		13, 17			150/28	mW/mA
Input Latch Voltage	10 mA	0 V	0 V		12	5.5			V
Output HIGH Current	4.5 V	4.5 V	0 V	2.0 V	15	-100		-250	mA
Input Clamp Diode Voltage	-12 mA				15			-1.5	V

NOTES:

3. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
4. All measurements are taken with ground pin tied to zero volts.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: "UP" Level = HIGH, "DOWN" Level = LOW.
7. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
8. Output source current is supplied through a resistor to ground.
9. With forced output current of $240 \mu\text{A}$ the output voltage must not exceed 0.15 V.
10. $R_L = 50 \Omega$ to ground.
11. Load is 50Ω in parallel with 100 pF .
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. I_+ is dependent upon loading. I_+ limit specified is for no-load test condition for both drivers.
14. Reference ac Test Circuit and Pulse Requirements.
15. Reference "Typical Output Current as a function of Output Voltage Curve".
16. $V_+ = 0 \text{ V}$.
17. $V_+ = 5.25 \text{ V}$.

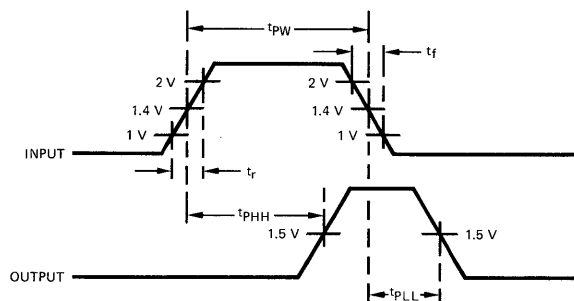
AC TEST CIRCUIT



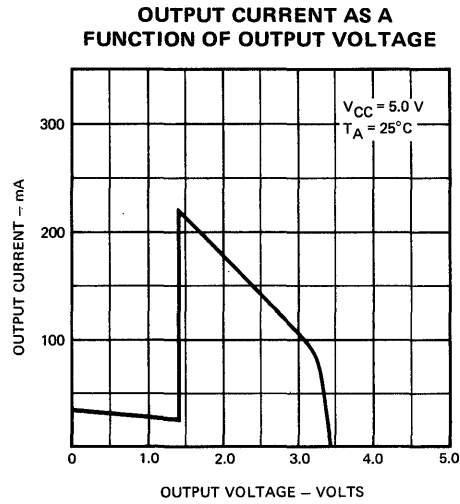
INPUT PULSE:

- Amplitude = 3.0 V
- $t_{PW} = 50 \text{ ns}$ (50% Duty Cycle)
- $t_r = t_f \leq 5 \text{ ns}$ (10% and 90% measurement points)

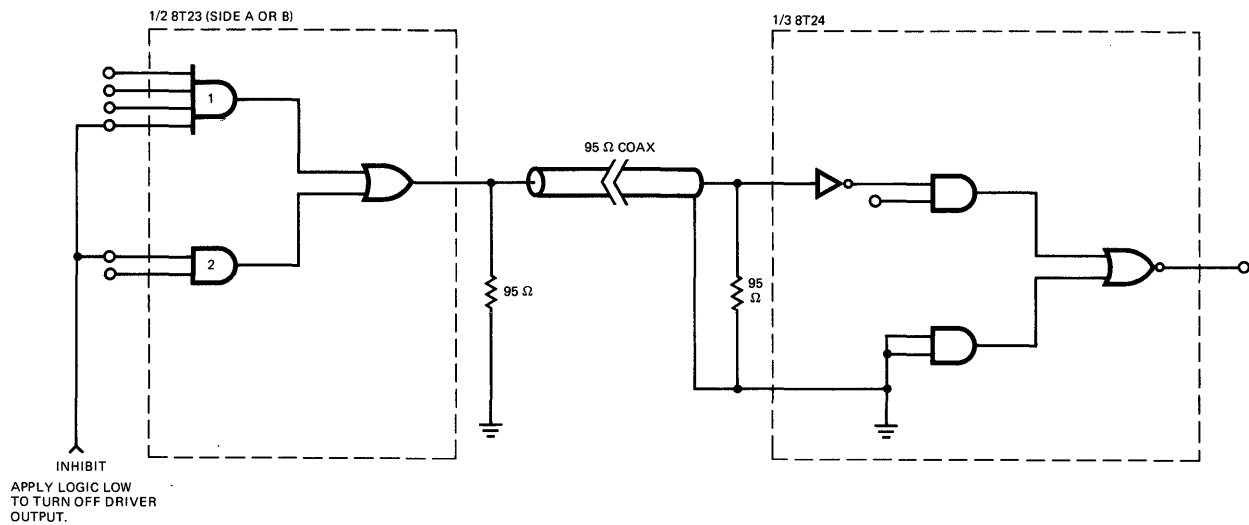
WAVEFORMS



TYPICAL PERFORMANCE CURVE FOR N8T23



TYPICAL APPLICATION



NOTE: To insure proper logic operation, unused inputs should not be left floating. Tie the unused inputs to V_{+} through a current limit resistor (2.2k Ω).
To inhibit the driver, apply a logic LOW voltage to one input from gate 1 and 2 as shown above.

8T24

TRIPLE LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 8T24 Triple Line Receiver is designed specifically to meet the IBM System/360 I/O Interface Specification (File No. S360-19). The logic inputs (S, A, B) are fully TTL or DTL compatible. The R (Receive) input is designed to withstand a positive dc input of +7 V with power on ($V_+ = 5\text{ V}$) and +6 V with power off, $V_+ = 0\text{ V}$) and a negative dc input of 0.15 V with power on or off. This protection allows normal bus operation even if one or more receivers have been powered down.

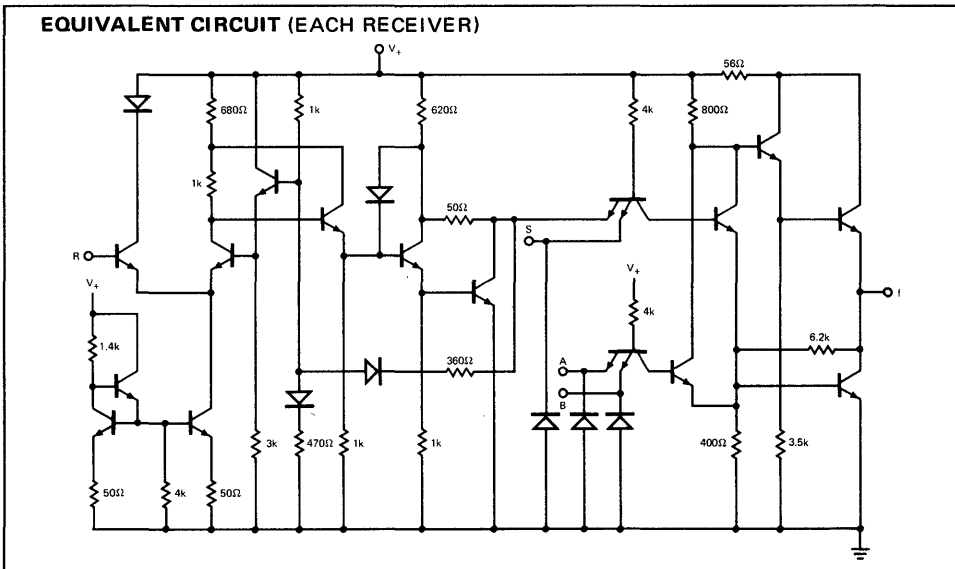
- MEETS IBM SYSTEM/360 I/O INTERFACE SPECIFICATION
- BUILT-IN INPUT THRESHOLD HYSTERESIS
- HIGH SPEED
- INDEPENDENT CHANNEL STROBING
- FANOUT OF 10 TTL LOADS
- SINGLE +5V SUPPLY OPERATION

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5V
Output Voltage (Note 1)	+7.0V
Supply Voltage (Note 1)	+7.0V
Storage Temperature Range	
Molded DIP (N8T24B)	-55°C to +125°C
Hermetic DIP (N8T24E)	-65°C to +150°C
Operating Temperature Range	0°C to +75°C
Lead Temperatures	
Hermetic DIP (soldering, 60 seconds)	300°C
Molded DIP (soldering, 10 seconds)	260°C
Internal Power Dissipation (Note 2)	730mW

NOTES:

1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3mW/°C.



CONNECTION DIAGRAM
16-LEAD DIP
 (TOP VIEW)
 PACKAGE OUTLINE 6B, 9B

ORDER INFORMATION

TYPE	PART NO.
N8T24	N8T24E
N8T24	N8T24B

LOGIC DIAGRAM

PIN 8 = GND
 PIN 16 = V₊

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 8T24

ELECTRICAL CHARACTERISTICS ($V_+ = 5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +75^\circ\text{C}$)

PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
		R	S	A	B	OUTPUTS		MIN.	TYP.	MAX.	
Output HIGH Voltage		1.70V	4.5V	0V	0V	-800 μ A	8	2.6	3.4		V
		0V	0.7V	0V	0V	-800 μ A	8	2.6	3.4		V
Output LOW Voltage		0.70V	1.7V	0V	0V	16mA	9		0.2	0.4	V
		0V	0V	1.7V	1.7V	16mA	9		0.2	0.4	V
Input LOW Current	S _n	0V	0.4V					-0.1		-1.6	mA
	A _n	0V		0.4V				-0.1		-1.6	mA
	B _n				0.4V			-0.1		-1.6	mA
Input HIGH Current	R _n	3.11V								0.17	mA
	R _n	7.0V								5.0	mA
	R _n	6.0V					10			5.0	mA
	S _n	3.11V	4.5V							40	μ A
	A _n			4.5V	0V					40	μ A
	B _n			0V	4.5V					40	μ A

ELECTRICAL CHARACTERISTICS ($V_+ = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)

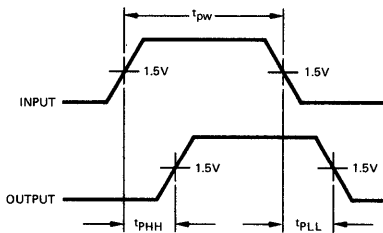
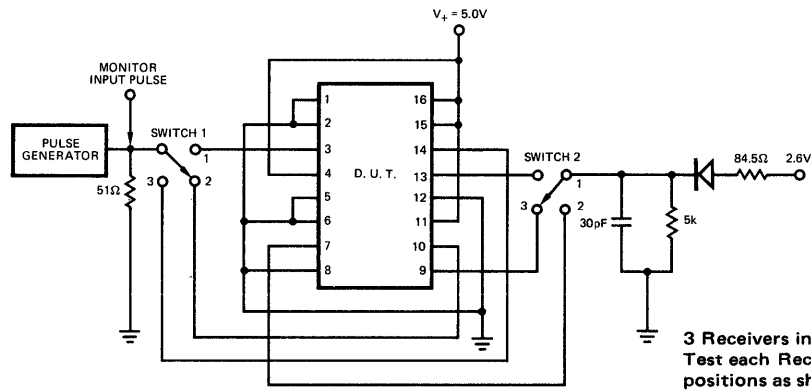
PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
		R	S	A	B	OUTPUTS		MIN.	TYP.	MAX.	
Turn-on Propagation Delay t _{PHH}		V _{IN}	5.0V	0V	0V		14		20	30	ns
Turn-off Propagation Delay t _{PLL}		V _{IN}	5.0V	0V	0V		14		20	30	ns
Hysteresis		V _{IN}	4.5V	0V	0V		12,13	0.2	0.4		V
Power/Consumption							15		315	380	mW
Supply Current							15		60	72	mA
Input Latch Voltage	S _n	3.11V	10mA	0V	0V		11	5.5			V
	A _n	0V	0V	10mA	0V		11	5.5			V
	B _n	0V	0V	0V	10mA		11	5.5			V
Output Short Circuit Current		3.11V	0V	0V	0V			-50		-100	mA
Input Clamp Diode Voltage	S _n		-12mA							-1.5	V
	A _n			-12mA						-1.5	V
	B _n				-12mA					-1.5	V

NOTES:

3. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
4. All measurements are taken with ground pin tied to zero volts.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: "UP" Level = "HIGH", "DOWN" Level = "LOW".
7. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
8. Output source current is applied through a resistor to ground.
9. Output sink Current is supplied through a resistor to V₊.
10. V₊ = 0.00V
11. This test guarantees operation free of Input latch up over the specified operating supply voltage range.
12. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "HIGH" to "LOW" state and the level at which the output begins to go from HIGH to LOW.
13. See Hysteresis test circuit.
14. Refer to AC test circuits.
15. V₊ = 5.25V.

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 8T24

AC TEST CIRCUIT AND WAVEFORMS



Input Pulse:
 Amplitude = 2.6V
 Pulse width = 200ns
 (50% Duty Cycle)
 $t_r = t_f = 5\text{ ns}$ (10% to 90%)

TABLE 1		
Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

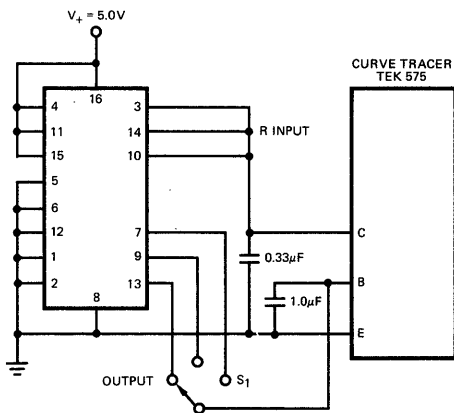


Fig. 1

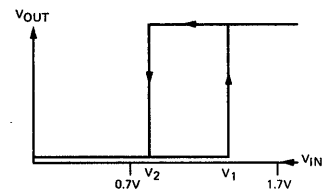
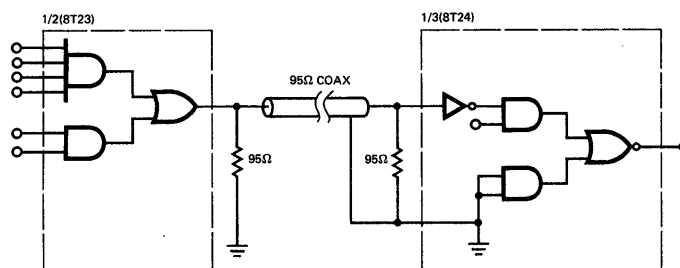


Fig. 2

Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Fig. 2.

1. V_1 and V_2 must be between 0.7V minimum and 1.7V maximum.
2. Hysteresis = $V_1 - V_2$

TYPICAL APPLICATION



SH0013

2-PHASE MOS CLOCK DRIVERS

FAIRCHILD INTEGRATED MICROSYSTEM CIRCUIT

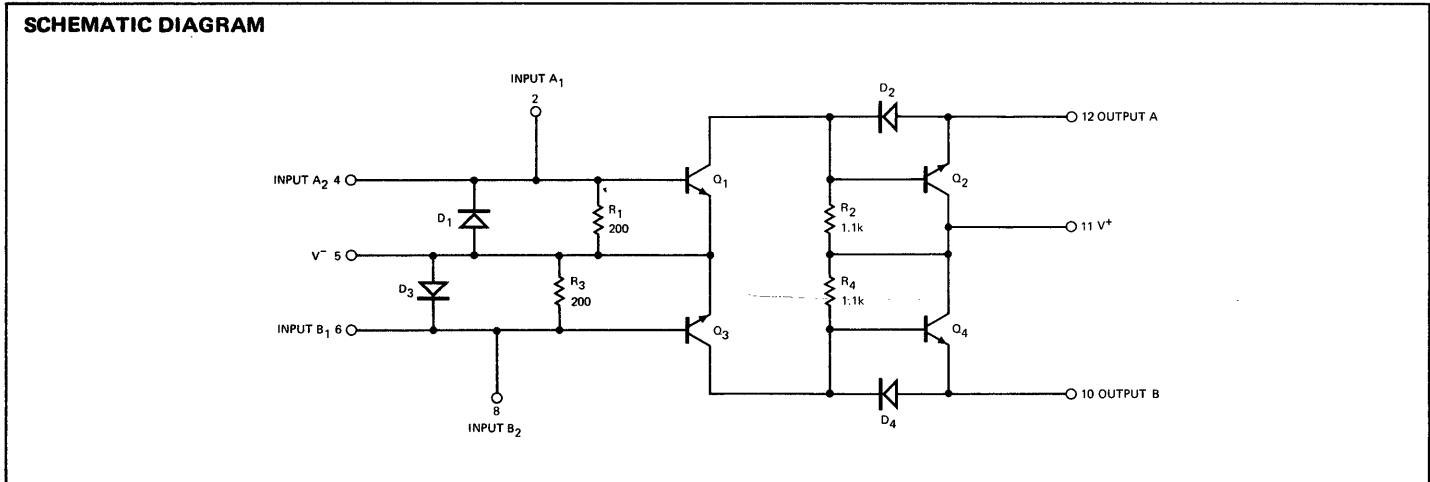
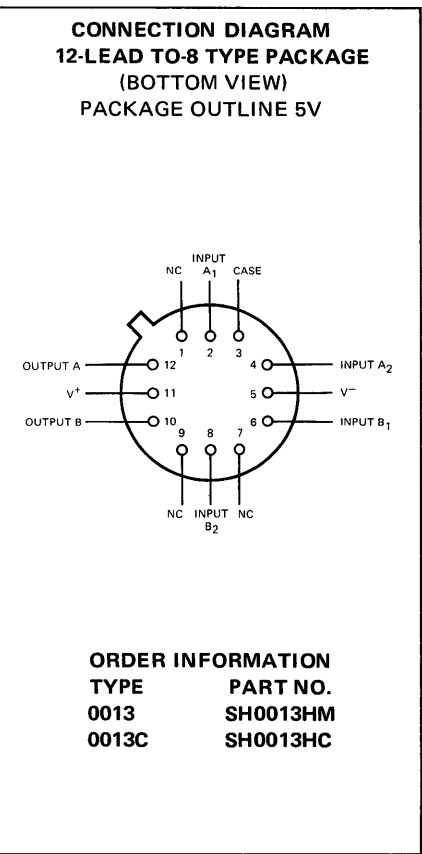
GENERAL DESCRIPTION – THE SH0013, designed for driving 2-phase MOS clock lines, is a dual high voltage driver capable of driving large capacitive loads at computer speeds. The SH0013 was designed to be driven by TTL circuits having moderate output current capability, such as TTL buffers (9009, 9N40, 9H40, 9S40) or TTL line drivers (9614). The circuit may also be driven by standard TTL circuits, such as the 9002, with slight degradation in rise time. Capacitive coupling from the driving TTL circuitry to the SH0013 provides independent fixed width output pulses. DC level shifting may also be employed and is especially simple for +5V, -12V MOS systems.

The device is supplied in a 12-pin TO-8 type package, capable of dissipating 1.0 W at 70°C or 0.5 W at 125°C. Use of an efficient fin radiator extends allowable dissipation to 1.66 W at 70°C or 0.8 W at +125°C.

- 30 V OUTPUT VOLTAGE SWING
- ±600 mA OUTPUT CURRENT CAPABILITY
- 5 MHz REPETITION RATE
- CAPACITIVE LEVEL SHIFTING
- INDEPENDENT FIXED WIDTH OUTPUT PULSES
- "ZERO" QUIESCENT POWER DISSIPATION

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Difference (Pin 11 to Pin 5)	30V
Input Current (Pins 2, 4, 6, 8)	±75 mA
Peak Output Current (Pins 10, 12)	±600 mA
Power Dissipation at 25°C (No Heat-Sink – See Figure 10)	1.5 W
Storage Temperature	-65°C to +150°C
Operating Temperature	
Military (SH0013M)	-55°C to +125°C
Commercial (SH0013C)	0°C to +85°C
Lead Temperature (1/16" from case for 60 seconds)	300°C



FAIRCHILD INTEGRATED MICROSYSTEM CIRCUITS • SH0013

ELECTRICAL CHARACTERISTICS (Note 1) (Figures 14, 16)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output LOW Voltage	$I_{OUT} = -50 \text{ mA}$ $I_{IN} = 1 \text{ mA}$	$V^+ - 3.0$	$V^+ - 1.0$		V
	$I_{OUT} = -100 \mu\text{A}$ $I_{IN} = 1 \text{ mA}$	$V^+ - 0.9$	$V^+ - 0.7$		V
Output HIGH Voltage	$I_{OUT} = 50 \text{ mA}$ $I_{IN} = 10 \text{ mA}$		$V^- + 1.5$	$V^- + 2.0$	V
	$I_{OUT} = 100 \mu\text{A}$ $I_{IN} = 10 \text{ mA}$		$V^- + 0.7$	$V^- + 0.9$	V
Power Supply Leakage Current	$V^+ - V^- = 30 \text{ V}$ $I_{OUT} = I_{IN} = 0$		<1.0	100	μA
Negative Input Voltage Clamp	$I_{IN} = -10 \text{ mA}$	$V^- - 1.2$	$V^- - 0.7$		V
$t_d(\text{on})$			15	30	ns
t_{rise} (Note 3)			35	50	ns
$t_d(\text{off})$ (Note 2)	$C_{IN} = 2200 \text{ pF}$ $R_{IN} = 0$		15	30	ns
t_{fall} (Note 2)	$V^+ - V^- = 20 \text{ V}$	40	50	80	ns
t_{fall} (Note 3)	$C_L = 1000 \text{ pF}$	40	70	120	ns
t_{pw}		340	420	490	ns
t_{rise}	$C_{IN} = 500 \text{ pF}$ $R_{IN} = 0$		15		ns
t_{fall}	$V^+ - V^- = 20 \text{ V}$		20		ns
t_{pw}	$C_L = 200 \text{ pF}$		110		ns
Positive Output Swing	$I_{OUT} = 0$		$V^+ - 0.7$		V
Negative Output Swing			$V^- + 0.7$		V

NOTES:

- (1) $V_+ = 20 \text{ V}$, $V_- = 0 \text{ V}$ unless otherwise specified. Typical values are for 25°C ; minimum and maximum values are for $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for 0013C, and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for the 0013M.
- (2) Values shown are for output pulse width determined by input pulse width (Fig. 16, $V_{IN} 2$).
- (3) Output rise and fall times vary depending upon input capacitance and resistance. Refer to Figures 7 and 8.

TABLE 1. TYPICAL DRIVE CAPABILITY OF SH0013 DRIVEN BY 9614 at 70°C ambient (No Heat Sink)

$V_+ - V_-$	FREQUENCY 50% DUTY CYCLE	PULSE WIDTH	R_{IN}	C_{IN}	C_L (MAX)	RISE TIME (MIN)
28V	4 MHz	100 ns	0	700 pF	50 pF	7 ns
20V					200 pF	
16V					350 pF	
28V	2 MHz	200 ns	10Ω	1800 pF	100 pF	5 ns
20V					400 pF	14 ns
16V					700 pF	19 ns
28V	1 MHz	200 ns	0	2300 pF	400 pF	19 ns
20V					1000 pF	34 ns
16V					1700 pF	45 ns
28V	0.5 MHz	500 ns	10Ω	4800 pF	2800 pF	130 ns
20V					5500 pF	183 ns
16V					9300 pF	248 ns

PERFORMANCE CURVES

Fig. 1 PULSE WIDTH AS A FUNCTION OF R_{IN} AND C_{IN} FOR SH0013 AND 9614 LINE DRIVER

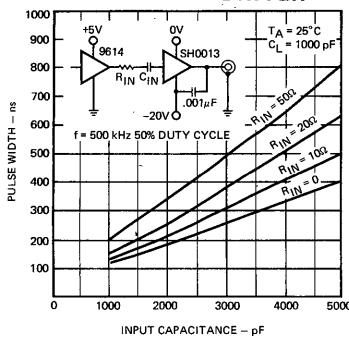


Fig. 2 PULSE WIDTH AS A FUNCTION OF R_{IN} AND C_{IN} FOR SH0013 AND 9009 DUAL BUFFER

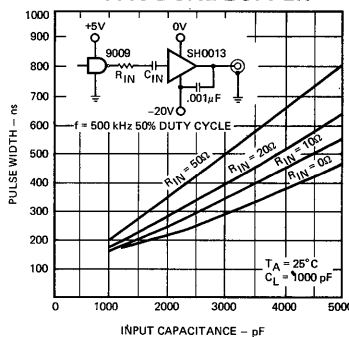
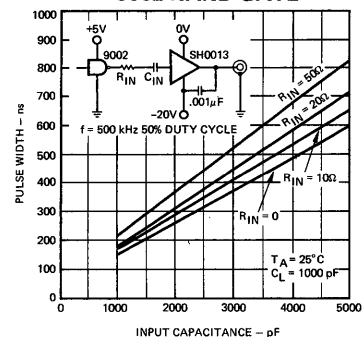


Fig. 3 PULSE WIDTH AS A FUNCTION OF R_{IN} AND C_{IN} FOR SH0013 AND 9002 NAND GATE



PERFORMANCE CURVES (Cont'd)

Fig. 4 PULSE WIDTH AS A FUNCTION OF AMBIENT TEMPERATURE

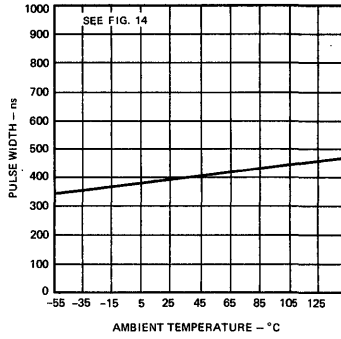


Fig. 5 PULSE WIDTH AS A FUNCTION OF TTL SUPPLY VOLTAGE

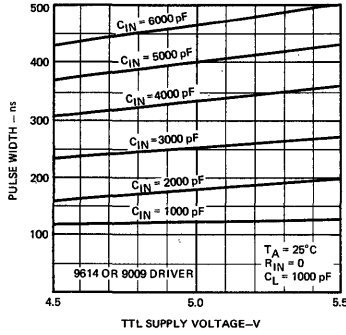


Fig. 6 ABSOLUTE MINIMUM RISE/FALL TIME AS A FUNCTION OF OUTPUT LOAD CAPACITANCE AND VOLTAGE SWING

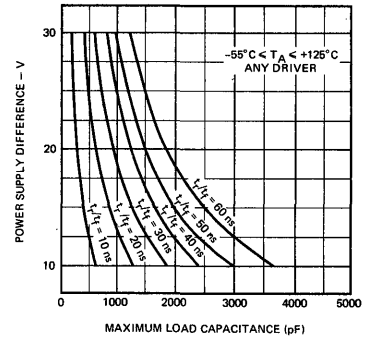


Fig. 7 RISE TIME AS A FUNCTION OF INPUT RESISTANCE

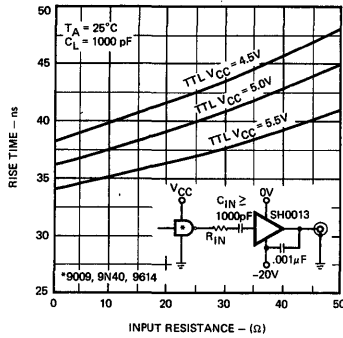


Fig. 8 FALL TIME AS A FUNCTION OF INPUT CAPACITANCE

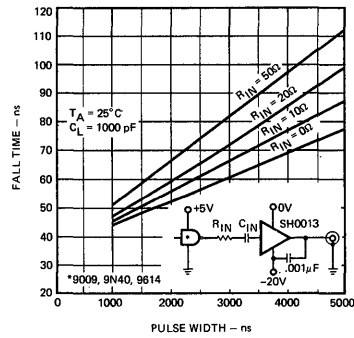


Fig. 9 TRANSITION TIMES AS A FUNCTION OF AMBIENT TEMPERATURE

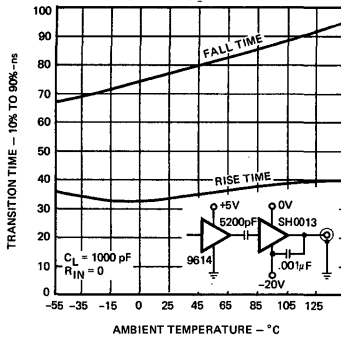


Fig. 10 MAXIMUM ALLOWABLE POWER DISSIPATION (12 LEAD TO-8 PACKAGE)

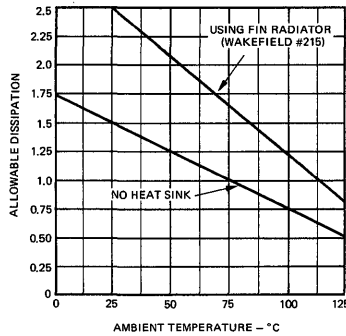


Fig. 11 AVERAGE INTERNAL POWER (PER DRIVER) AS A FUNCTION OF SUPPLY DIFFERENCE AND DUTY CYCLE

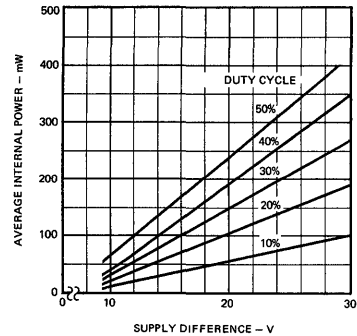


Fig. 12 TRANSIENT POWER AS A FUNCTION OF FREQUENCY FOR 16 V SUPPLY DIFFERENCE

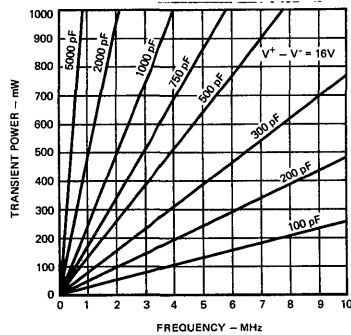
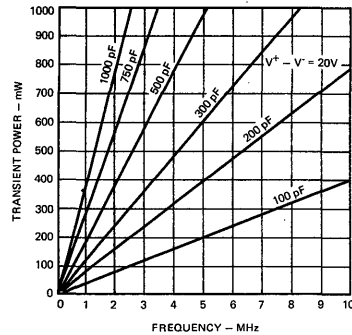
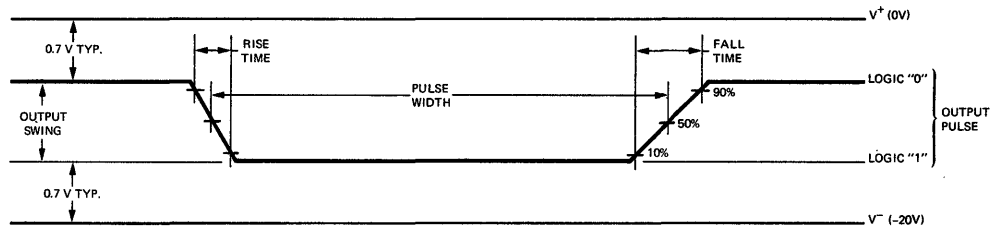


Fig. 13 TRANSIENT POWER AS A FUNCTION OF FREQUENCY FOR 20 V SUPPLY DIFFERENCE



WAVEFORM DEFINITIONS

APPLICATIONS



Logic "0" = Most positive output voltage
 Logic "1" = Most negative output voltage
 Output Swing = Clock pulse amplitude

V^+ = MOS V_{SS} Supply
 V^- = MOS V_{DD} Supply
 V^+ = V^- - Power Supply Difference
 $V^+ - V^-$ = Power Supply Difference

PULSE CHARACTERISTICS

All output pulse characteristics (rise time, fall time, pulse width) are determined by the input circuitry (R_{IN} , C_{IN}) and the driving element. In operation, the driving element, such as a 9614 line driver, delivers a positive voltage through the coupling elements to the SH0013 input transistor. As the input voltage reaches approximately 0.6 V, the input transistor (Q_1) begins to turn on and discharge the load capacitance in some rise time (t_r). If $R_{IN} = 0$ and $C_{IN} > 1000$ pF, the rise time is determined by the input current available from the driver. For the 9614, the available current is ~ 90 mA, causing the SH0013 to deliver a peak output current of ~ 550 mA. Adding input resistance lowers the available input current, increasing the rise time. When the output is fully ON (Logic "1"), the input capacitor will continue to discharge; the driver output impedance, coupling resistor (if any) and the SH0013 input impedance combine in series to determine the output pulse width. When the input current has decayed to a level which is insufficient to keep the input transistor saturated, it begins to turn off and the upper output transistor (Q_2) begins to charge the load capacitor in some fall time (t_f). Fall time is affected by the load capacitance and the input coupling components (R_{IN} , C_{IN}).

Typical pulse widths are shown in Figures 1–5 for various drivers versus coupling capacitance and resistance.

RISE TIME/FALL TIME LIMIT

The maximum transient output current that the SH0013 may conduct is ± 600 mA. More current than this might cause permanent damage or shorten the life of the device. The transient output current is given by

$$I_{\text{peak}} = \frac{\Delta V}{t} \times 0.8 \times C_L \tag{Eq. 1}$$

where ΔV = output swing, $t = t_r$ or t_f (10% to 90%), C_L = load capacitance, 0.8 = fraction of output swing from 10% to 90%.

Refer to Figure 6 for absolute minimum computed rise/fall times; see Figure 7 for typicals. Fall time is affected somewhat by the coupling elements as shown in Figure 8. See Figure 9 for rise/fall time variations with temperature.

MAXIMUM CAPACITIVE LOADING

The maximum capacitive load is determined by the maximum allowable dissipation of the TO-8 type Package, output swing, frequency and duty cycle. Duty cycle and supply difference determine the average internal power dissipated in the 1100 Ω resistors (P_{dc}).

$$P_{dc} = \frac{(V^+ - V^-)^2}{1100} \times (\text{Duty Cycle}) \tag{Eq. 2}$$

where duty cycle refers to the fraction of the cycle spent in the logical "1" state.

Figure 11 shows computed average internal power as a function of duty cycle and supply difference. Frequency, output swing and load capacitance determine the transient power dissipated in Q_1 , and Q_2 due to charging and discharging the load capacitance. Transient power (P_{ac}) may be computed as:

$$P_{ac} = C (\Delta V)^2 f \tag{Eq. 3}$$

where ΔV = output swing. For 16V or 20V supplies, see Figures 12 or 13.

For other supply voltages, use Eq. 3. The maximum allowable power dissipation versus ambient temperature for the TO-8 type Package is shown in Figure 10. The sum of the average internal power (P_{dc}) and the transient power (P_{ac}) is limited by the maximum allowable package dissipation.

$$P_{\text{TOTAL}} = P_{ac} + P_{dc} \leq P_{\text{max}} \tag{Eq. 4}$$

The maximum load capacitance may be easily determined using Eqs. 1, 2, 3, and 4.

APPLICATION CIRCUITS

Figures 17 and 18 show typical application circuits. Figure 17 shows a full two-phase system, where the coupling resistance and capacitance set the pulse width. Figure 18 shows a method of dc level shifting for +5V, -12V MOS systems. Note that in this circuit the SH0013 output waveform is identical to the waveform applied to the 9002.

STANDARD AC TEST CIRCUIT

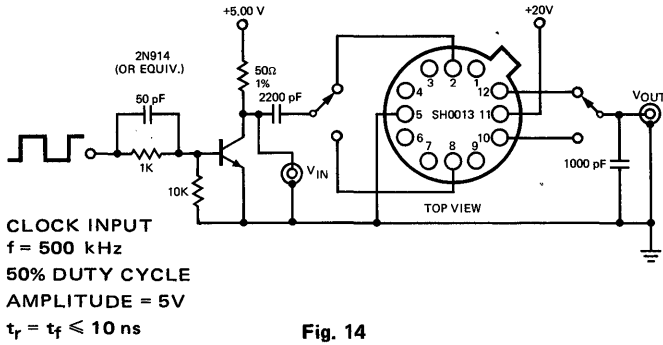


Fig. 14

TYPICAL APPLICATION AC TEST CIRCUIT

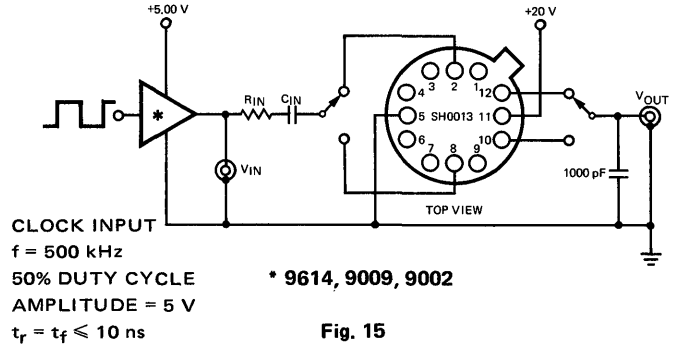
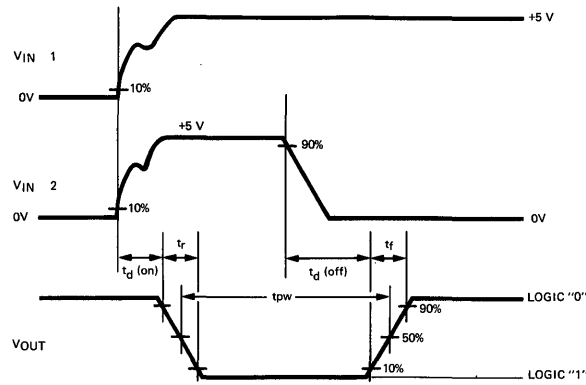


Fig. 15

TIMING DIAGRAM



VIN1: RC INPUT NETWORK DETERMINES t_{pw} . ALL PARAMETERS APPLICABLE EXCEPT $t_d \text{ off}$.
 VIN2: INPUT PULSE WIDTH DETERMINES t_{pw} .

Fig. 16

TWO-PHASE MOS CLOCK DRIVER

CIRCUIT

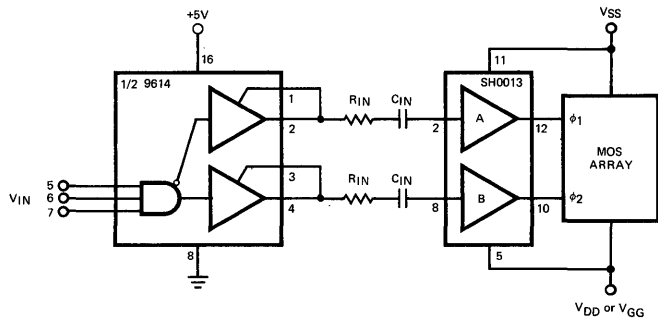
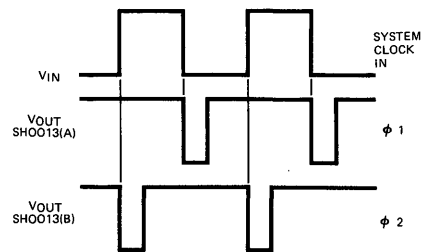


Fig. 17

WAVEFORMS



DC LEVEL SHIFTING

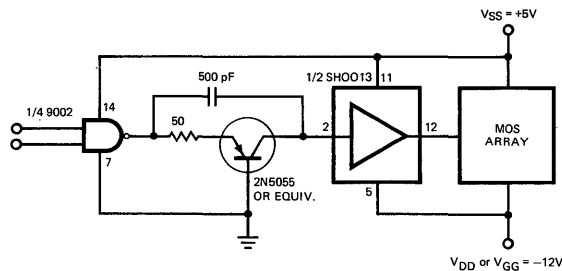


Fig. 18

SH2001

HIGH VOLTAGE, HIGH CURRENT DRIVER

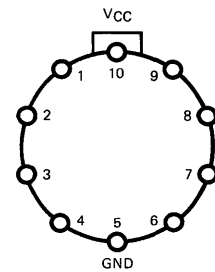
FAIRCHILD INTEGRATED MICROSYSTEMS

- INPUTS DTL/TTL COMPATIBLE
- USE FOR CORE, CABLE, AND LAMP DRIVER
- HIGH CURRENT CAPABILITY . . . 250 mA SINKING CURRENT AT 0.5 V
- HIGH VOLTAGE CAPABILITY . . . 50 V V_{CE0}
- LOGIC FLEXIBILITY . . . 4-INPUT NAND WITH INHIBIT (NOR) INPUT
- HIGH SPEED . . . $t_{on} = 70$ ns (TYP), $t_{off} = 110$ ns (TYP)

ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

Voltage Applied to Pin 8	+40 V
Voltage Applied to Pin 10	8 V
Internal Pointer Dissipation	
Metal Can	680 mW
Flatpak	570 mW
Storage Temperature	-65°C to +150°C
Input Reverse Current	1 mA
Current on Pin 8	1 A
Operating Temperature Range	
Military (SH2001)	-55°C to +125°C
Commercial (SH2001C)	0°C to 70°C

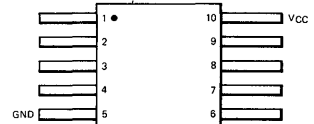
CONNECTION DIAGRAMS
(SEE BLOCK DIAGRAM)
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5E



ORDER INFORMATION

TYPE	PART NO.
SH2001	SH2001HM
SH2001C	SH2001HC

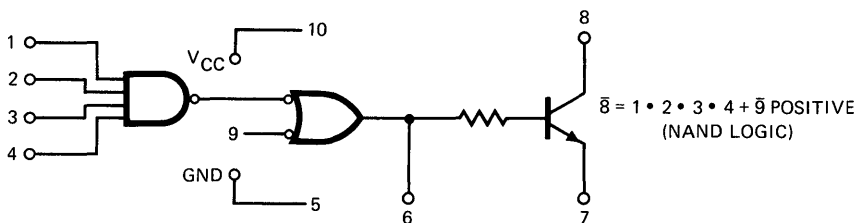
10-LEAD FLATPACK
(TOP VIEW)
PACKAGE OUTLINE 3F



ORDER INFORMATION

TYPE	PART NO.
SH2001	SH2001FM
SH2001C	SH2001FC

BLOCK DIAGRAM/CONNECTION DIAGRAM



Note: Above pin numbers apply to both flatpak and can, Top View.

FAIRCHILD INTEGRATED MICROSYSTEMS SH2001

SH2001 AND SH2001C

GUARANTEED TEST SEQUENCE

TEST NO.	LTPD GROUP	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMIT	
													MIN.	MAX.
1	A	V _{IH}	V _{IH}	V _{IH}	V _{IH}	GND		GND	I _{OL1}		V _{CCL}	V ₈		V _{OL}
2	A	V _{IL}				GND		GND	I _{OL1}	V _{IL}	V _{CCL}	V ₈		V _{OL}
3	A	V _{IL}				GND	I _{OL2}				V _{CCL}	V ₆		V _{OL2}
4	A		V _{IL}			GND	I _{OL2}				V _{CCL}	V ₆		V _{OL2}
5	A			V _{IL}		GND	I _{OL2}				V _{CCL}	V ₆		V _{OL2}
6	A				V _{IL}	GND	I _{OL2}				V _{CCL}	V ₆		V _{OL2}
7	A				GND	GND	I _{OL2}			V _{IH}	V _{CCL}	V ₆		V _{OL2}
8	B	V _R	GND	GND	GND	GND					V _{CCH}	I ₁		I _R
9	B	GND	V _R	GND	GND	GND					V _{CCH}	I ₂		I _R
10	B	GND	GND	V _R	GND	GND					V _{CCH}	I ₃		I _R
11	B	GND	GND	GND	V _R	GND					V _{CCH}	I ₄		I _R
12	B					GND				V _R	V _{CCH}	I ₉		I _R
13	C	V _F	V _R	V _R	V _R	GND					V _{CCH}	I ₁		-I _F
14	C	V _R	V _F	V _R	V _R	GND					V _{CCH}	I ₂		-I _F
15	C	V _R	V _R	V _F	V _R	GND					V _{CCH}	I ₃		-I _F
16	C	V _R	V _R	V _R	V _F	GND					V _{CCH}	I ₄		-I _F
17	C				GND	GND				V _F	V _{CCH}	I ₉		-I _F
18	D					GND		GND			V _{CCL}	V ₆	V _{OH}	
19	E	GND				GND	I _{OL3}	GND	V _{OX}		V _{CCL}	I ₈		I _{OX}
20	F					GND		GND			V _{PD}	I ₁₀		I _{PDH}
21	F	GND				GND					V _{MAX}	I ₁₀		I _{MAX}
22*	F					GND					V _{PD}			t _{on}
23*	F					GND					V _{PD}			t _{off}

*See Test Conditions on Page 3

FORCING FUNCTIONS (Temperature Range -55°C to +125°C) SH2001

SYMBOL	-55°C	+25°C	+125°C	UNITS
V _{CCL}	4.50	4.50	4.50	V
V _{CCH}	5.50	5.50	5.50	V
V _{PD}		5.00		V
V _{MAX}		8.00		V
V _{IL}	1.40	1.10	0.80	V
V _{IH}	2.10	1.90	1.70	V
V _R	4.00	4.00	4.00	V
V _F	0.40	0.40	0.40	V
I _{OL1}	250	250	250	mA
I _{OL2}	34.0	36.0	32.0	mA
I _{OL3}	8.0	8.0	8.0	mA
V _{OX}	40.0	40.0	40.0	V

FORCING FUNCTIONS (Temperature Range 0°C to +70°C) SH2001C

SYMBOL	0°C	+25°C	+70°C	UNITS
V _{CCL}	5.00	5.00	5.00	V
V _{CCH}	5.00	5.00	5.00	V
V _{PD}		5.00		V
V _{MAX}		8.00	.950	V
V _{IL}	1.20	1.10	1.80	V
V _{IH}	2.00	1.90	4.00	V
V _R	4.00	4.00	0.50	V
V _F	0.45	0.45	250	V
I _{OL1}	250	250	34.0	mA
I _{OL2}	36.0	36.0	8.0	mA
I _{OL3}	8.0	8.0	40.0	mA
V _{OX}	40.0	40.0		V

FAIRCHILD INTEGRATED MICROSYSTEMS SH2001

TEST LIMITS (Temperature Range -55°C to +125°C)

SH2001

SYMBOL	-55°C		+25°C		+125°C		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VOL1		0.45		0.45		0.45	V
VOL2		0.45		0.45		0.45	V
VOH	2.10		2.00		1.80		V
I _R				6.0		5.0	μA
-I _F		1.60		1.60		1.50	mA
I _{OX}				5.0		200	μA
I _{PDH}				30.6			mA
I _{MAX}				29.6			mA
t _{on}				160			ns
t _{off}				220			ns

TEST LIMITS (Temperature Range 0°C to +70°C)

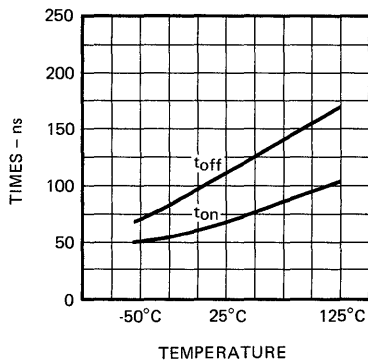
SH2001C

SYMBOL	0°C		+25°C		+70°C		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VOL1		0.45		0.45		0.5	V
VOL2		0.45		0.45		0.5	V
VOH	2.05		1.95		1.85		V
I _R				5.0		10.0	μA
-I _F		1.40		1.40		13.5	mA
I _{OX}				5.0		200	μA
I _{PDH}				30.6			mA
I _{MAX}				34.0			mA
t _{on}				200			ns
t _{off}				260			ns

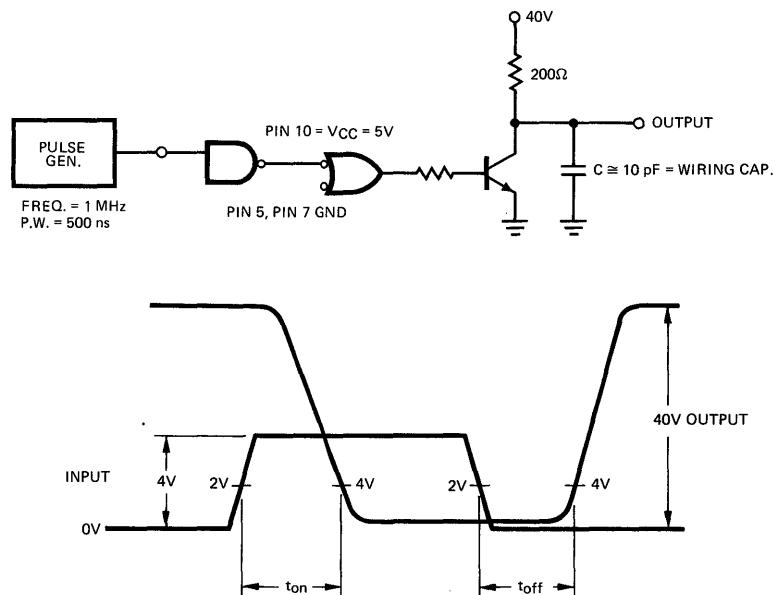
TABLE OF LTPD'S (These apply to test sequence page 2)

GROUP	COLD	+25°C	HOT
A	15%	10%	15%
B		10%	15%
C	15%	10%	15%
D	15%	10%	15%
E		10%	15%
F		10%	15%

TYPICAL SWITCHING TIMES

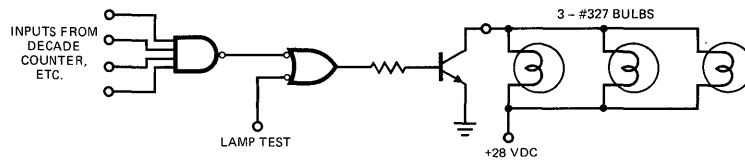


SWITCHING TIME TEST CONDITIONS

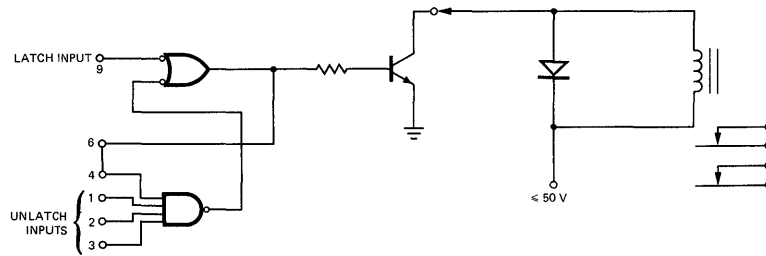


APPLICATIONS

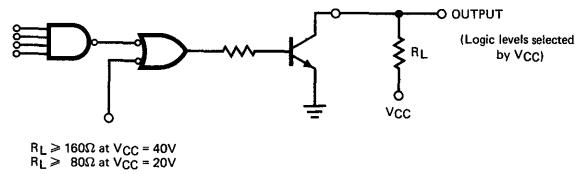
LAMP DRIVER



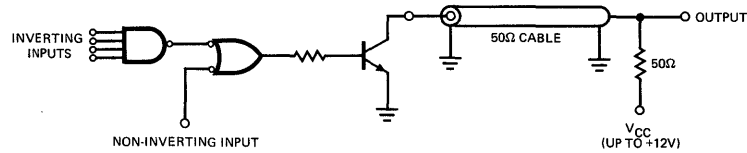
LATCHING RELAY



DTL INTERFACE DRIVER



HIGH CURRENT LINE TRANSMITTER



NOTE: If only non-inverting input is used, one of the inverting inputs must be grounded.

SH2002

DTL HIGH POWER DRIVER

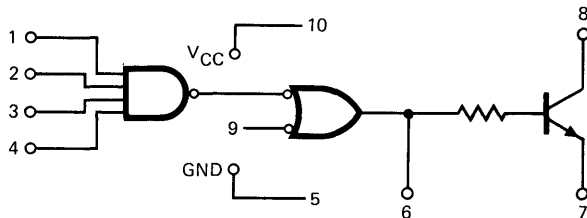
FAIRCHILD INTEGRATED MICROSYSTEMS

- LOGIC FLEXIBILITY . . . LATCHABLE 4-INPUT NAND WITH INHIBIT (NOR) INPUT
- HIGH CURRENT CAPABILITY . . . UP TO 150 mA
- HIGH VOLTAGE CAPABILITY . . . 50 V V_{CE0}
- INPUT COMPATIBLE WITH DTL/TTL PRODUCTS
- FULL -55°C to $+125^{\circ}\text{C}$ TEMPERATURE OPERATION
- APPLICATIONS INCLUDE CABLE AND LAMP DRIVER

ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature unless otherwise noted)

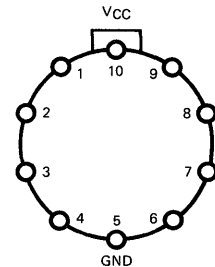
Voltage Applied to Pin 10 (continuous)	+8.0V
Input Reverse Current	1.0 mA
Voltage Applied to Pin 8 (continuous)	+40V
Voltage Applied to Pin 10 (pulsed ≤ 1 second)	+12V
Power Dissipation (Derate Linearity to $+175^{\circ}\text{C}$)	800mW
Storage Temperature Range	
Metal Can, Flatpak	-65°C to $+150^{\circ}\text{C}$
Molded Dip	-55°C to $+125^{\circ}\text{C}$
Operating Temperature Range	
Military (SH2002)	-55°C to $+125^{\circ}\text{C}$
Commercial (SH2002C)	0°C to 70°C

BLOCK DIAGRAM



Note: Above pin numbers refer to all packages, Top View

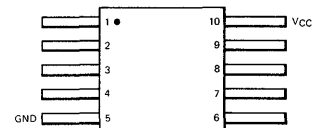
CONNECTION DIAGRAMS
(SEE BLOCK DIAGRAM)
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5E



ORDER INFORMATION

TYPE	PART NO.
SH2002	SH2002HM
SH2002C	SH2002HC

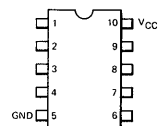
10-LEAD FLATPACK
(TOP VIEW)
PACKAGE OUTLINE 3F



ORDER INFORMATION

TYPE	PART NO.
SH2002	SH2002FM
SH2002C	SH2002FC

10-LEAD MOLDED DIP
(TOP VIEW)
PACKAGE OUTLINE 9F



ORDER INFORMATION

TYPE	PART NO.
SH2002C	SH2002PC

FAIRCHILD INTEGRATED MICROSYSTEMS SH2002

SH2002 AND SH2002C

GUARANTEED TEST SEQUENCE

TEST NO.	LTPD GROUP	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMIT	
													MIN.	MAX.
1	A	V _{IH}	V _{IH}	V _{IH}	V _{IH}	GND		GND	I _{OL1}		V _{CCCL}	V ₈		V _{OL}
2	A	V _{IL}				GND		GND	I _{OL1}	V _{IL}	V _{CCCL}	V ₈		V _{OL}
3	A	V _{IL}				GND	I _{OL2}				V _{CCCL}	V ₆		V _{OL2}
4	A		V _{IL}			GND	I _{OL2}				V _{CCCL}	V ₆		V _{OL2}
5	A			V _{IL}		GND	I _{OL2}				V _{CCCL}	V ₆		V _{OL2}
6	A				V _{IL}	GND	I _{OL2}				V _{CCCL}	V ₆		V _{OL2}
7	A				GND	GND	I _{OL2}			V _{IH}	V _{CCCL}	V ₆		V _{OL2}
8	B	V _R	GND	GND	GND	GND					V _{CCCH}	I ₁		I _R
9	B	GND	V _R	GND	GND	GND					V _{CCCH}	I ₂		I _R
10	B	GND	GND	V _R	GND	GND					V _{CCCH}	I ₃		I _R
11	B	GND	GND	GND	V _R	GND					V _{CCCH}	I ₄		I _R
12	B					GND				V _R	V _{CCCH}	I ₉		I _R
13	C	V _F	V _R	V _R	V _R	GND					V _{CCCH}	I ₁		-I _F
14	C	V _R	V _F	V _R	V _R	GND					V _{CCCH}	I ₂		-I _F
15	C	V _R	V _R	V _F	V _R	GND					V _{CCCH}	I ₃		-I _F
16	C	V _R	V _R	V _R	V _F	GND					V _{CCCH}	I ₄		-I _F
17	C				GND	GND				V _F	V _{CCCH}	I ₉		-I _F
18	D					GND		GND			V _{CCCL}	V ₆	V _{OH}	
19	E	GND				GND		GND	V _{OX}		V _{CCCL}	I ₈		I _{OX}
20	F					GND		GND			V _{PD}	I ₁₀		I _{PDH}
21	F	GND				GND					V _{MAX}	I ₁₀		I _{MAX}

FORCING FUNCTIONS (Temperature Range -55°C to +125°C) SH2002

SYMBOL	-55°C	+25°C	+125°C	UNITS
V _{CCCL}	4.50	4.50	4.50	V
V _{CCCH}	5.50	5.50	5.50	V
V _{PD}		5.00		V
V _{MAX}		8.00		V
V _{IL}	1.40	1.10	0.80	V
V _{IH}	2.10	1.90	1.70	V
V _R	4.00	4.00	4.00	V
V _F	0.40	0.40	0.40	V
I _{OL1}	150	150	150	mA
I _{OL2}	8.0	8.0	7.50	mA
V _{OX}	40.0	40.0	40.0	V

FORCING FUNCTIONS (Temperature Range 0°C to +70°C) SH2002C

SYMBOL	0°C	+25°C	+70°C	UNITS
V _{CCCL}	5.00	5.00	5.00	V
V _{CCCH}	5.00	5.00	5.00	V
V _{PD}		5.00		V
V _{MAX}		8.00		V
V _{IL}	1.20	1.10	.950	V
V _{IH}	2.00	1.90	1.80	V
V _R	4.00	4.00	4.00	V
V _F	0.45	0.45	0.50	V
I _{OL1}	250	250	250	mA
I _{OL2}	8.0	8.0	7.5	mA
V _{OX}	40.0	40.0	40.0	V

FAIRCHILD INTEGRATED MICROSYSTEMS SH2002

SH2002

TEST LIMITS (Temperature Range -55°C to +125°C)

SYMBOL	-55°C		+25°C		+125°C		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VOL1		0.45		0.40		0.45	V
VOL2		0.45		0.40		0.45	V
VOH	2.10		2.00		1.80		V
I _R				2.0		5.0	μA
-I _F		1.60		1.60		1.50	mA
I _{OX}				5.0		200	μA
I _{PDH}				30.6			mA
I _{MAX}				29.6			mA

SH2002C

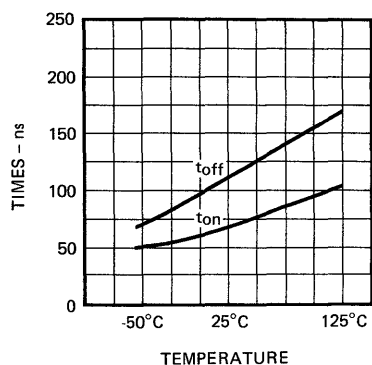
TEST LIMITS (Temperature Range 0°C to +70°C)

SYMBOL	0°C		+25°C		+70°C		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VOL1		0.45		0.45		0.5	V
VOL2		0.45		0.45		0.5	V
VOH	2.05		1.95		1.85		V
I _R				5.0		10.0	μA
-I _F		1.40		1.40		1.35	mA
I _{OX}				5.0		200	μA
I _{PDH}				30.6			mA
I _{MAX}				34.0			mA

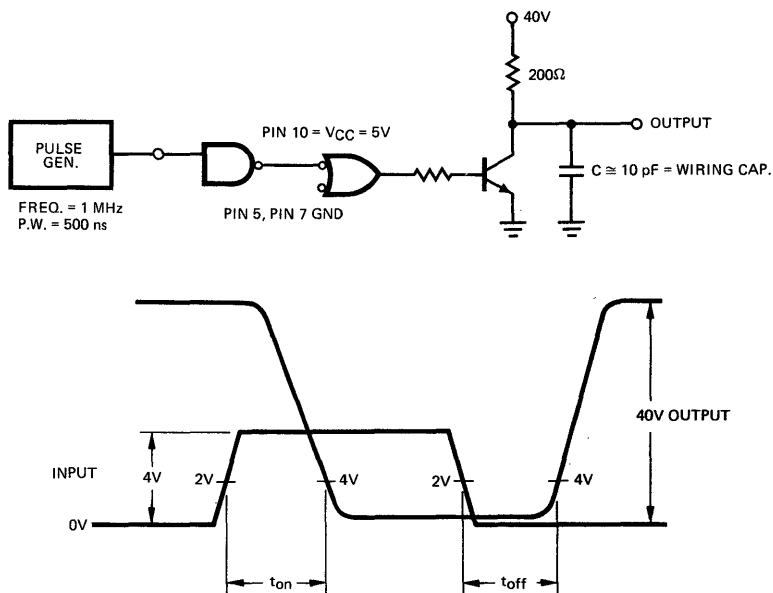
TABLE OF LTPD'S (These apply to test sequence page 2)

GROUP	COLD	+25°C	HOT
A	15%	10%	15%
B		10%	15%
C	15%	10%	15%
D	15%	10%	15%
E		10%	15%
F		10%	15%

TYPICAL SWITCHING TIMES

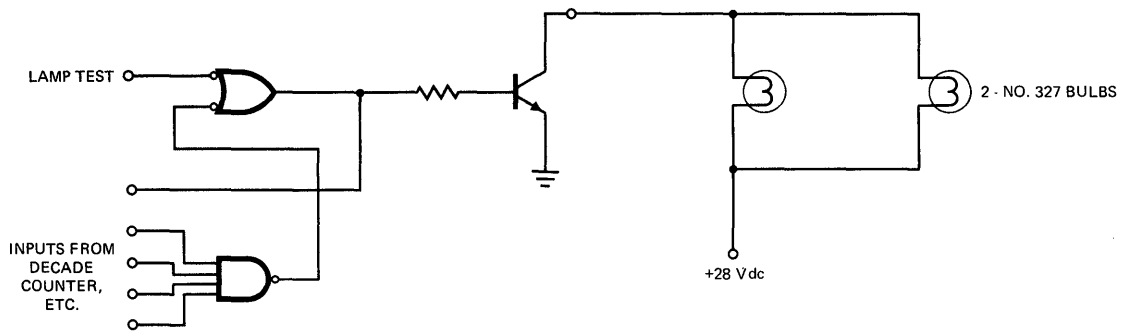


SWITCHING TIME TEST CONDITIONS

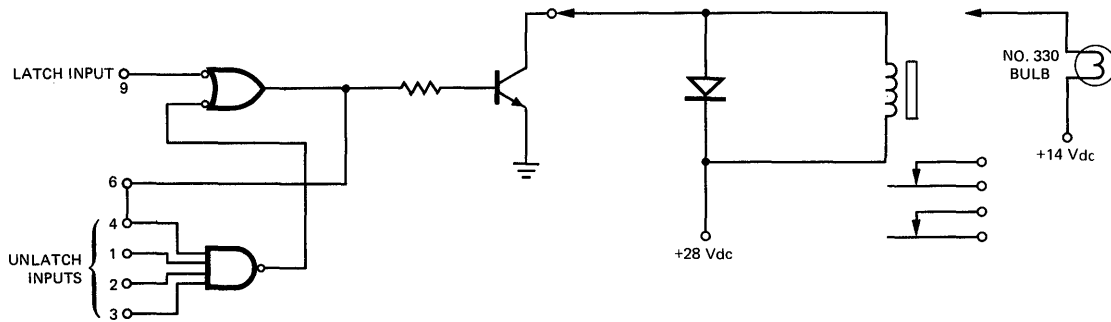


APPLICATIONS

LAMP DRIVER

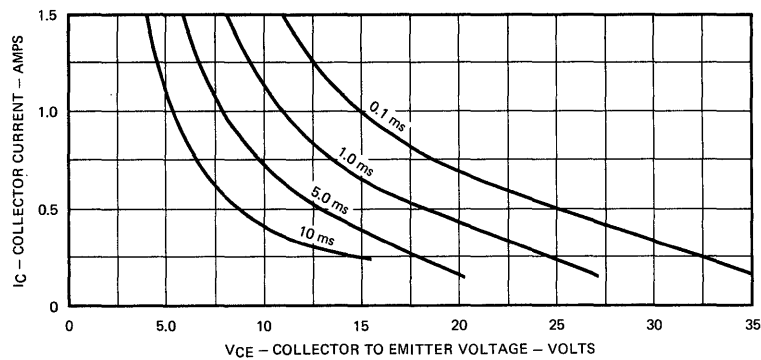


LATCHING RELAY OR FAULT LAMP DRIVER



Relay will unlatch if any input (1, 2, 3) goes LOW.

OUTPUT TRANSFER PULSE SAFE OPERATING AREA



SH2200

HIGH VOLTAGE, HIGH CURRENT DRIVER

FAIRCHILD INTEGRATED MICROSYSTEMS

FEATURES

- INPUT DTL/TTL COMPATIBLE
- HIGH SINKING CURRENT CAPABILITY . . . 500 mA AT 0.6 V
- HIGH VOLTAGE CAPABILITY . . . 50 V, V_{OX}
- LOGIC FLEXIBILITY . . . 4-INPUT NAND WITH INHIBIT (NOR) INPUT

APPLICATIONS

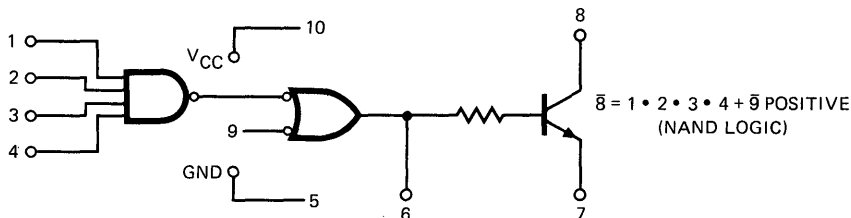
- RELAY AND LAMP DRIVER WITH LATCHING
- TAPE READOUT, TEST EQUIPMENT
- SOLENOID DRIVER

ABSOLUTE MAXIMUM RATINGS

Voltage Applied to Pin 8	+50V
Voltage Applied to Pin 10	+8.0V
Input Reverse Current	1.0 mA
Current on Pin 8	1.0A
Storage Temperature Range	
Metal Can and Flatpak	-65°C to +150°C
Molded DIP	-55°C to +125°C
Operating Temperature Range	
Metal Can and Flatpak	-55°C to +125°C
Molded DIP	0°C to +70°C
Maximum Power Dissipation	
At 25°C Ambient Temperature	
Metal Can (Note 1)	680 mW
Flatpak (Note 1)	575 mW
Molded DIP	455 mW

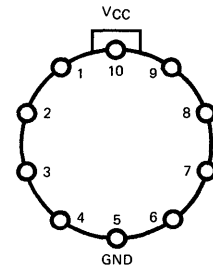
Note 1. Use proper heat sink at temperature above 100°C

BLOCK DIAGRAM



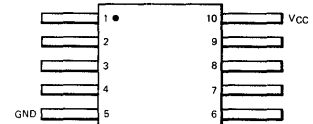
Note: Above pin numbers apply to all package types, Top View

CONNECTION DIAGRAMS (SEE BLOCK DIAGRAM) 10-LEAD METAL CAN (TOP VIEW) PACKAGE OUTLINE 5E



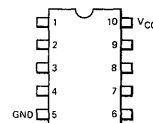
ORDER INFORMATION	
TYPE	PART NO.
SH2200	SH2200HM
SH2200C	SH2200HC

10-LEAD FLATPACK (TOP VIEW) PACKAGE OUTLINE 3F



ORDER INFORMATION	
TYPE	PART NO.
SH2200	SH2200FM
SH2200C	SH2200FC

10-LEAD MOLDED DIP (TOP VIEW) PACKAGE OUTLINE 9F



ORDER INFORMATION	
TYPE	PART NO.
SH2200C	SH2200PC

FAIRCHILD INTEGRATED MICROSYSTEMS SH2200

GUARANTEED TEST SEQUENCE

TEST NO.	LTPD GROUP AT															LIMITS	
	COLD	+25°C	HOT	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	MIN	MAX	
2	B	A	C	V _{IH}	V _{IH}	V _{IH}	V _{IH}	GND		GND	I _{OL1}		V _{CC}	V ₈		V _{OL1}	
3	B	A	C	V _{IL}				GND		GND	I _{OL1}	V _{IL}	V _{CC}	V ₈		V _{OL1}	
4	-	-	-		V _{IL}			GND		GND	I _{OL1}	V _{IL}	V _{CC}	V ₈		V _{OL1}	
5	-	-	-			V _{IL}		GND		GND	I _{OL1}	V _{IL}	V _{CC}	V ₈		V _{OL1}	
6	-	-	-				V _{IL}	GND		GND	I _{OL1}	V _{IL}	V _{CC}	V ₈		V _{OL1}	
7	B	A	C	V _{IL}				GND	I _{OL2}				V _{CC}	V ₆		V _{OL2}	
8	B	A	C		V _{IL}			GND	I _{OL2}				V _{CC}	V ₆		V _{OL2}	
9	B	A	C			V _{IL}		GND	I _{OL2}				V _{CC}	V ₆		V _{OL2}	
10	B	A	C				V _{IL}	GND	I _{OL2}				V _{CC}	V ₆		V _{OL2}	
11	B	A	C				GND	GND	I _{OL2}			V _{IH}	V _{CC}	V ₆		V _{OL2}	
12		A	C	V _R	GND	GND	GND	GND					V _{CC}	I ₁		I _R	
13		A	C	GND	V _R	GND	GND	GND					V _{CC}	I ₂		I _R	
14		A	C	GND	GND	V _R	GND	GND					V _{CC}	I ₃		I _R	
15		A	C	GND	GND	GND	V _R	GND					V _{CC}	I ₄		I _R	
16		A	C					GND				V _R	V _{CC}	I ₉		I _R	
17	B	A	C	V _F	V _R	V _R	V _R	GND					V _{CC}	I ₁		-I _F	
18	B	A	C	V _R	V _F	V _R	V _R	GND					V _{CC}	I ₂		-I _F	
19	B	A	C	V _R	V _R	V _F	V _R	GND					V _{CC}	I ₃		-I _F	
20	B	A	C	V _R	V _R	V _R	V _F	GND					V _{CC}	I ₄		-I _F	
21	B	A	C				GND	GND				V _F	V _{CC}	I ₉		-I _F	
22	B	A	C					GND		GND			V _{CC}	V ₆	V _{OH1}		
23	-	A	C	GND				GND	I _{OL3}	GND	V _{OX}		V _{CC}	I ₈		I _{OX}	
24	-	A	-					GND					V _{PD}	I ₁₀		I _{PD}	
25	-	A	-	GND				GND				GND	V _{MAX}	I ₁₀		I _{MAX}	

FORCING FUNCTIONS (Temperature Range 0°C to 70°C) SH2200C

SYMBOL	0°C	+25°C	+70°C	UNITS
V _{CC}	5.0	5.0	5.0	V
V _{PD}		5.0		V
V _{MAX}		8.0		V
V _{IL}	0.85	0.85	0.85	V
V _{IH}	1.9	1.8	1.6	V
V _R	4.5	4.5	4.5	V
V _F	0.45	0.45	0.45	V
V _{OX}		50	50	V
I _{OL1}	500	500	500	mA
I _{OL2}	16	16	16	mA
I _{OL3}		8.0		mA

TEST LIMITS (Temperature Range 0°C to 70°C) SH2200C

SYMBOL	0°C	+25°C	+70°C	UNITS
V _{OL1}	0.6	0.6	0.6	V
V _{OL2}	0.45	0.45	0.45	V
V _{OH1}	1.95	1.85	1.65	V
I _R		60	60	μA
-I _F	1.6	1.6	1.6	mA
I _{OX}		5.0	200	μA
I _{PD}		12.2		mA
I _{MAX}		30		mA

FAIRCHILD INTEGRATED MICROSYSTEMS SH2200

FORCING FUNCTIONS (Temperature Range -55°C to +125°C) SH2200

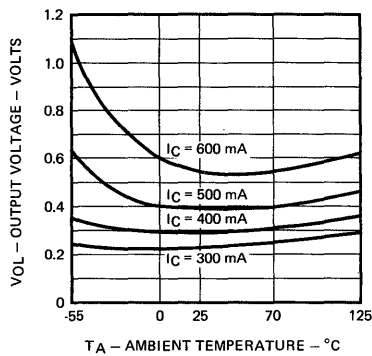
SYMBOL	-55°C	+25°C	+125°C	UNITS
V _{CC}	5.0	5.0	5.0	V
V _{PD}		5.0		V
V _{MAX}		8.0		V
V _{IL}	0.8	0.9	0.8	V
V _{IH}	2.0	1.7	1.4	V
V _R	4.5	4.5	4.5	V
V _F	0.4	0.4	0.4	V
V _{OX}		50	50	V
I _{OL1}	500	500	500	mA
I _{OL2}	16	16	16	mA
I _{OL3}		8.0		mA

TEST LIMITS (Temperature Range -55°C to +125°C) SH2200

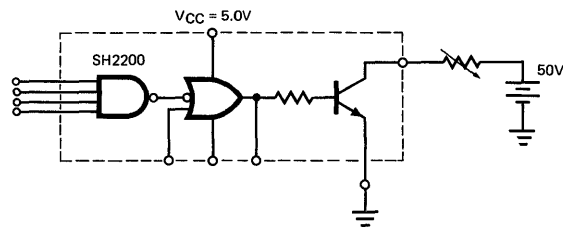
SYMBOL	-55°C	+25°C	+125°C	UNITS
V _{OL1}	0.8	0.6	0.7	V
V _{OL2}	0.4	0.4	0.4	V
V _{OH1}	2.05	1.75	1.45	V
I _R		60	60	μA
-I _F	1.6	1.6	1.6	mA
I _{OX}		5.0	200	μA
I _{PD}		11		mA
I _{MAX}		25		mA

PERFORMANCE CURVES

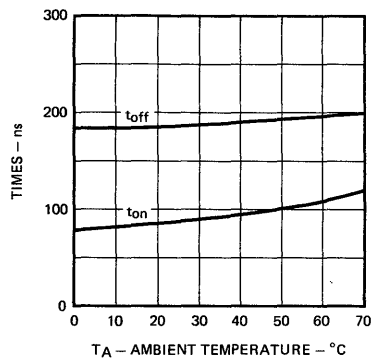
TYPICAL SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE



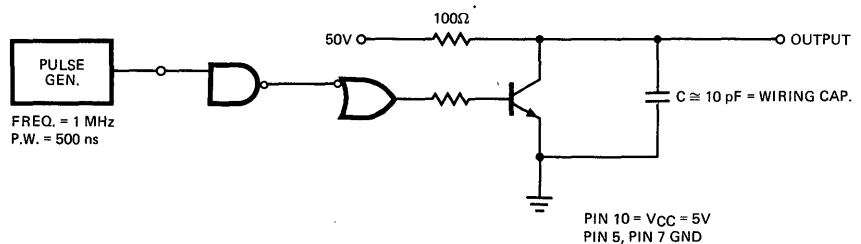
OUTPUT VOLTAGE TEST CIRCUIT



TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

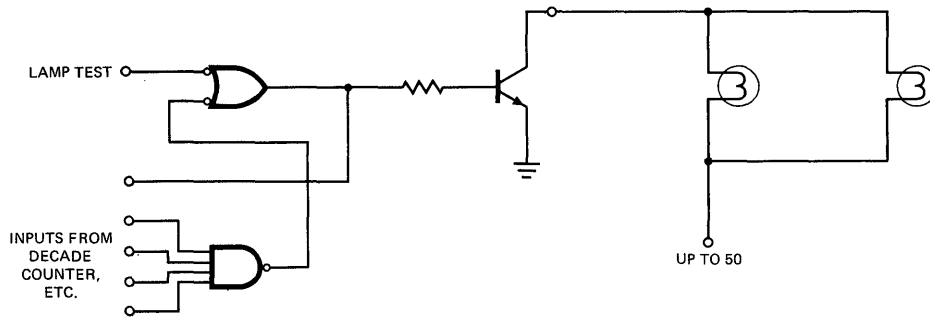


SWITCHING TIME TEST CIRCUIT

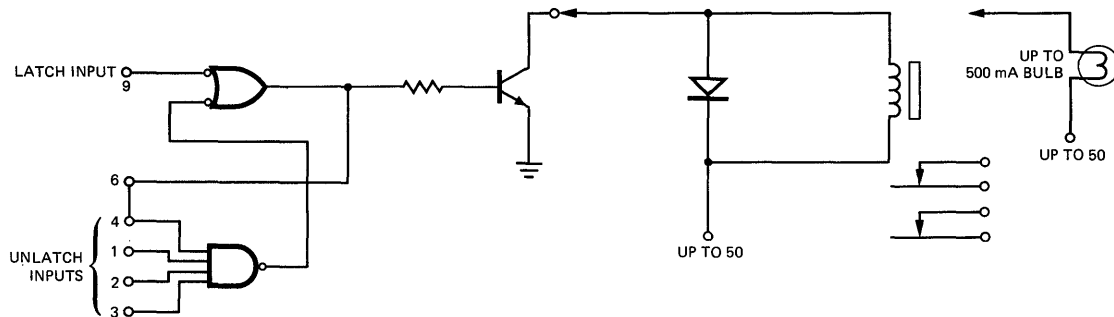


APPLICATIONS

LAMP DRIVER



LATCHING RELAY OR FAULT LAMP DRIVER



Relay will unlatch if any input (1, 2, 3) goes LOW.

SH8090

10-BIT D/A CONVERTER

FAIRCHILD INTEGRATED MICROSYSTEMS

GENERAL DESCRIPTION — The SH8090 is a complete Digital to Analog Converter using hybrid, MOS/LSI, Linear IC, and thick film technology. The digital word can be entered serially or in parallel. Transfer gates provide isolation between data input registers and the holding register. The analog output is provided with short circuit protection and offset voltage null capability.

- SERIAL or PARALLEL OPERATION
- 8 and 10-BIT DATA LENGTHS
- 300 mW POWER DISSIPATION
- MOS LOGIC LEVELS
- ANALOG OUTPUT LEVEL 0 TO -5 V

ABSOLUTE MAXIMUM RATINGS

Logic Input Levels	-30 to $+0.3\text{ V}$
Power Supplies	
Logic V_{GG}	-29 V
Analog V_{CC} & V_{DD}	$\pm 15\text{ V}$
Reference V_f	-6.0 to $+0.3\text{ V}$
Operation Temperature	-20°C to $+85^\circ\text{C}$
Storage Temperature	-55°C to $+125^\circ\text{C}$

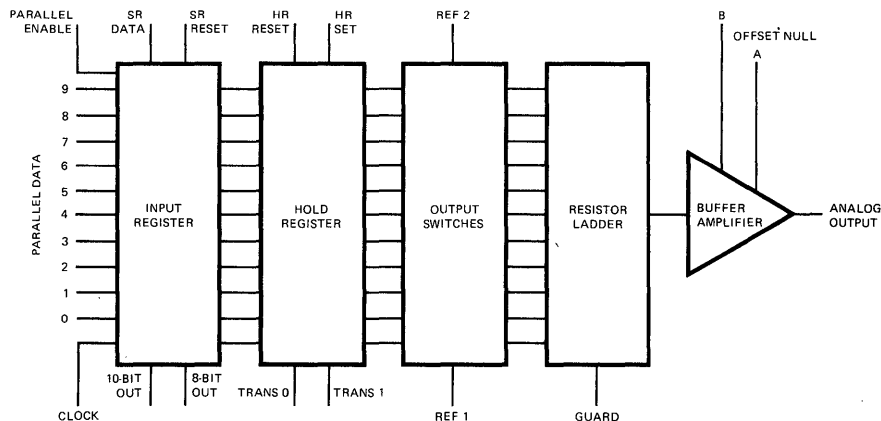
CONNECTION DIAGRAM
30-LEAD FLATPAK
PACKAGE OUTLINE 2B

ORDER INFORMATION

TYPE	PART NO.
8090	SH8090FM

6

BLOCK DIAGRAM



FAIRCHILD INTEGRATED MICROSYSTEMS • SH8090

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input HIGH Voltage			0		-2.0	V
Input LOW Voltage			-9.0		-30	V
Output HIGH Voltage			0		-1.0	V
Output LOW Voltage			-10		-30	V
Clock Input	Amplitude		-9.0		-30	V
	Width		1.0		10	μs
Clock Frequency	f _{MAX}		DC		100	kHz
Logic Input Capacitance	C _{IN}			10		pF
Logic Input Leakage	I _{LX}	V _{IN} = -20 V			5.0	μA
Power Supply Current Drain	I _{MAX}					
Logic V _{GG}		V _{GG} = -27 V		4.5		mA
Analog V _{CC} & V _{DD}		V _{CC} & V _{DD}		3.5		mA
Voltage Reference		V _f = -5.0 V		100		μA
Total Power Dissipation	P _{MAX}			180		mW
Analog Output Voltage Offset	V _{OFF}	Logic all "0" R _L ≥ 2.0 kΩ		1.0		mV
Analog Output Load	R _L		2.0	10		kΩ

SPECIFICATIONS (T_A = 25°C, Ref Voltage = -5.0 V)

Accuracy	±0.1% of Full Range, Typ.
Settling Time	
Serial Operation	20 μs max.
Parallel Operation	20 μs max.
Word Rate (Continuous 10 BIT NRZ)	
Serial Operation	10,000 word/s
Parallel Operation	50,000 word/s
Output Range	0.0 V to -5.0 V ±5 mV
Temperature Coefficient	±0.002%/°C of full scale
Supply Voltage Rejection Ratio	≤180 μV/V
Offset Drift (Long term)	≤0.15 μV/Day

FUNCTIONS

PIN NO.	DESCRIPTION
1	RESET SR: A "1" voltage level applied to this input will reset the input register but will not affect data in the hold register.
28	RESET HR: A "1" voltage level at this pin will reset the hold register to all "0"s address. The analog voltage will be 0 volts.
27	SET HR: A "1" voltage level at this pin will set the hold register to all "1"s address. The analog voltage will be at full scale.
29, 30	TRANSFER "1" & "0": When both transfer "1" and transfer "0" are at A "1" level, data is transferred from the input register to the hold register.
14	PARALLEL ENABLE: A "1" voltage level applied to this pin will enable the parallel data inputs and inhibit the serial data input.
21	GUARD: This pin provides extra shielding from logic noise and external interference when connected to the analog output.
22, 26	OFFSET NULL: Although the SH8090 has very low offset, it may be desirable to adjust the offset to zero.

NEW
PRODUCTS
TO BE
ANNOUNCED

COMPUTER/
INTERFACE

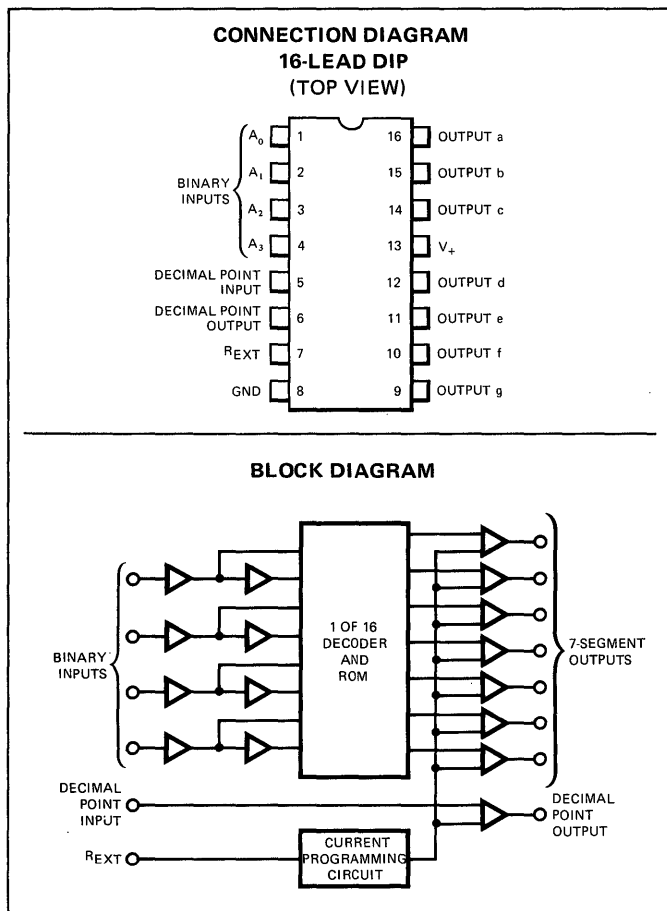


9660

SEVEN SEGMENT DECODER/ PROGRAMMABLE CURRENT DRIVER

GENERAL DESCRIPTION — The 9660 7-Segment Decoder/Programmable Current Driver is designed to accept four binary inputs (BCD) and a decimal point input. It converts these signals to active HIGH 7-segment and decimal point constant current outputs for driving common cathode LED displays. One external resistor sets the driver output currents for driving each segment and can be used either as an LED brightness control or for increasing the drive capability for multiplexing systems. The on-chip decoder and ROM are normally programmed hexadecimal although other 4-bit binary codes can be programmed.

- 7-SEGMENT AND DECIMAL POINT OUTPUT
- SINGLE RESISTOR PROGRAMS OUTPUT CURRENTS
- OUTPUT CURRENT RANGE PROGRAMMABLE FROM 5 mA TO 50 mA
- ON-CHIP DECODING AND PROGRAMMABLE ROM
- TTL/MOS INPUT COMPATIBLE INPUTS
- OPERATES FROM +5V

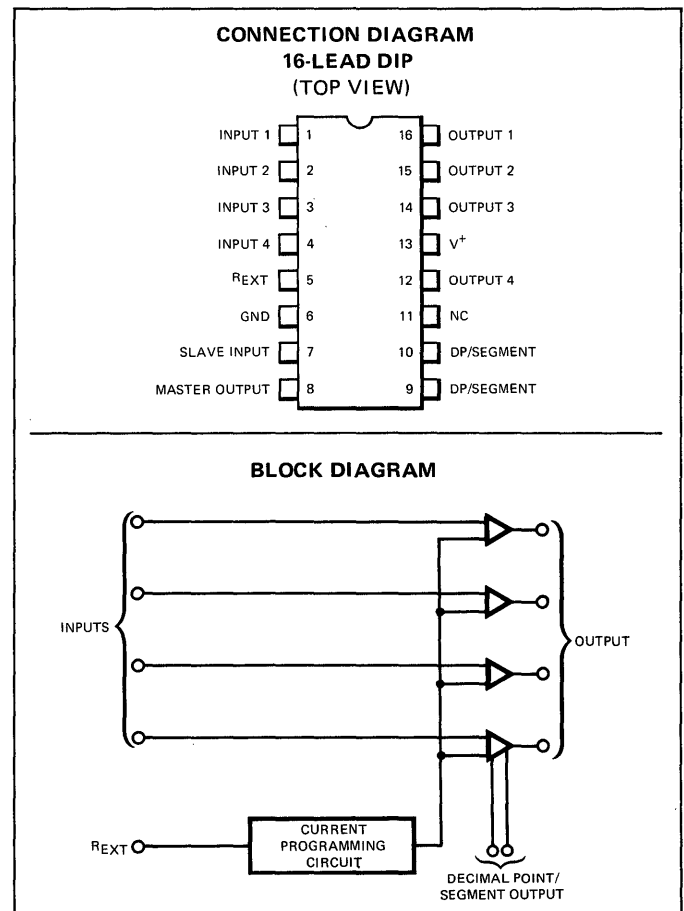


9661

QUAD PROGRAMMABLE CURRENT SEGMENT DRIVER

GENERAL DESCRIPTION — The 9661 Quad Programmable, Current Segment Driver is designed to drive common cathode LED displays. One resistor sets the output currents from 5 mA to 75 mA which enables its use in driver-per-digit or multiplex LED display applications. Two devices can be connected to give a total of 7-segment drivers and a decimal point driver with the output currents all determined by one external resistor.

- OUTPUT CURRENTS FROM 5 mA TO 75 mA
- TTL/MOS INPUT COMPATIBLE INPUTS
- SINGLE RESISTOR PROGRAMMED FOR OUTPUT CURRENT FOR ONE OR MORE DEVICES
- OPERATES FROM +5V



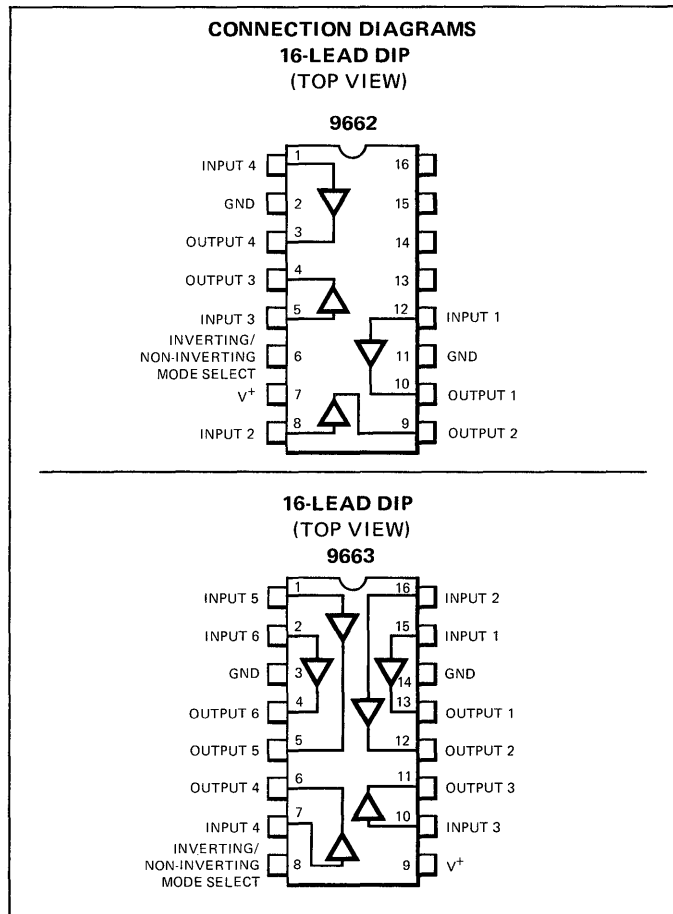
9662/9663

LED/LAMP DIGIT DRIVER

GENERAL DESCRIPTION — The 9662 is a Quad LED/Lamp Digit Driver and the 9663 is a Hex LED/Lamp Digit Driver with active LOW outputs designed to sink the common cathode current of 7-segment LED displays. The driver's inputs are TTL/MOS compatible with inverting or non-inverting operation selected by one external pin connection.

These devices are also ideal for driving lamps, relays, or other circuits requiring high drive currents.

- MOS/TTL COMPATIBLE INPUTS
- 600 mA OUTPUT SINK CAPABILITIES
- INVERTING OR NON-INVERTING MODE SELECTION
- OPERATES FROM +5 V



GLOSSARY

COMPUTER/INTERFACE

Bandwidth — The frequency at which the device gain is 0.707 of its low frequency value.

Clamped Output HIGH Voltage — The voltage potential necessary to turn on (forward bias) the clamping diode on the output pin.

Clamped Output LOW Voltage — See Clamped Output HIGH Voltage.

Clock Frequency — The reciprocal of the clock period; the clock repetition rate.

Clock Input, Amplitude — The peak amplitude of the clock signal.

Clock Input, Width — The time duration of the clock pulse.

Common Mode Input Firing Voltage — The common mode input voltage that exceeds the dynamic range of the input stage resulting in the output switching states.

Common Mode Input Overload Recovery Time — The time delay between removal of an input common mode voltage outside the input common mode range, and resumption of normal device operation.

Common Mode Rejection Ratio — The ratio of the change in output voltage to the change in input common mode voltage.

Common Mode Voltage — The arithmetic mean of the voltage present at the differential inputs with respect to the device ground reference.

Delay Time — See Propagation Delay.

Differential Input Bias Current — The current required in the differential input stage in order to bias the stage into operation.

Differential Input Impedance — The impedance seen looking between the input terminals.

Differential Input Offset Current — The difference in currents required by the transistors in the input stage to bias the input stage to its quiescent operation point.

Differential Input Overload Recovery Time — The time delay between removal of a differential input voltage that exceeds the differential input voltage operating range, and resumption of normal device operation.

Differential Input Threshold Voltage — The voltage difference between the + and - inputs required to guarantee the output logic state.

Differential Voltage Gain — The ratio of the output voltage to the differential input voltage.

Enable Input Forward Current — The current drawn out of the input necessary to force the input into a logic LOW state.

Enable Input Leakage Current — The current flowing into the enable input necessary to insure a logic HIGH state.

Fall Time — The time required for the signal to fall from 90% to 10% of its output value into a specified load network.

Gate Input HIGH Current — See Enable Input Leakage Current.

Gate Input LOW Current — See Enable Input Forward Current.

Hysteresis — The voltage difference between the switching points of the device. See Lower Input Threshold Voltage and Upper Input Threshold Voltage.

Input Bias Current — The current required to place the input stage into its quiescent operation region.

Input Capacitance — The equivalent capacitance seen looking into either input with the other input grounded.

Input Clamp Diode Voltage — The input voltage at which the clamp diode associated with the input becomes forward biased.

Input Current — The current flowing into the input with a specified voltage applied to the input.

Input Current at Maximum Input Voltage — The leakage current into a TTL or DTL input with the absolute maximum allowed input voltage applied to the input.

Input Forward Current — See Input LOW Current.

Input HIGH Current — The leakage current into an input when that input is in a HIGH or logic "1" state.

Input HIGH Voltage — The voltage required at the input to define the input as being in a HIGH or logic "1" state.

Input Latch Voltage — See Input Clamp Diode Voltage.

Input LOW Current — The current drawn out of the input when the input is in a LOW or logic "0" state.

Input LOW Voltage — The voltage required at the input to define the input as being in a LOW or logic "0" state.

Input Noise Voltage — The rms noise voltage present at the amplifier output divided by the gain of the amplifier — measured with the inputs connected to ground through a low resistance.

Input Offset Current — The difference between the currents into the input terminals required to set the output voltage to zero volts.

Input Resistance — The equivalent resistance seen looking into either input terminal with the other terminal grounded.

Input Reverse Current — See Input HIGH Current.

Input to Output Delay — See Propagation Delay.

Input Voltage — The voltage potential between the input terminal and the device ground reference.

Input Voltage Range — The range of input voltages which, if exceeded on either input terminal, could cause the device to cease functioning properly.

Input Voltage Rating — See Input Voltage Range.

Linearity — The deviation of the characteristic from a straight line.

Logic Input Capacitance — The equivalent capacitance seen looking into the logic input terminal.

Logic Input Leakage – See Input HIGH Current.

Logic Inputs, HIGH – An input voltage potential between 2.0 and 5.5 V – defines the HIGH or logic “1” input state.

Logic Inputs, LOW – An input voltage potential between 0 and 0.8 V – defines the LOW or Logic “0” input state.

Logic Outputs, HIGH – An output voltage potential between 2.4 and 5.5 V – defines the HIGH or logic “1” output state.

Logic Outputs, LOW – An output voltage potential between 0 and 0.4 V – defines the LOW or logic “0” output state.

Lower Input Threshold Voltage – In conjunction with hysteresis, the voltage potential at which the device will change to the opposite output logic state in response to an algebraically decreasing input voltage.

Negative Supply Current – The current drain on the negative power supply out of the device negative power supply pin.

Open Loop Threshold Voltage – The switching point of the device with the hysteresis disabled, in an amplifier with selectable hysteresis.

Output Common Mode Voltage - The arithmetic mean of the two output voltages, for devices with differential outputs.

Output HIGH Current – The current sourced by the output while maintaining a HIGH output logic level.

Output HIGH Leakage Current – The leakage current into the output transistor at the specified output voltage potential, for uncommitted or open collector NPN outputs.

Output HIGH Voltage – See Logic Outputs, HIGH.

Output Impedance – The equivalent impedance seen looking into the output terminal.

Output Leakage Current – See Output HIGH Leakage Current.

Output LOW Leakage Current – The current out of the output in the output LOW state, for uncommitted or open emitter NPN outputs.

Output LOW Voltage – See Logic Output, LOW.

Output Offset Voltage – The voltage difference between the two outputs with both inputs grounded.

Output Resistance – The equivalent resistance seen looking into the output terminal.

Output Short-Circuit Current – The current flowing out of the output when the output is shorted to ground.

Output Sink Current – The maximum current into the collector of the output transistor, for open collector devices.

Output Voltage – The voltage present at the output terminal, referred to ground.

Output Voltage Swing – The peak output amplitude, referred to ground, that can be delivered without signal clipping.

Positive Supply Current – The device current drain via the positive power supply pin.

Power Consumption – The dc power required to operate the device under no load conditions.

Power Supply Rejection – The ratio of the change in input offset voltage to the change in power supply voltage causing it.

Propagation Delay – The time interval between application of an input voltage step and its arrival at the output, measured at the 50% of final value points.

Propagation Delay Time, HIGH to LOW Output – The propagation delay of a signal causing the output to change from a HIGH to a LOW logic state.

Propagation Delay Time, LOW to HIGH Output – The propagation delay of a signal causing the output to change from a LOW to a HIGH logic state.

Resistive Output HIGH Voltage – See Logic Outputs, HIGH.

Resistive Output LOW Voltage – See Logic Outputs, LOW.

Response Control Input Current – The current flowing into the response control pin with a specified voltage applied to the response control pin.

Rise Time – The time interval required for a signal to rise from 10% to 90% of its final amplitude.

Static Forward Current Transfer Ratio – The ratio of dc collector current to base current in a transistor.

Storage Time – The propagation delay due to stored charge in the transistor.

Strobe Input Current – See Input HIGH Current.

Strobe Input HIGH Current – See Input HIGH Current.

Strobe Input Leakage Current – See Input HIGH Current.

Strobe Input LOW Current – See Input LOW Current.

Strobe to Output Delay – The propagation delay of a signal applied to the strobe input and the response of the output, measured at the 50% of final amplitude points.

Supply Voltage Rejection Ratio – The ratio of the change in input offset voltage to the change in power supply voltage that produces it.

Switching Speed – See Propagation Delay.

Terminating Resistance – The resistance of a resistor normally used to provide a termination to a transmission line.

Threshold Uncertainty – The device to device variation in input threshold voltage including effects of differing temperatures.

Transition Time, HIGH to LOW Output – See Fall Time.

Transition Time, LOW to HIGH Output – See Rise Time.

Turn-Off Delay – See Propagation Delay Time, LOW to HIGH Output.

Turn-Off Propagation Delay – See Propagation Delay Time, LOW to HIGH Output.

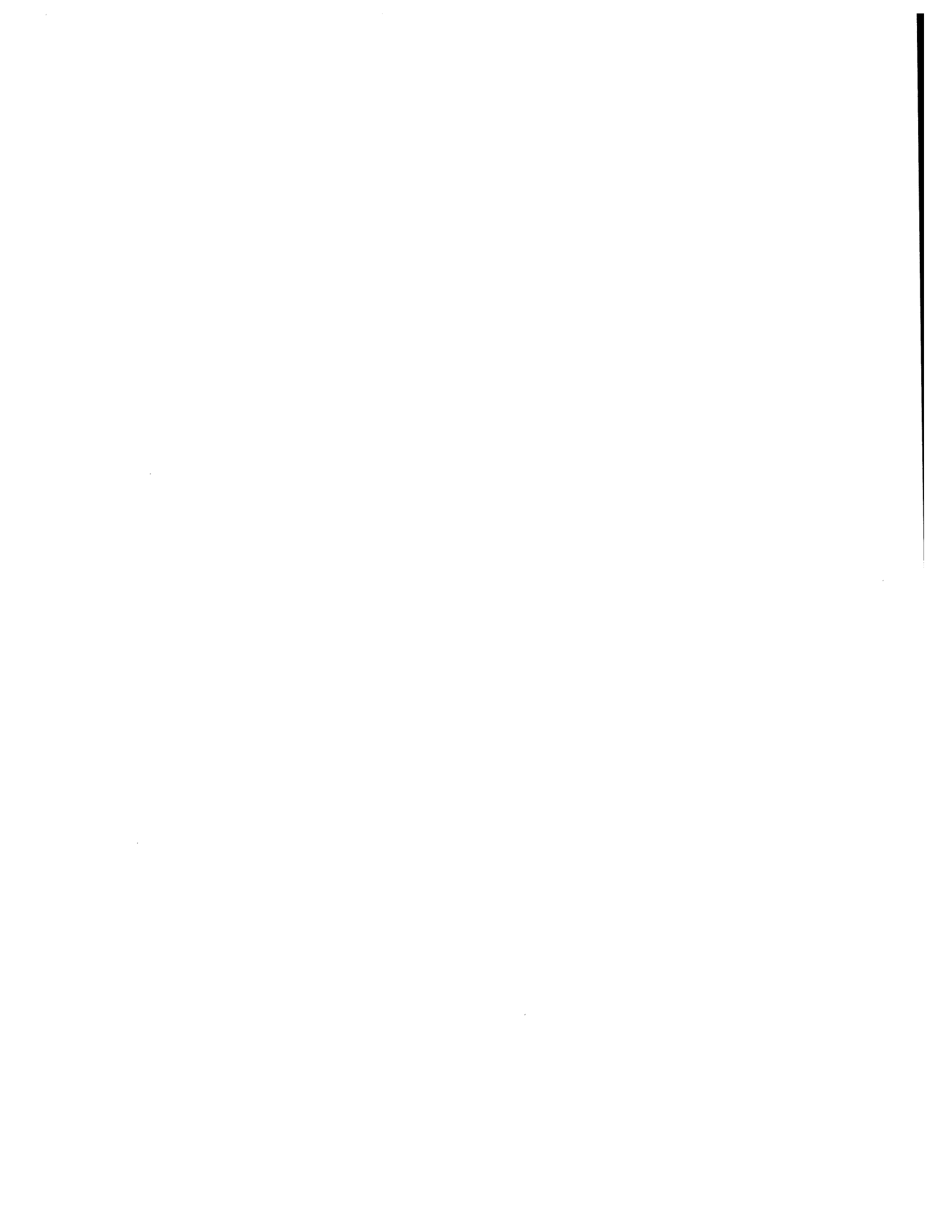
Turn-Off Time – See Propagation Delay Time, LOW to HIGH Output.

Turn-On Delay – See Propagation Delay Time, HIGH to LOW Output.

Turn-On Propagation Delay – See Propagation Delay Time, HIGH to LOW Output.

Turn-On Time – See Propagation Delay Time, HIGH to LOW Output.

Upper Input Threshold Voltage – The input voltage that causes the output to change logic state, when the input voltage is increasing in a device with hysteresis.



LINEAR LINEAR LINEAR LINEAR LINEAR LINEAR LINEAR

CONTENTS AND SECTION SELECTOR

CONSUMER	7
TRANSISTOR/DIODE ARRAYS/ANALOG SWITCHES	8
PACKAGE OUTLINES	9
ORDER INFORMATION	10
MIL-M-38510/MIL-STD-883	11
DICE	12
INDUSTRY CROSS REFERENCE GUIDE	13
APPLICATION INFORMATION	14

INDEX

Selection Guide 7-4

DATA SHEETS

Television Receiver and Video Tape Recorder

μ A703	RF-IF Amplifier	7-9
μ A704	Television Sound System	7-96
μ A723	Voltage Regulator	5-7
μ A733	Differential Video Amplifier	6-12
μ A746	Chroma Demodulator	7-32
μ A780	Chroma Subcarrier Regenerator	7-60
μ A781	Gain Controlled IF Amplifier	7-66
μ A786	PAL Chroma Demodulator	7-71
μ A796	Modulator/Demodulator	7-74
μ A7800	Three-Terminal Voltage Regulators	5-14
μ A78M00	Three-Terminal Voltage Regulators	5-45
TBA510	Chroma Processing Circuit	7-98
TBA920	Horizontal Oscillator, Phase Comparator and Sync Separator	7-99
TBA970	Television Video Amplifier	7-99
1326	Chroma Demodulator	7-100
3064	TV Automatic Fine Tuning Circuit	7-78
3065	TV Sound System	7-82
3066	TV Chroma Processor	7-85
3067	TV Chroma Demodulator	7-89

AM/FM Receiver — Audio

μ A703	RF-IF Amplifier	7-9
μ A705	Dual Channel Power Amplifier	7-96
μ A706	5 Watt Audio Amplifier	7-11
μ A720	AM Radio System	7-16
μ A732	FM Stereo Multiplex Decoder	7-21
μ A739	Dual Low Noise Operational Amplifier	7-24
μ A749	Dual Audio Preamplifier	7-36
μ A753	FM Gain Block	7-44
μ A757	Gain Controlled IF Amplifier	7-47
μ A758	Phase Locked Loop Stereo Multiplex Decoder	7-53
μ A767	FM Stereo Multiplex Decoder	7-57
μ A768	FM Stereo Multiplex Decoder	7-21
μ A769	FM Stereo Multiplex Decoder	7-57
μ A7800	Three-Terminal Voltage Regulators	5-14
μ A78M00	Three-Terminal Voltage Regulators	5-45
2136	FM IF Amplifier and Detector	7-101
3075	FM IF Amplifier-Limiter, Detector, Audio Preamplifier	7-92
3076	FM Gain Block	7-101

Automotive and Appliance

μ A741	Frequency Compensated Operational Amplifier	3-53
μ A742	Zero Crossing AC Trigger - TRIGAC	7-28
μ A7350	Tachometer Subsystem	7-97

μ A7351	Triple Operational Amplifier	7-97
μ A7800	Three-Terminal Voltage Regulators	5-14
μ A78M00	Three-Terminal Voltage Regulators	5-45
Calculator (See Computer/Interface Selection Guide)		
μ A7800	Three-Terminal Voltage Regulators	5-14
μ A78M00	Three-Terminal Voltage Regulators	5-45
9660	Seven Segment Decoder/Programmable Current Driver	6-146
9661	Quad Programmable Current Segment Driver ...	6-146
9662	LED/Lamp Digit Driver	6-147
9663	LED/Lamp Digit Driver	6-147
75491	MOS to LED Segment and Digit Driver	6-110
75492	MOS to LED Segment and Digit Driver	6-110
Glossary		7-102
Optional Packaging Outlines		7-104

INTRODUCTION

The application of linear integrated circuit technology to consumer electronics — pioneered by Fairchild with the μ A703 RF-IF amplifier in 1967 — is now a production reality.

Today, systems from video tape recorders to television receivers to automotive control systems are performing complex functions at greater component economies than at any previous time. Fairchild linear circuits have helped make this possible with:

- "STATE OF THE ART" monolithic technologies for design of complex consumer circuits
- High volume, low cost processing technology
- Co-operative product planning with customers to achieve the best system economies

At Fairchild, linear second generation technology has made possible advanced standard circuits such as the μ A758 phase locked loop stereo decoder and the μ A7800 series of three terminal voltage regulators. Other advanced products include custom camera circuits utilizing MOS, linear and digital circuitry and technology.

Many other complex linear circuits are being developed for consumer applications from automotive to television to calculators. A sampling of these will be found in the New Product section of this data catalog.

The Fairchild consumer linear team is working with customers to bring to the market linear circuits which will optimize cost and performance requirements of consumer electronic products — and they are being reliably produced in volume by the linear volume leader.

Contact us for your consumer needs. Put Fairchild to work for you.

CONSUMER CIRCUITS SELECTION GUIDE

DEVICE TYPE	AUTOMOTIVE & APPLIANCE CONTROL CIRCUITS				AUDIO CIRCUITS			
	μ A741	μ A742	μ A7350*	μ A7351*	Preamplifier		Power Amplifier	
					μ A739	μ A749	μ A705*	μ A706
Audio Driver								
Audio Pre-Amp, Single/Dual					X	X		
Audio Power Amp, Single/Dual							X	X
Audio Mute								
AFC/AFT								
AGC								
ACC								
Chroma Amplifier								
Chroma Demodulator								
Chroma Processor								
Comparator			X					
Converter								
DC Amplifier								
Detector								
Demodulator								
Electronic Attenuator								
IF Amplifier								
Limiter								
Luminance Amplifier								
Mixer								
Modulator								
Noise Gate								
Oscillator								
Operational Amplifier	X		X	X				
Phase Comparator								
Regulated Power Supply								
Sync Separator								
Stereo Switch								
RF Amplifier								
Tachometer			X					
Thyristor & Scr Control		X						
Tint Control								
Voltage Regulator								
Video Amplifier								
Zener Reference								

AM/FM RECEIVER CIRCUITS

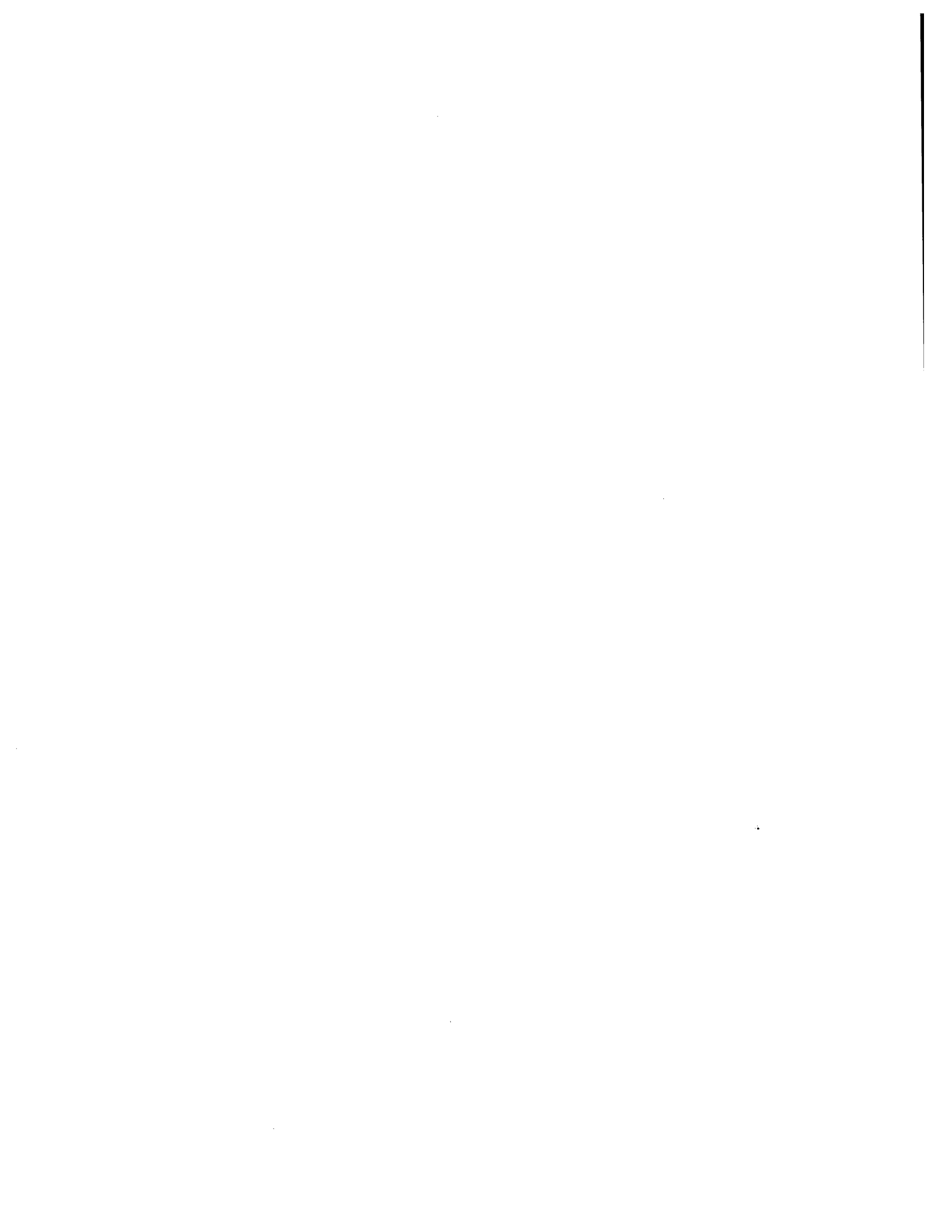
AM, FM, IF & Detector							Stereo Decoders				
μ A703	μ A720	μ A753	μ A757	2136*	3075	3076*	μ A732	μ A758	μ A767	μ A768	μ A769
					X						
							X	X	X	X	X
							X	X		X	
	X		X								
	X										
			X	X			X	X	X	X	X
X	X	X	X	X	X	X					
X		X	X	X	X	X					
X	X		X								
			X								
X	X						X	X	X	X	X
	X	X		X	X			X			
							X	X		X	
	X										
	X	X		X	X	X					

*See New Product Section

CONSUMER CIRCUITS SELECTION GUIDE

DEVICE TYPE	TV RECEIVER CIRCUITS								
	AFT	Chroma Processing							
	3064	2 Chip NTSC		3 Chip NTSC				2 Chip PAL	
		3066	3067	μ A746	μ A780	μ A781	1326*	μ A786	TBA510*
Audio Driver									
Audio Pre-Amp, Single/Dual									
Audio Power Amp, Single/Dual									
Audio Mute									
AFC/AFT	X								
AGC									
ACC		X							
Chroma Amplifier		X				X			X
Chroma Demodulator			X	X			X	X	
Chroma Processor		X			X				
Comparator									
Converter									
DC Amplifier	X								
Detector	X								
Demodulator									
Electronic Attenuator						X			X
IF Amplifier	X								
Limiter									
Luminance Amplifier									
Mixer									
Modulator									
Noise Gate									
Oscillator		X			X				
Operational Amplifier									
Phase Comparator									
Regulated Power Supply				X	X	X	X		
Sync Separator									
Stereo Switch									
RF Amplifier									
Tachometer									
Thyristor & Scr Control									
Tint Control			X		X				
Voltage Regulator					X				
Video Amplifier									
Zener Reference	X	X	X						

			VOLTAGE REGULATORS			VIDEO TAPE RECORDER SYSTEMS		
Luminance Amplifier	Sound Systems		Horizontal Oscillator					
TBA970*	μA704*	3065	TBA920*	μA723	μA7800	μA78M00*	μA733	μA796
	X	X						
	X							
	X	X						
X	X	X						X
	X	X						
	X	X						
X							X	
								X
			X					
			X					
			X					
		X						
			X					
	X	X		X	X	X		
							X	



μA703

RF-IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

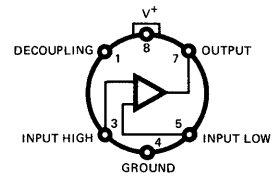
GENERAL DESCRIPTION — The μA703 is a monolithic RF-IF Amplifier constructed using the Fairchild Planar* epitaxial process and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

- 29 mmho MINIMUM FORWARD TRANSADMITTANCE
- 1.0 mmho/0.05 mmho MAXIMUM INPUT/OUTPUT CONDUCTANCE
- 18 pF/4.0 pF MAXIMUM INPUT/OUTPUT CAPACITANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

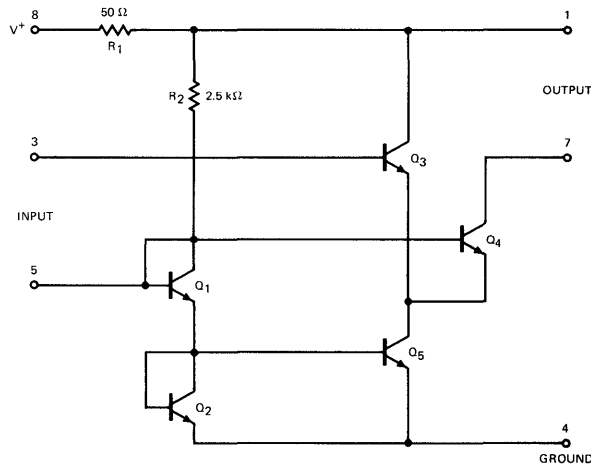
CONNECTION DIAGRAM
8-LEAD METAL CAN
 (TOP VIEW)
 PACKAGE OUTLINE 5Z



NOTE: Pin 4 connected to case.

ORDER INFORMATION	
TYPE	PART NO.
703C	703HC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

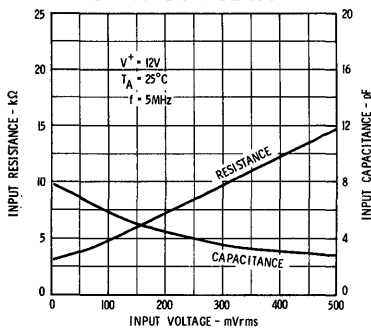
703C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$, $V_+ = 12 V$ unless otherwise specified)

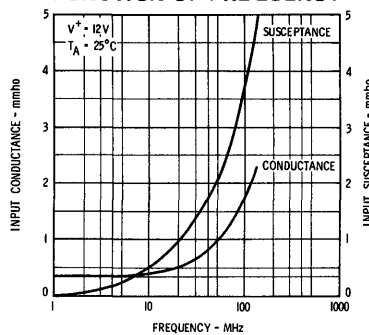
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_{IN} = 0$		9.0	14	mA
Power Consumption	$e_{IN} = 0$		110	170	mW
Quiescent Output Current	$e_{IN} = 0$	1.5	2.5	3.3	mA
Peak-to-Peak Output Current	$e_{IN} = 400 mV_{rms}$, $f = 1 kHz$	3.0			mA
Output Saturation Voltage	$I_7 = 2.5 mA$			1.7	V
Forward Transadmittance	$e_{IN} = 10 mV_{rms}$, $f = 1 kHz$	29	33		mmho
Input Conductance	$e_{IN} < 10 mV_{rms}$, $f = 10.7 MHz$		0.35	1.0	mmho
Input Capacitance	$e_{IN} < 10 mV_{rms}$, $f = 10.7 MHz$		9.0	18	pF
Output Conductance	$e_{OUT} = 100 mV_{rms}$, $f = 10.7 MHz$		0.03	0.05	mmho
Output Capacitance	$e_{OUT} = 100 mV_{rms}$, $f = 10.7 MHz$		2.0	4.0	pF
Noise Figure	$f = 10.7 MHz$, $R_S = 500 \Omega$		6.0		dB
	$f = 100 MHz$, $R_S = 500 \Omega$		8.0		dB

TYPICAL PERFORMANCE CURVES FOR 703C

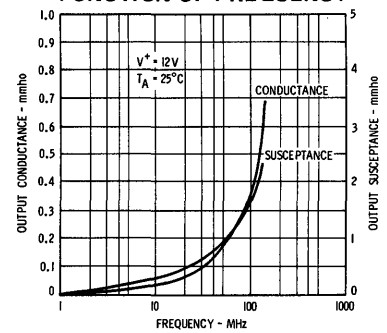
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



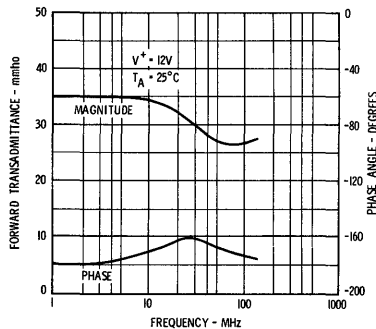
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



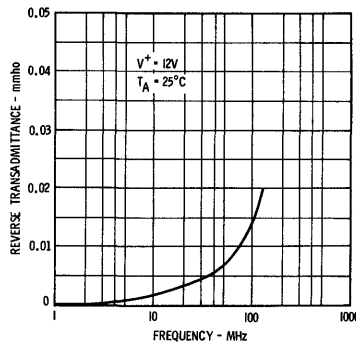
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



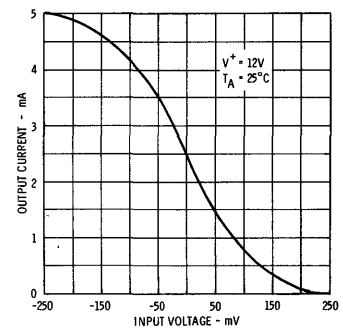
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



μA706

5 WATT AUDIO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

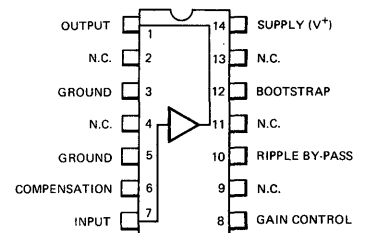
GENERAL DESCRIPTION — The μA706 monolithic 5.0 W Audio Amplifier is constructed using the Fairchild Planar* epitaxial process. It is ideally suited as an audio amplifier in automobile radios. Provided with adequate heat sinking, the circuit is optimized to provide 5.5 W (continuous output) into a 4.0 Ω speaker using a single 14 V supply. The circuit operates over the full automobile battery range of 6.0 V to 16 V. The μA706 incorporates such special features as self-centering bias, direct coupling to the input, low quiescent current, high input impedance and low distortion. Operation as a 5.0 W audio amplifier is achieved with minimal external components.

Other applications for the μA706 are home audio equipment, TV receivers and many industrial applications.

- OUTPUT POWER 5.5 W (14 V — 4 Ω)
- LOW DISTORTION
- LOW QUIESCENT CURRENT
- SELF CENTERING BIAS
- HIGH INPUT IMPEDANCE
- HIGH PEAK OUTPUT CURRENT
- HIGH IMMUNITY TO DAMAGE FROM SHORT-CIRCUITED LOAD†
- PIN-FOR-PIN REPLACEMENT FOR TBA641B

†The device will withstand repetitive short circuits across the speaker load if the absolute maximum junction temperature is not exceeded.

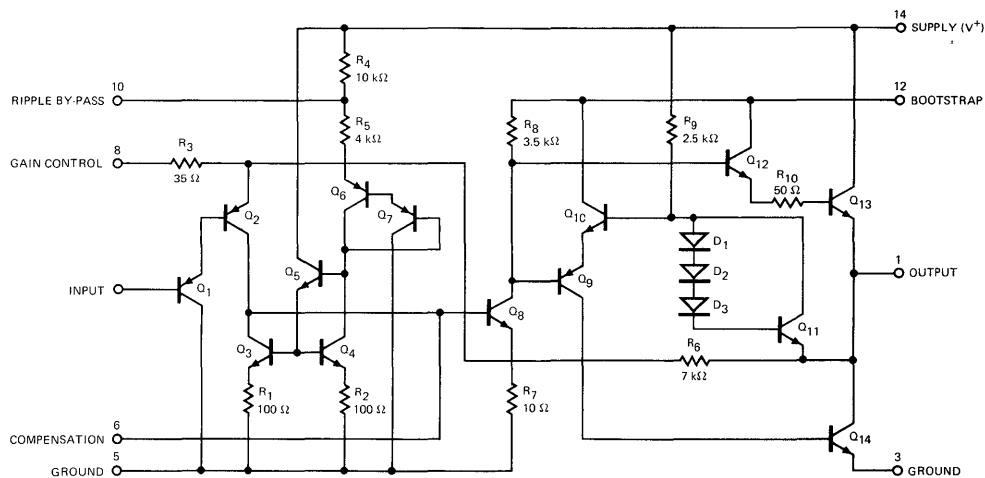
CONNECTION DIAGRAM 14-LEAD DIP (TOP VIEW) PACKAGE OUTLINE 9H, 9J



ORDER INFORMATION

TYPE	PART NO.
706AC	706APC
706BC	706BPC

EQUIVALENT CIRCUIT



○ = Pin Numbers

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A706

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (No Signal)	25 V
Supply Voltage	16 V
Input Voltage	-0.5 V to V^+
Peak Output Current	2.5 A
Operating Temperature Range	-30°C to +85°C
Storage Temperature	-55°C to +125°C
Maximum Junction Temperature	150°C
Power Dissipation ($T_C \leq 85^\circ\text{C}$)	5 W
Power Dissipation ($T_A \leq 25^\circ\text{C}$)	
Package Type A (706A)	1.7 W
Package Type B (706B)	2.3 W
Power Dissipation ($T_A \leq 85^\circ\text{C}$)	
Package Type A (706A)	0.9 W
Package Type B (706B)	1.2 W

PACKAGE THERMAL RESISTANCE

Thermal Resistance, Junction to Ambient	
Package Type A (706A)	73°C/W
Package Type B (706B)	55°C/W
Thermal Resistance, Junction to Case	
Package Type A (706A)	11°C/W
Package Type B (706B)	12°C/W

ELECTRICAL CHARACTERISTICS

706AC AND 706BC

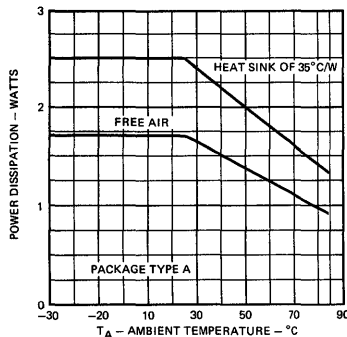
($V^+ = 14\text{ V}$, $R_L = 4\ \Omega$, $T_A = 25^\circ\text{C}$, $\theta_{C-A} = 13^\circ\text{C/W}$, Test Circuit 1, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Total Supply Current	$P_{OUT} = 0$	10	18	30	mA
Quiescent Current in Output Transistors	$P_{OUT} = 0$	7	15	27	mA
Input Bias Current			200	950	nA
DC Output Level	$R_S = 22\ \text{k}\Omega$	6.55	7.0	7.45	V
Voltage Gain, A_V	$R_B = 0\ \Omega$	43	46	49	dB
Output Power, P_{OUT}	THD = 10%, $f = 1\ \text{kHz}$, $A_V = 46\ \text{dB}$	4.5	5.5		W
Total Harmonic Distortion	$f = 1\ \text{kHz}$, $A_V = 46\ \text{dB}$				
	$P_{OUT} = 50\ \text{mW}$		0.3		%
	$P_{OUT} = 2.0\ \text{W}$		0.5		%
	$P_{OUT} = 4.5\ \text{W}$		3.0		%
Equivalent Input Noise Voltage	$R_S = 22\ \text{k}\Omega$, B.W. = 10 kHz		3.5		μV
Total Supply Current	$P_{OUT} = 4.5\ \text{W}$		510		mA
Input Impedance	$A_V = 46\ \text{dB}$, $f = 1\ \text{kHz}$		3.0		$\text{M}\Omega$

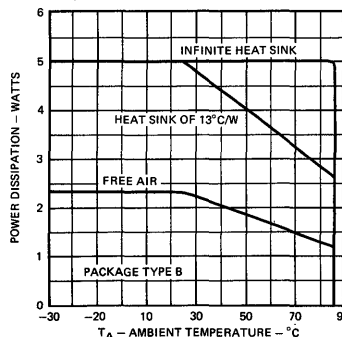
TYPICAL PERFORMANCE CURVES FOR 706AC AND 706BC

($T_A = 25^\circ\text{C}$, $\theta_{C-A} = 13^\circ\text{C/W}$, Test Circuit 1, $A_V = 46\ \text{dB}$)

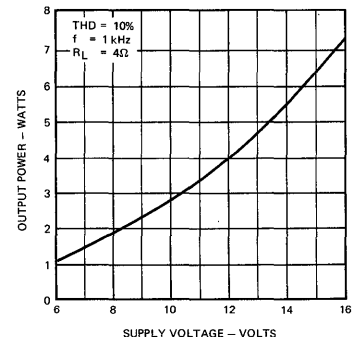
MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (FOR PACKAGE TYPE A)



MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (FOR PACKAGE TYPE B)

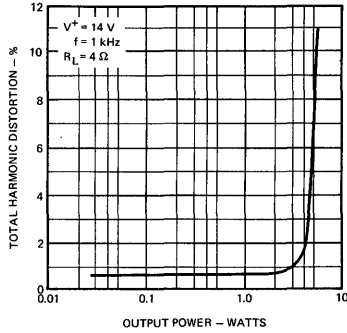


OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

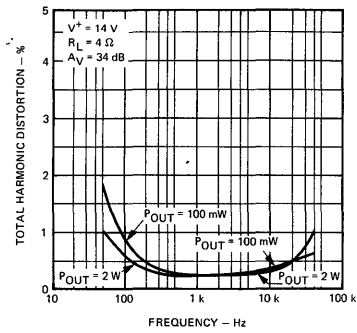


TYPICAL PERFORMANCE CURVES FOR 706AC AND 706BC (Cont'd)

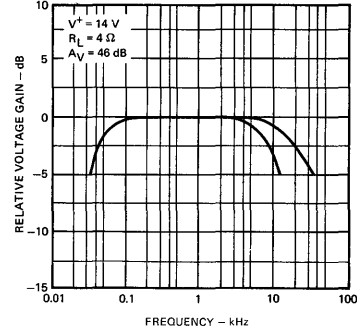
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



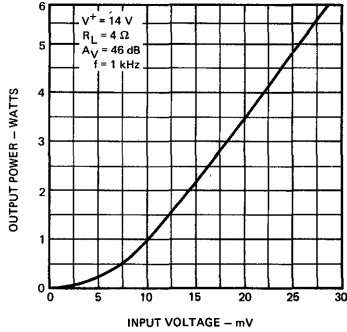
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



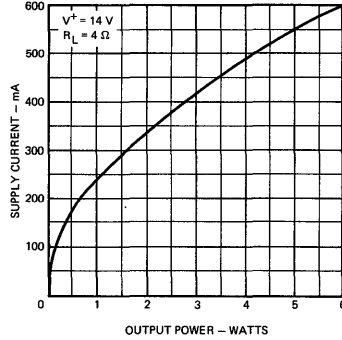
RELATIVE VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



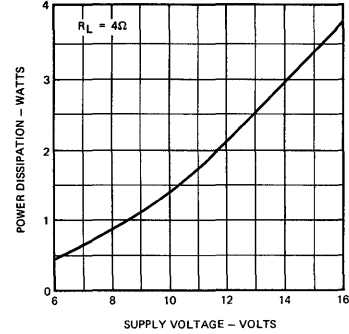
OUTPUT POWER AS A FUNCTION OF INPUT VOLTAGE



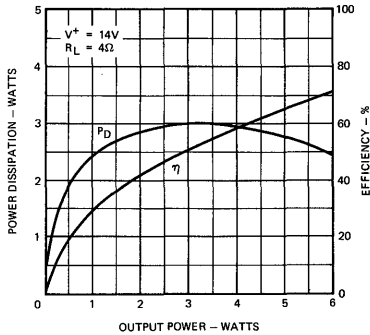
SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER



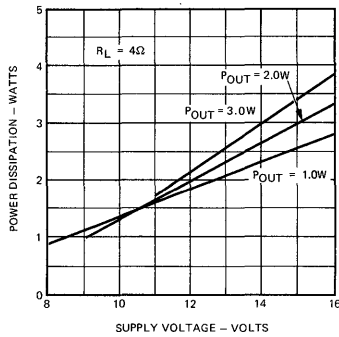
MAXIMUM POWER DISSIPATION BY THE INTEGRATED CIRCUIT AS A FUNCTION OF SUPPLY VOLTAGE



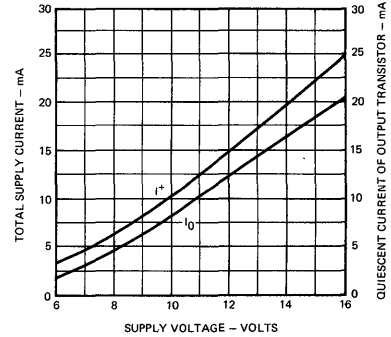
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER



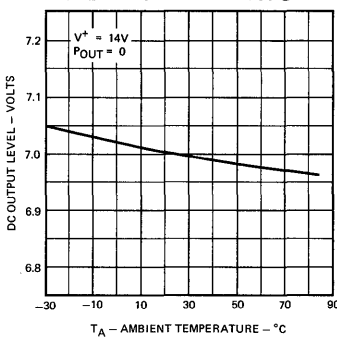
POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE



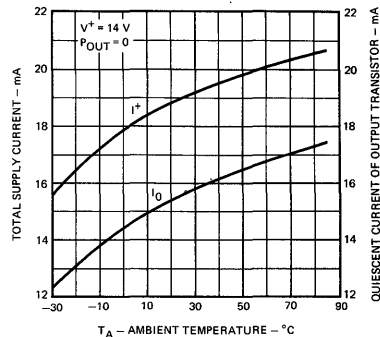
TOTAL SUPPLY CURRENT AND QUIESCENT CURRENT OF OUTPUT TRANSISTOR AS A FUNCTION OF SUPPLY VOLTAGE



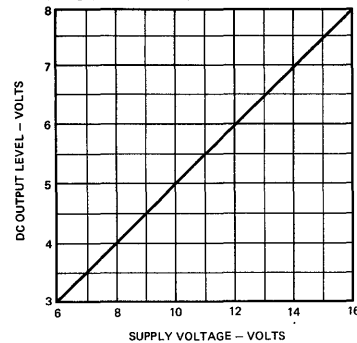
DC OUTPUT LEVEL AS A FUNCTION OF AMBIENT TEMPERATURE



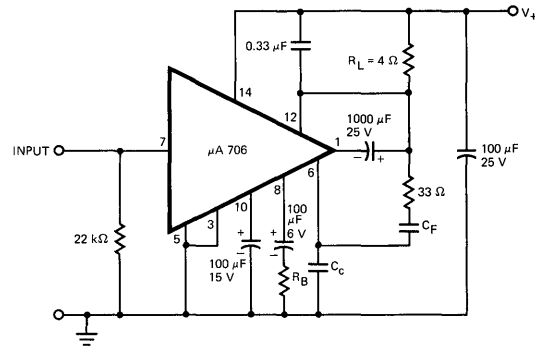
TOTAL SUPPLY CURRENT AND QUIESCENT CURRENT OF OUTPUT TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE



DC OUTPUT LEVEL AS A FUNCTION OF SUPPLY VOLTAGE

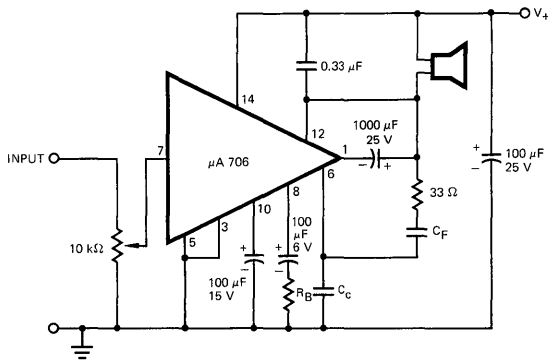


TEST CIRCUIT 1 ($A_V = 46 \text{ dB}$, $R_B = 0 \Omega$, $C_C = 1.5 \mu\text{F}$, $C_F = 150 \text{ pF}$)



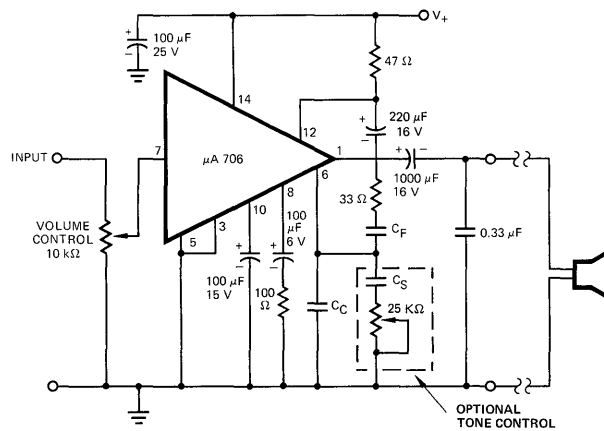
TYPICAL AUDIO APPLICATIONS

5 WATT AUDIO AMPLIFIER WITH MINIMUM COMPONENT COUNT



A_V	34 dB		46 dB	
	10 kHz	20 kHz	10 kHz	20 kHz
R_B	100 Ω	100 Ω	0 Ω	0 Ω
C_C	10 nF	6.8 nF	2.7 nF	1.5 nF
C_F	1 nF	470 pF	330 pF	150 pF

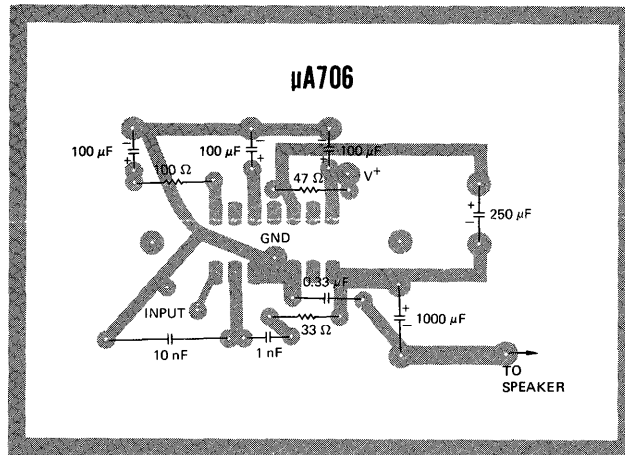
5 WATT AUDIO AMPLIFIER WITH LOAD CONNECTED TO GROUND



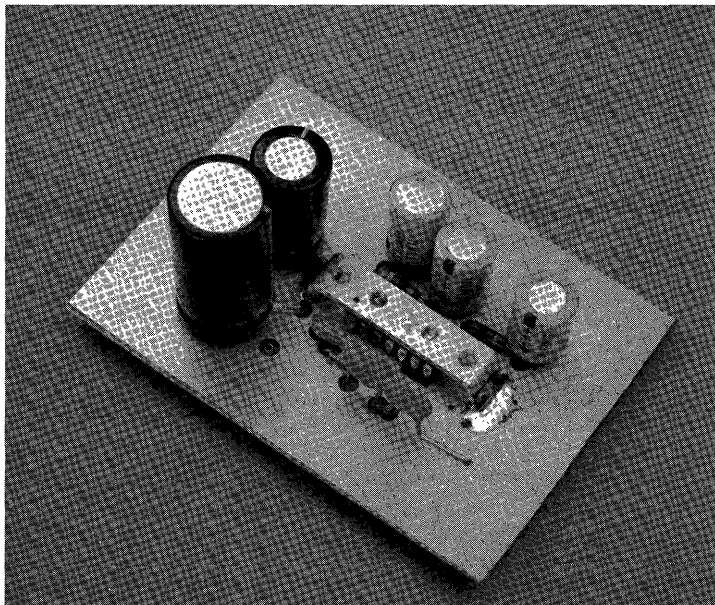
A_V	34 dB	46 dB
C_S	27 nF	5.6 nF

Note: C_S selected for 3 dB at 4 kHz.

A PC BOARD LAYOUT FOR THE 5 WATT AUDIO AMPLIFIER



PHOTOGRAPH OF THE μ A706 IN A TYPICAL APPLICATION



μA720

AM RADIO SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUITS

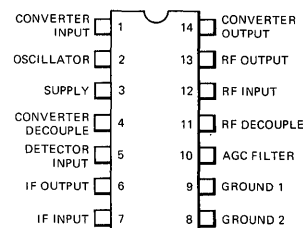
GENERAL DESCRIPTION — The μA720 is a monolithic AM Radio Receiver System made with the patented Fairchild Planar* epitaxial process. The device contains two amplifiers, a mixer-oscillator, an AGC detector and a voltage regulator. It is intended for superheterodyne AM receiver applications. Since all parts of the circuit are accessible separately, the μA720 can be used in a variety of other applications. The voltage regulator is protected against short term overvoltage transients.

- **AM-RF OSCILLATOR-CONVERTER, IF AMPLIFIER ON ONE CHIP**
- **REGULATED SUPPLY**
- **OVERVOLTAGE PROTECTION**
- **AMPLIFIERS SEPARATELY ACCESSIBLE**
- **AGC FOR RF STAGE**

ABSOLUTE MAXIMUM RATINGS

Operating Voltage	16V
Current into Supply Terminal (Pin 3)	40mA
Power Dissipation (Note 1)	670mW
Current into RF Output Terminal (Pin 13)	20mA
Current into RF Input Terminal (Pin 12)	10mA
Current into IF Input Terminal (Pin 7)	10mA
Current into or out of Detector Input Terminal (Pin 5)	±10mA
Current into AGC Filter Terminal (Pin 10)	10mA
Negative Voltage on RF Input, IF Input, and Detector Input Terminals	-5V
Negative Voltage on Converter Input Terminal	0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperatures	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C

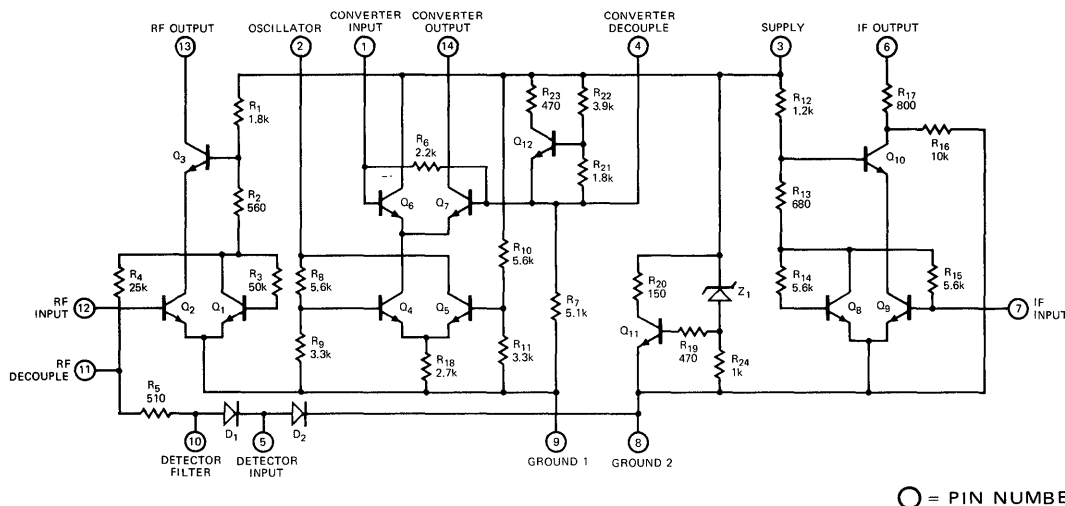
CONNECTION DIAGRAM 14-LEAD DIP (TOP VIEW) PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
720C	720DC
720C	720PC

EQUIVALENT CIRCUIT



○ = PIN NUMBER

See notes on following page.

*Planar is a patented Fairchild process

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A720

720C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_+ = 12\text{ V}$, Test Circuit 1, unless otherwise indicated)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC CHARACTERISTICS (Oscillator OFF, S_1 in Pos 2, S_3 in Pos 2, unless otherwise indicated)					
Voltage on Supply Terminal (V_3)	$I_2 + I_3 = 15\text{ mA}$	6.6	7.0	7.5	V
Voltage on Supply Terminal (V_3)	$I_2 + I_3 + I_{13} + I_{14} = 22\text{ mA}$, S_3 in Pos 1	6.6	7.0	7.5	V
Current into Oscillator and Supply Terminal ($I_2 + I_3$)	$V_3 = 5\text{ V}$, S_1 in Pos 1	4.0	6.0	8.0	mA
Current into Oscillator, Supply, RF Out, and Conv. Out Terminals ($I_2 + I_3 + I_{13} + I_{14}$)	$V_3 = 5\text{ V}$, S_1 in Pos 1, S_3 in Pos 1	6.0	9.0	12	mA
Oscillator Current (I_2)	$I_2 + I_3 = 15\text{ mA}$		1.2		mA
RF Output Current (I_{13})	$I_2 + I_3 = 15\text{ mA}$		4.0		mA
IF Output Current (I_6)	$I_2 + I_3 = 15\text{ mA}$		4.0		mA
Voltage on Converter Input (V_1)	$I_2 + I_3 = 15\text{ mA}$		5.8		V
Voltage on IF Input (V_7)	$I_2 + I_3 = 15\text{ mA}$		0.75		V
Voltage on RF Input (V_{12})	$I_2 + I_3 = 15\text{ mA}$		0.67		V
Internal Power Dissipation	$I_2 + I_3 + I_{13} + I_{14} = 22\text{ mA}$, S_3 in Pos 1		200		mW

AC CHARACTERISTICS (Signals are measured at the device pins)

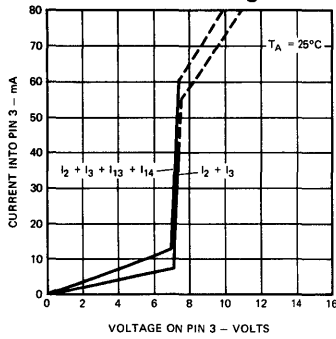
RF Transconductance ($g_{mRF} = i_{13}/e_{12}$)	$f_{12} = 1\text{ MHz}$, $e_{12} = 100\ \mu\text{VRMS}$, $e_5 = 0$ Oscillator OFF	80	120	180	mmhos
RF Input Resistance (R_{IN12})	$f_{12} = 1\text{ MHz}$, $e_{12} = 100\ \mu\text{VRMS}$, S_2 in Pos 2	500	1000		Ω
RF Input Capacitance (C_{IN12})	$f_{12} = 1\text{ MHz}$, $e_{12} = 100\ \mu\text{VRMS}$, S_2 in Pos 2		50		pF
RF Output Resistance (R_{OUT13})	$f_{13} = 1\text{ MHz}$		50		k Ω
RF Output Capacitance (C_{OUT13})	$f_{13} = 1\text{ MHz}$		10		pF
RF Noise Voltage, $\sqrt{e_n^2}$	Referred to Input, $R_S = 50\ \Omega$, $f_{13} = 1\text{ MHz}$		3.0		nV/ $\sqrt{\text{Hz}}$
Detector Input Voltage (e_5)	RF Stage Gain Reduction				
	$\Delta g_{mRF} = 3\text{ dB}$, $f_{13} = 1\text{ MHz}$, $f_5 = 260\text{ kHz}$ $\Delta g_{mRF} = 40\text{ dB}$, $f_{13} = 1\text{ MHz}$, $f_5 = 260\text{ kHz}$	140 220	180 270	250 330	mVRMS mVRMS
IF Transconductance ($g_{mIF} = i_e/e_7$)	$f_7 = 260\text{ kHz}$, $e_7 = 1\text{ mVRMS}$	50	90	130	mmhos
IF Input Resistance (R_{IN7})	$f_7 = 260\text{ kHz}$	600	1000		Ω
IF Input Capacitance (C_{IN7})	$f_7 = 260\text{ kHz}$		70		pF
IF Output Resistance (R_{OUT6})	$f_6 = 260\text{ kHz}$		10		k Ω
IF Output Capacitance (C_{OUT6})	$f_6 = 260\text{ kHz}$		8		pF
Converter Transconductance ($g_{mCON} = i_{14}/e_1$)	$f_1 = 1\text{ MHz}$, $e_1 = 1\text{ mVRMS}$, $f_{14} = f_{\text{oscillator}} - f_1$	1.5	2.5	3.4	mmhos
Converter Input Resistance (R_{IN1})	$f_1 = 1\text{ MHz}$	1000	1400		Ω
Converter Input Capacitance (C_{IN1})	$f_1 = 1\text{ MHz}$		8		pF
Converter Output Resistance (R_{OUT14})	$f_{14} = 260\text{ kHz}$		50		k Ω
Converter Output Capacitance (C_{OUT14})	$f_{14} = 260\text{ kHz}$		10		pF
Oscillator Output Voltage (e_2)			1.2		VRMS

Note 1. Rating applies for ambient temperatures to $+70^\circ\text{C}$. Derate at $8.3\text{ mW}/^\circ\text{C}$ between $+70^\circ\text{C}$ and $+85^\circ\text{C}$.

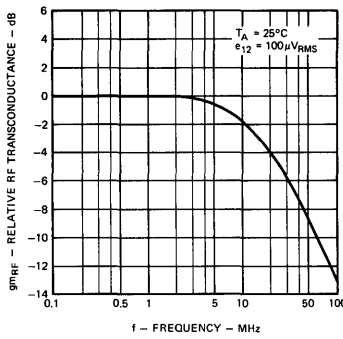
FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A720

TYPICAL PERFORMANCE CURVES FOR 720C TEST CIRCUIT 1, unless otherwise specified.

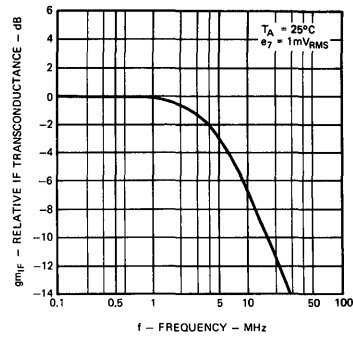
CURRENTS AS A FUNCTION OF VOLTAGE (V_3)



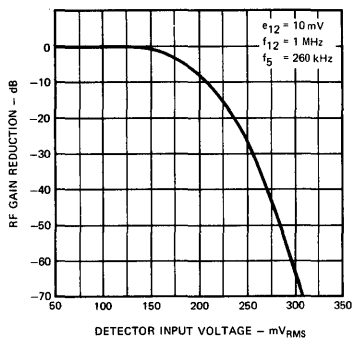
RF TRANSDUCANCE AS A FUNCTION OF FREQUENCY



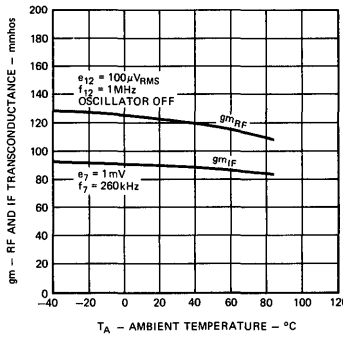
IF TRANSDUCANCE AS A FUNCTION OF FREQUENCY



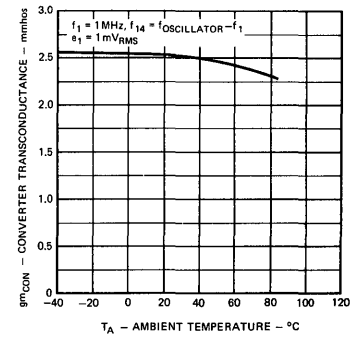
RF AGC CHARACTERISTIC



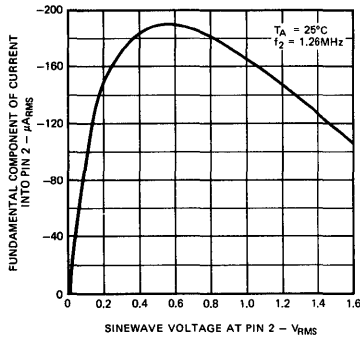
RF AND IF TRANSDUCANCE AS A FUNCTION OF TEMPERATURE



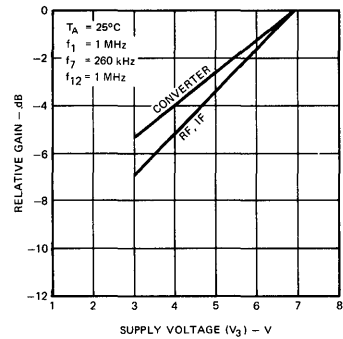
CONVERTER TRANSDUCANCE AS A FUNCTION OF TEMPERATURE



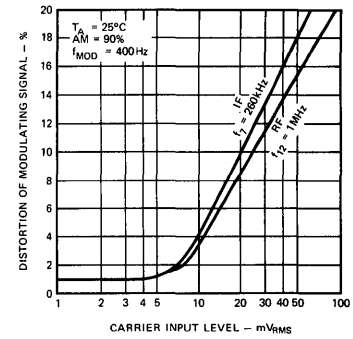
OSCILLATOR TERMINAL (PIN 2) V/I CHARACTERISTIC



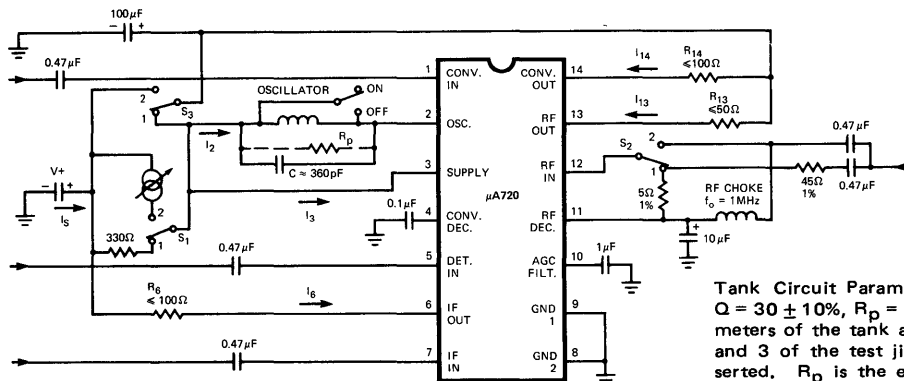
RELATIVE GAIN AS A FUNCTION OF SUPPLY TERMINAL VOLTAGE



TOTAL HARMONIC DISTORTION OF THE MODULATING SIGNAL AS A FUNCTION OF CARRIER INPUT LEVEL

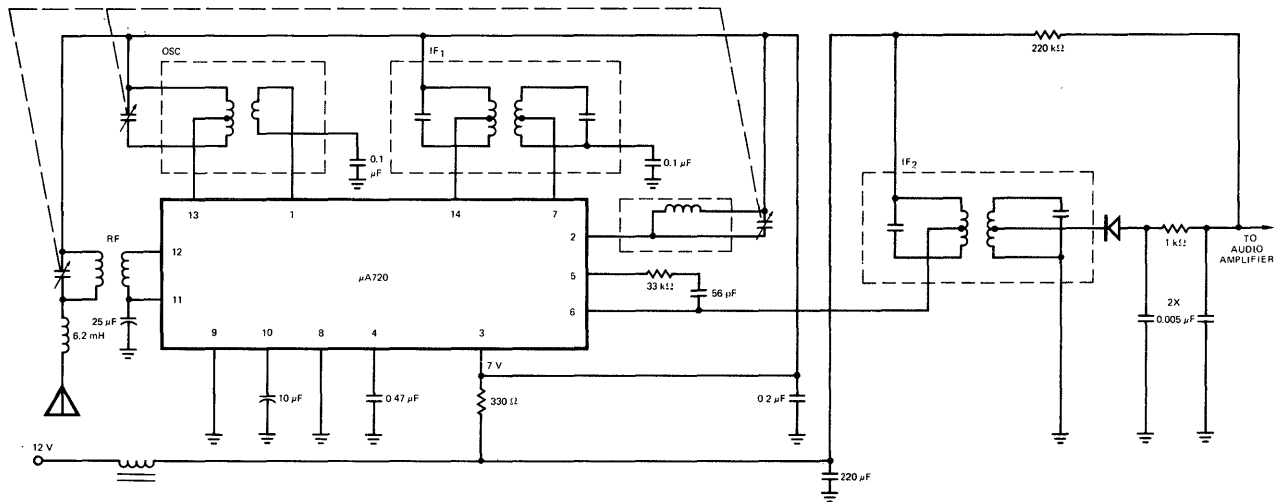


TEST CIRCUIT 1



Tank Circuit Parameters: $f_0 = 1.26\text{MHz}$, $Q = 30 \pm 10\%$, $R_p = 10k\Omega \pm 5\%$. The parameters of the tank are measured at pins 2 and 3 of the test jig without a device inserted. R_p is the effective parallel resistance at resonance.

AM RADIO (CAPACITOR TUNED)



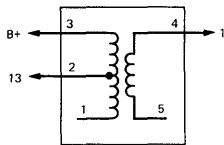
VARIABLE CAPACITOR (AIR VARICON)

ANT & RF 13 pF ~ 190 pF
 OSC 12 pF ~ 80 pF

ANTENNA COIL

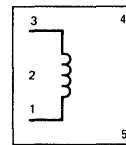
10 mm ϕ x 120 mm Ferrite Antenna

RF COIL



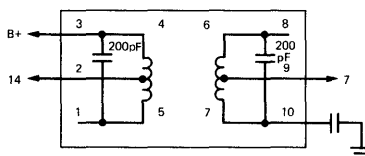
1-2 44 Turns
 2-3 81 Turns
 4-5 8 Turns

OSC COIL



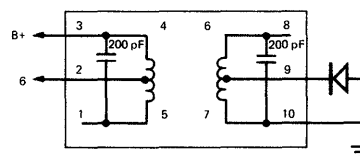
1-3 95 Turns

1st. IF COIL



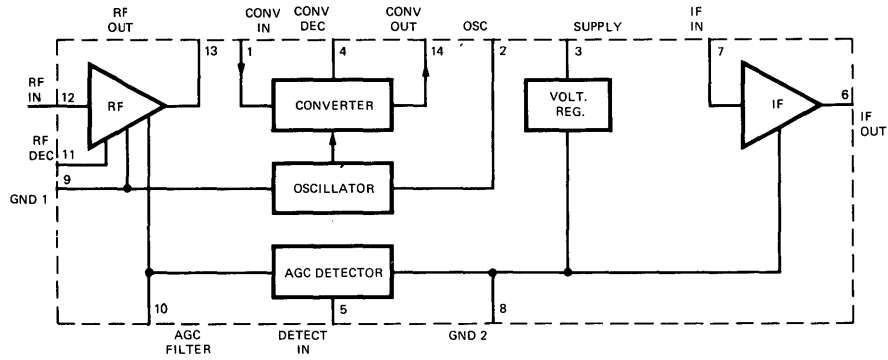
1-2 120 Turns
 2-3 80 Turns
 9-10 15 Turns
 9-8 185 Turns
 Core: $k = .021$

2nd. IF COIL

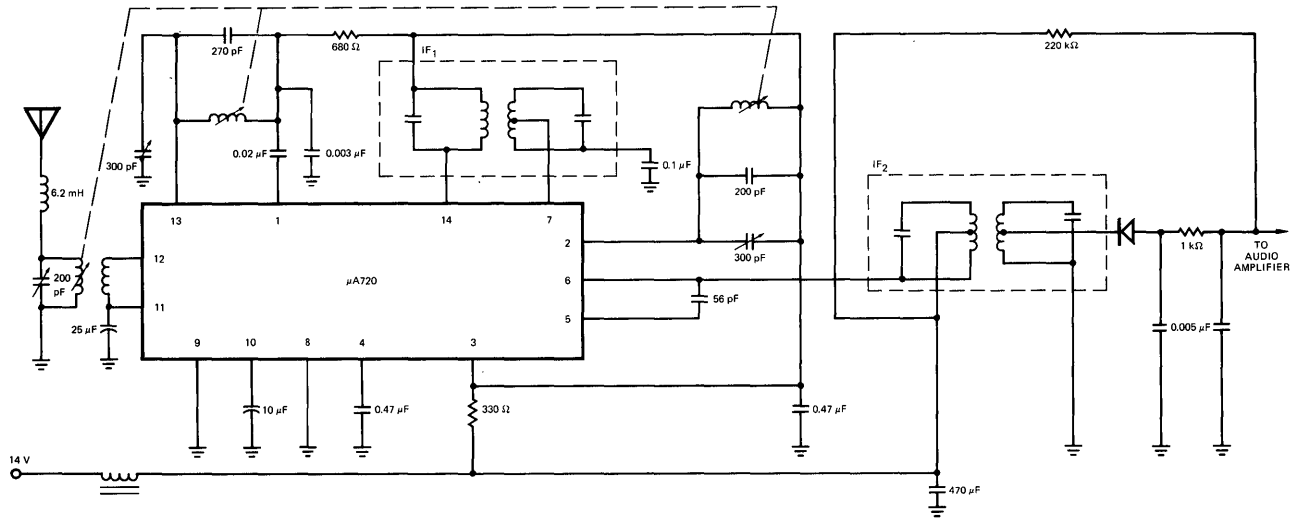


1-2 120 Turns
 2-3 80 Turns
 9-10 30 Turns
 9-8 170 Turns
 Core: $k = 0.021$

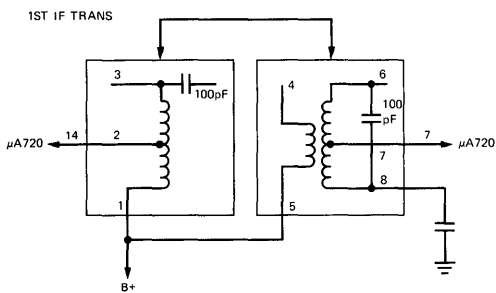
BLOCK DIAGRAM AND TYPICAL APPLICATIONS



AM CAR RADIO (SLUG TUNED)

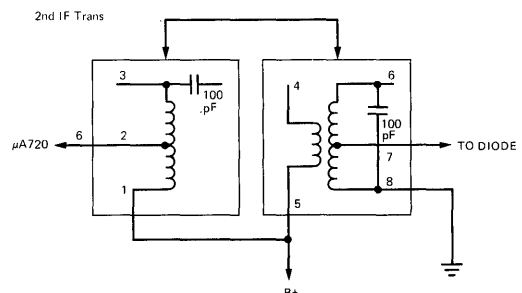


1st. IF TRANSFORMER



- 1-2 223 Turns
- 1-3 350 Turns
- 4-5 8 Turns
- 7-8 10 Turns
- 6-8 350 Turns
- $Q_0 = 56$
- 10 x 10 mm Core

2nd. IF TRANSFORMER



- 1-2 67 Turns
- 1-3 350 Turns
- 4-5 8 Turns
- 7-8 40 Turns
- 6-8 350 Turns
- $Q_0 = 58$
- 10 x 10 mm Core

μA732 • μA768

FM STEREO MULTIPLEX DECODERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA732 and μA768 are monolithic FM Stereo Multiplex Decoder systems constructed using the Fairchild Planar* epitaxial process. They are electrically identical; however, the right and left stereo outputs are reversed for the μA768. These integrated circuits demodulate a stereo multiplex signal into the right and left audio channels while inherently suppressing SCA frequency components. Internal provision is made for interstation audio muting, stereo/mono mode switching and driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement make the μA732 and μA768 suitable for all line-operated and automotive FM stereo multiplex applications.

- 45 dB CHANNEL SEPARATION
- 55 dB STORECAST REJECTION WITHOUT SCA FILTERS
- HIGH CURRENT STEREO INDICATOR LAMP DRIVER
- OPERATION WITH 8 V TO 14 V SUPPLIES
- INTERNAL STEREO SWITCHING AND AUDIO MUTING FUNCTIONS

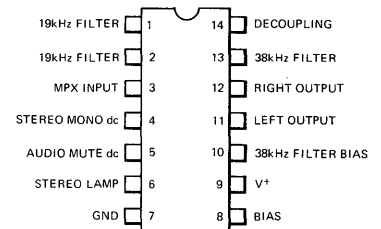
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver (Note 2)	100 mA
Internal Power Dissipation	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	732DC, 768DC +300°C
Molded DIP (Soldering, 10 seconds)	732PC, 768PC +260°C

CONNECTION DIAGRAM

**14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A**

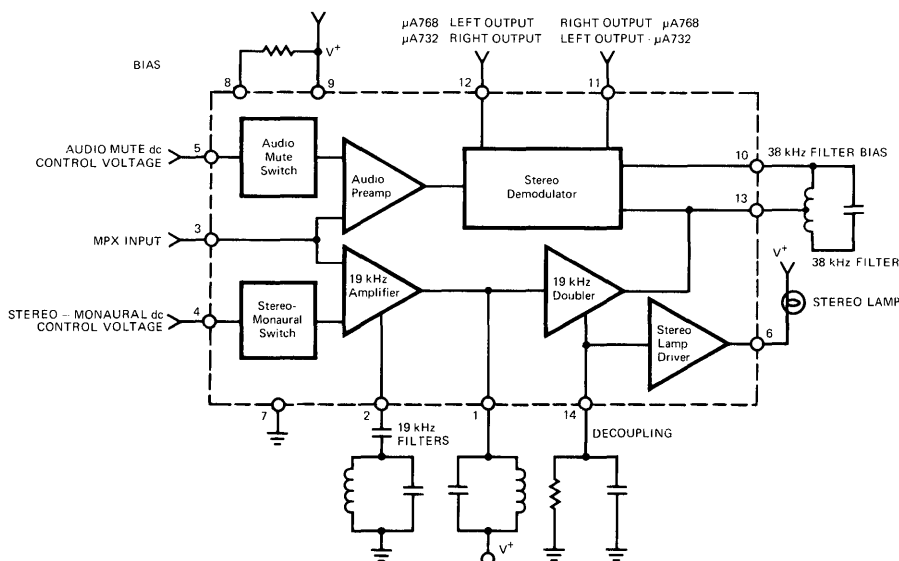
μA732



ORDER INFORMATION

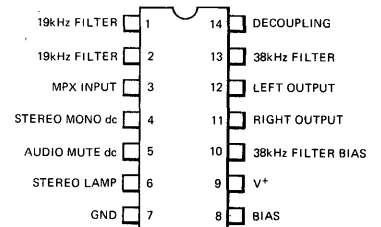
TYPE	PART NO.
732C	732DC
732C	732PC

BLOCK DIAGRAM (μA732 and μA768)



**14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A**

μA768



ORDER INFORMATION

TYPE	PART NO.
768C	768DC
768C	768PC

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A732 • μ A768

732C AND 768C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_+ = +12\text{ V}$, $200\text{ mV}_{\text{RMS}}$ standard stereo multiplex signal applied to input, unless otherwise specified (Note 3). Refer to Test Circuit of Figure 1.)

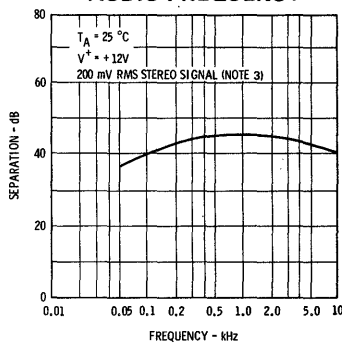
PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Current		11	18	mA
Input Resistance	12	20		$k\Omega$
Stereo Separation				
$f = 100\text{ Hz}$		40		dB
$f = 1\text{ kHz}$	30	45		dB
$f = 10\text{ kHz}$	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/ V
67 kHz Storecast Rejection (Note 4)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV_{RMS}
Stereo Indicator Lamp off	4.0	8.0		mV_{RMS}
DC Voltage Required at Pin 4 for Stereo-Monaural Switching				
Stereo on	1.0	1.25	1.5	Vdc
Stereo off	0.6	0.85	1.0	Vdc
DC Voltage Required at Pin 5 for Audio Mute Switching				
Audio on	1.0	1.20	1.5	Vdc
Audio off	0.6	0.85	1.0	Vdc
Mute Attenuation of Audio	45	55		dB
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

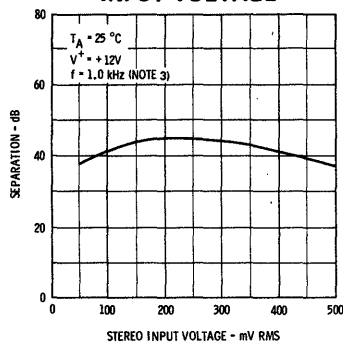
- Power supply transients up to 22 V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15 V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.
- Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.
- "Standard Stereo Multiplex Signal" here refers to a 200 mV RMS (0.56 V p-p) composite stereo signal including 10% pilot with $L = 1$ and $R = 1$ as described in the FCC Rules on FM Broadcasting.
- Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES FOR 732C AND 768C

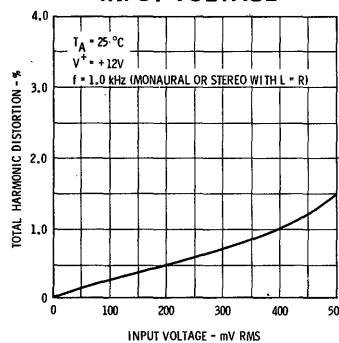
SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



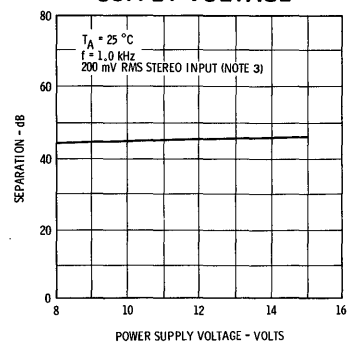
1 kHz SEPARATION AS A FUNCTION OF COMPOSITE INPUT VOLTAGE



1 kHz DISTORTION AS A FUNCTION OF INPUT VOLTAGE



1 kHz SEPARATION AS A FUNCTION OF POWER SUPPLY VOLTAGE



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A732 • μ A768

μ A732 • μ A768 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

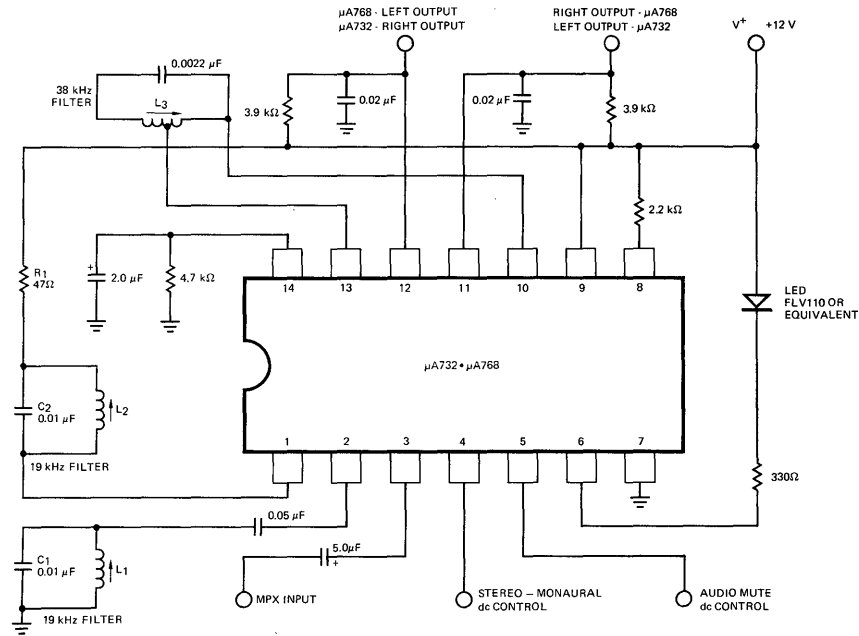
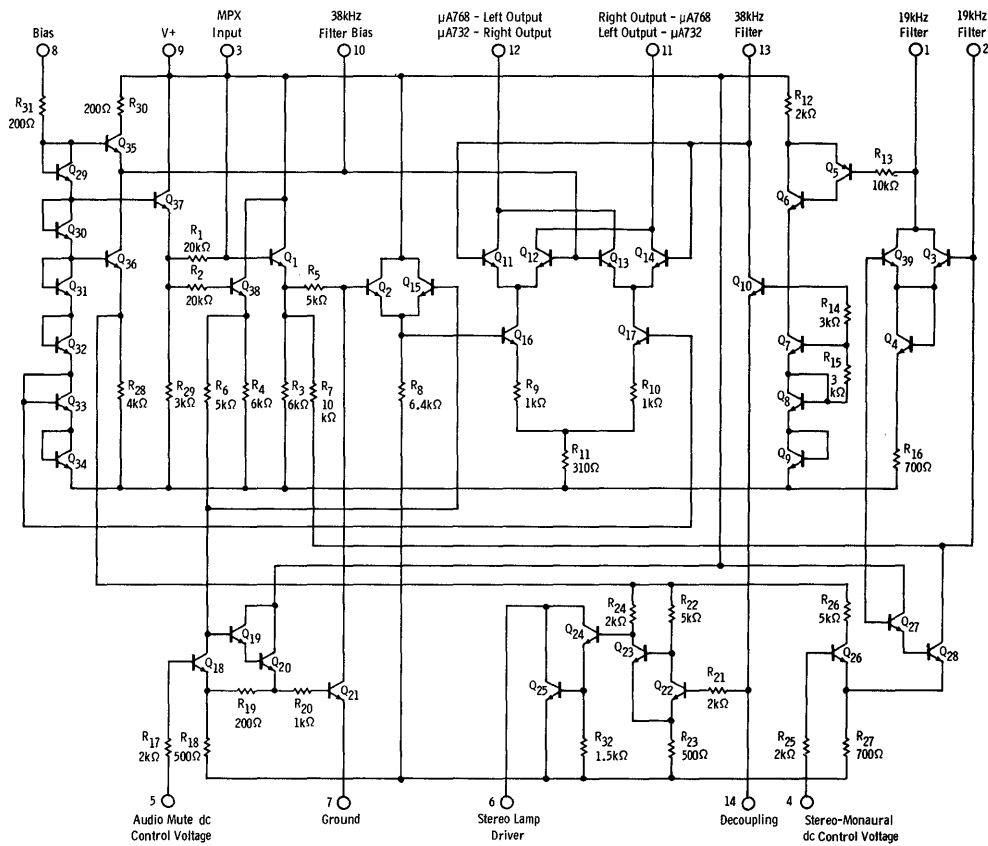


Fig. 1

NOTES:

- (1) Capacitors C_1 , C_2 and C_3 should be polystyrene or mylar.
- (2) Coils L_1 and L_2 are 7.0 mH nominal with $Q = 60$ (Miller #1361 or equivalent).
- (3) Coil L_3 is 8.0 mH nominal with $Q = 80$, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
- (4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19 kHz sensitivity.

μ A732 • μ A768 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA739

DUAL LOW NOISE AUDIO PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

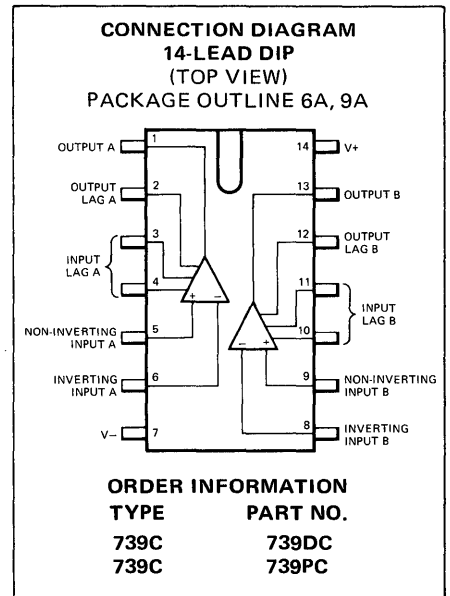
GENERAL DESCRIPTION – The μA739 consists of two identical monolithic Operational Amplifiers using the Fairchild Planar* epitaxial process. These low noise, high gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltages and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

- SINGLE OR DUAL SUPPLY OPERATION
- LOW NOISE FIGURE, 2.0 dB
- HIGH GAIN, 20,000 V/V
- LARGE COMMON MODE RANGE, ±11 V
- EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE
- NO LATCH-UP
- OUTPUT SHORT CIRCUIT PROTECTED

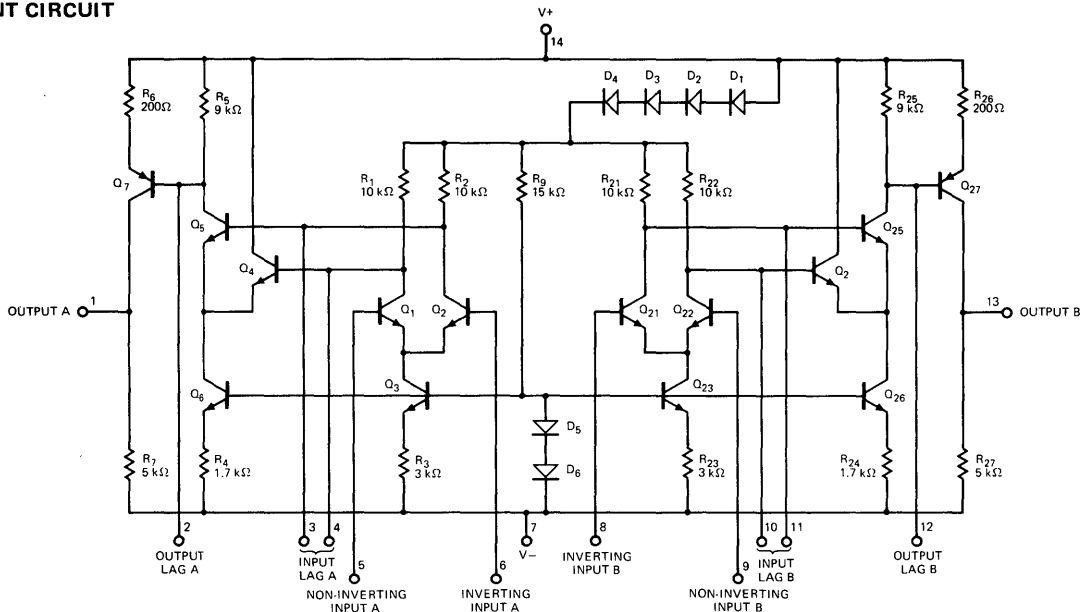
ABSOLUTE MAXIMUM RATINGS

Supply Voltage
 Internal Power Dissipation (Note 1)
 Differential Input Voltage
 Input Voltage (Note 2)
 Storage Temperature Range
 Operating Temperature Range
 Lead Temperature
 Hermetic DIP (Soldering, 60 seconds)
 Molded DIP (Soldering, 10 seconds)
 Output Short-Circuit Duration, $T_A = 25^\circ\text{C}$ (Note 3)

±18 V
 670 mW
 ±5 V
 ±15 V
 -55°C to +125°C
 0°C to +70°C
 300°C
 260°C
 30 seconds



EQUIVALENT CIRCUIT



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A739

739C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $R_L = 50\text{ k}\Omega$ to Pin 7, $T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300	2000	nA
Input Resistance		37	150		k Ω
Large Signal Voltage Gain	$V_{OUT} = \pm 5.0V$	6500	20,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-14	-15		V
Output Resistance	$f = 1.0\text{kHz}$		5.0		k Ω
Input Voltage Range		± 10	± 11		V
Common Mode Rejection Ratio	$R_S \leq 10\text{k}\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{k}\Omega$		50		$\mu\text{V/V}$
Power Consumption	$V_{OUT} = 0$		270	420	mW
Supply Current	$V_{OUT} = 0$		9.0	14	mA
Broadband Noise Figure	$R_S = 5.0\text{k}\Omega$, BW = 10Hz to 10kHz		2.0		dB
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20\text{mV}$		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20\text{mV}$		0.3		μs
Slew Rate (unity gain) [See Figure 2]	$C_1 = 0.1\mu\text{F}$, $R_1 = 4.7\Omega$		1.0		V/ μs
Channel Separation (See Figure 3)	$R_S \leq 10\text{k}\Omega$, $f = 10\text{kHz}$		140		dB

The following specifications apply for $V_S = \pm 4.0V$, $T_A = 25^\circ\text{C}$

Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300		nA
Supply Current	$V_{OUT} = 0$		2.5		mA
Power Consumption	$V_{OUT} = 0$		20		mW
Large Signal Voltage Gain	$V_{OUT} = \pm 1.0V$	2500	15,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		-3.6	-4.0		V

NOTES:

1. Rating applies at ambient temperature below 70°C .
2. For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

PULSE RESPONSE WAVEFORMS

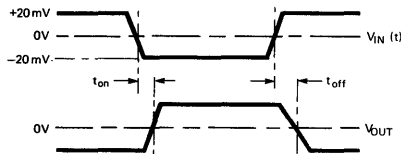


Fig. 1

FREQUENCY RESPONSE TEST CIRCUIT

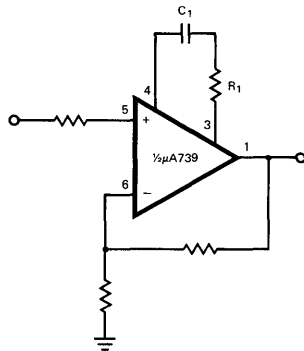


Fig. 2

CHANNEL SEPARATION TEST CIRCUIT

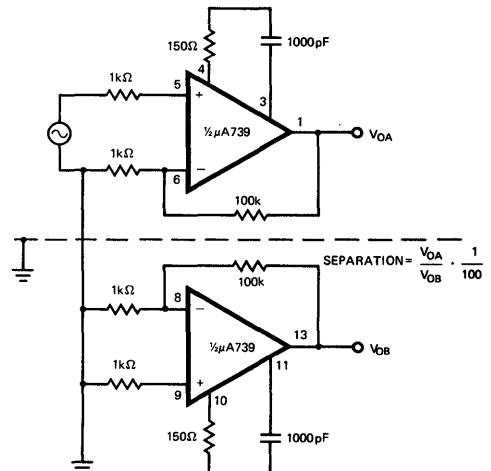
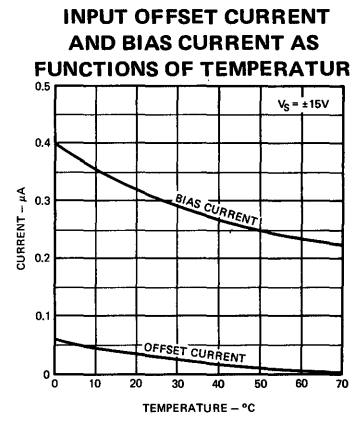
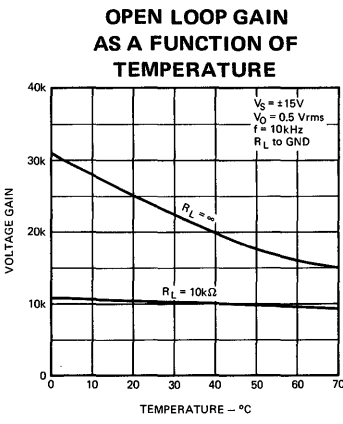
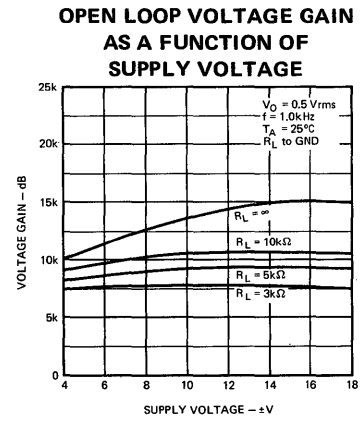
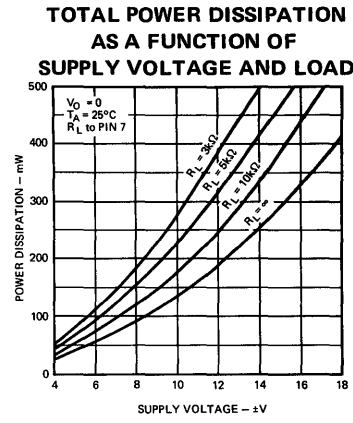
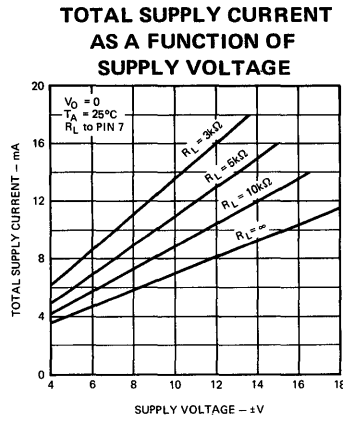
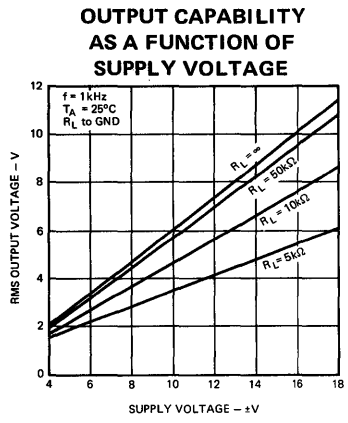
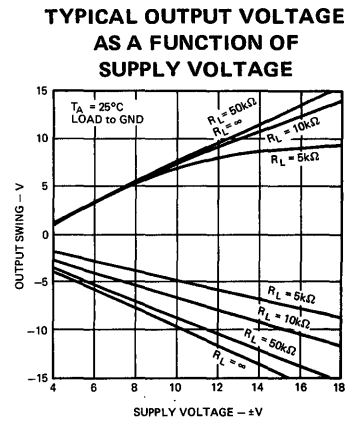
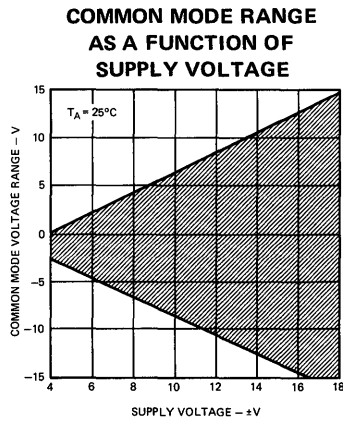
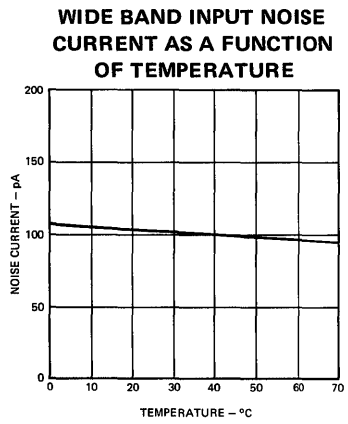
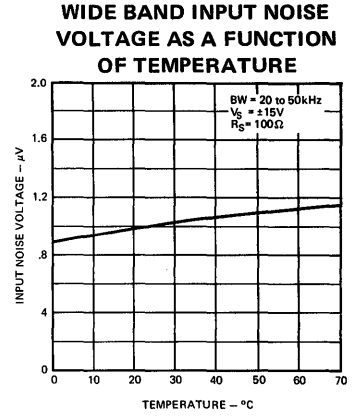
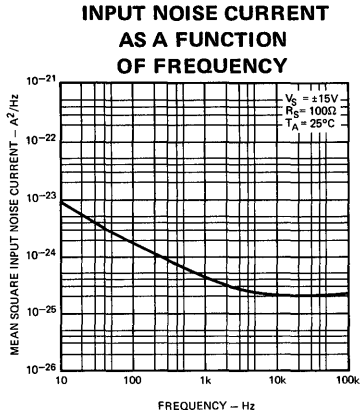
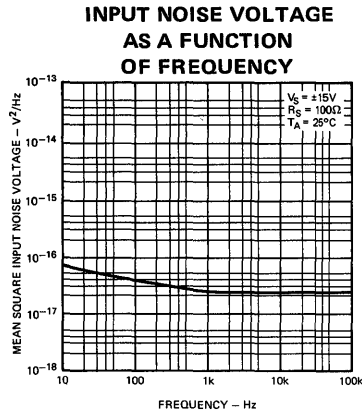


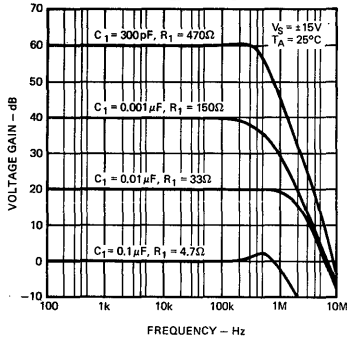
Fig. 3

TYPICAL PERFORMANCE CURVES FOR 739C

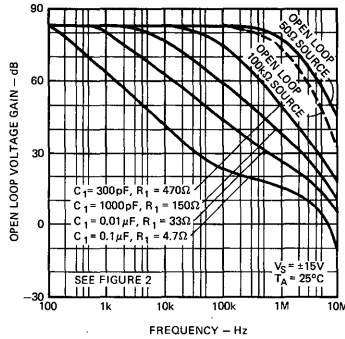


TYPICAL PERFORMANCE CURVES FOR 739C

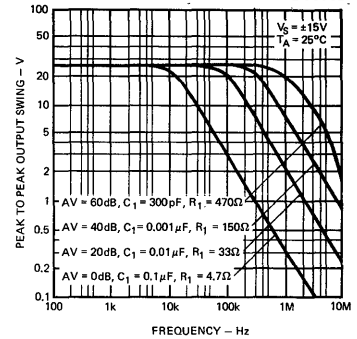
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



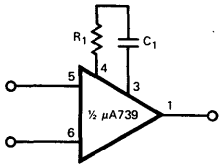
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



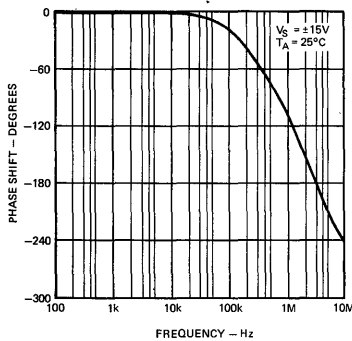
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



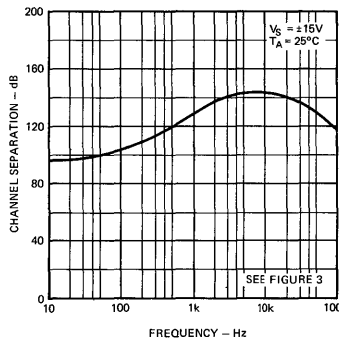
FREQUENCY COMPENSATION NETWORK



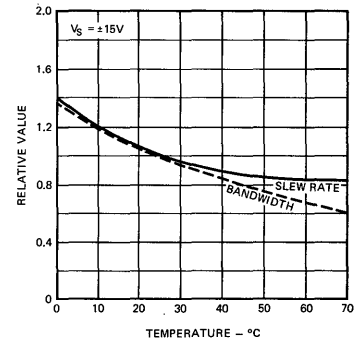
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



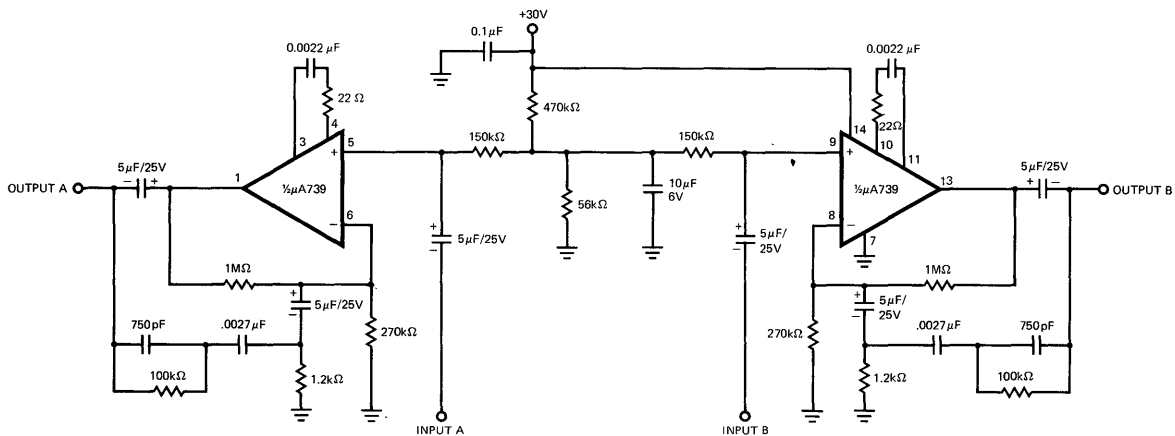
CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY



CHANGE OF AC CHARACTERISTICS WITH TEMPERATURE



TYPICAL APPLICATION
STEREO PHONO PREAMPLIFIER – RIAA EQUALIZED



TYPICAL PERFORMANCE

Gain 40dB at 1 kHz, RIAA equalized
Input overload point, 80mV rms
Noise level, $2 \mu\text{V}$ referred to input
Signal to noise ratio, 74dB below 10mV
Channel separation @ 1 kHz, 80dB

μA742

ZERO CROSSING AC TRIGGER-TRIGAC

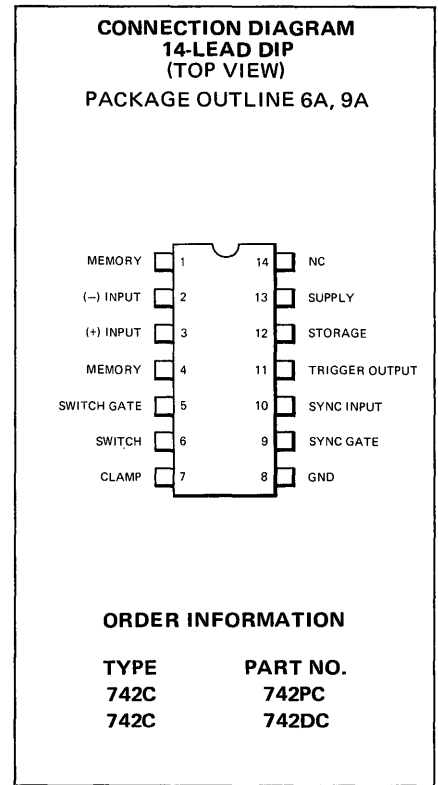
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA742 is a monolithic Zero Crossing AC Trigger (TRIGAC) utilizing the Fairchild Planar* Epitaxial Process. It is intended for use in ac power control circuits for operation directly off the ac line or with a separate ac or dc power supply. The TRIGAC functions as a threshold detector and a driver for triacs and SCR's. As a threshold detector, it senses level changes at the inputs and as a driver it supplies high energy pulses for thyristor triggering. The trigger pulses occur at the zero crossing of the load current and therefore minimize RFI generation for either resistive or inductive loads

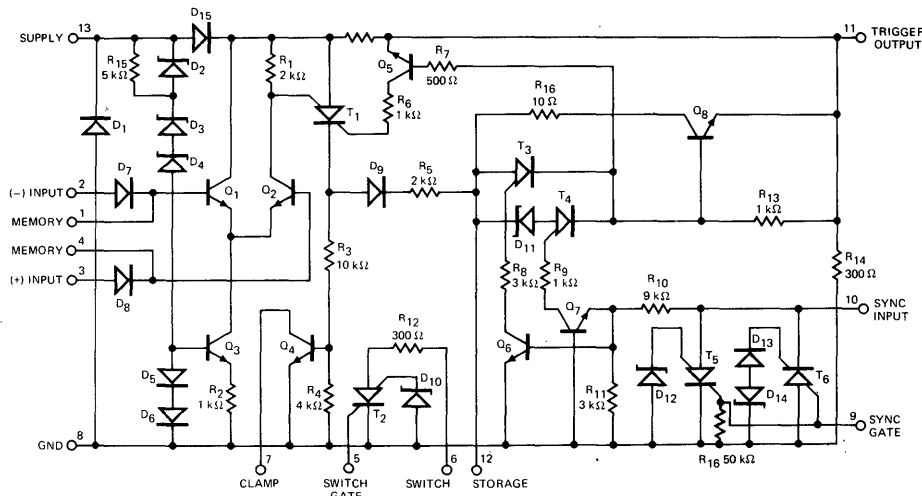
- DESIGNED FOR APPLICATIONS IN 60Hz AND 400Hz AC POWER CONTROL SYSTEMS HAVING RESISTIVE OR INDUCTIVE LOADS
- OPERATES DIRECTLY FROM AN AC LINE OR FROM A DC SUPPLY
- INPUT COMPATIBLE WITH A WIDE RANGE OF SENSOR IMPEDANCES
- BRIDGE SENSING WITH ADJUSTABLE HYSTERESIS SET POINTS
- PROVIDES FOR TIME PROPORTIONING OPERATION
- PROVIDES ZERO CROSSING THYRISTOR TRIGGERING FOR MINIMUM RFI
- EVEN NUMBER OF CONSECUTIVE HALF-CYCLE TRIGGERINGS FOR TRIACS AND INVERSE PARALLEL SCR's IN MOST APPLICATIONS

ABSOLUTE MAXIMUM RATINGS

Peak Current into Supply Terminal (ac Operation)	± 30mA
Continuous Current into Supply Terminal (dc Operation)	20mA
RMS Current into Sync Input Terminal	15mA
Current into Switch Terminal	10mA
Power Dissipation	670mW
Voltage at (+) or (-) Input Terminal	(Note 1)
Differential Voltage between (+) and (-) Input Terminals	± 7V
Current into Clamp Terminal (Clamp ON)	20mA
Voltage at Clamp Terminal (Clamp OFF)	25V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature	
Hermetic DIP (soldering, 60 seconds)	300°C
Molded DIP (soldering, 10 seconds)	260°C
Trigger Output Short-Circuit Duration (Note 2)	Continuous



EQUIVALENT CIRCUIT



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A742

742C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Voltage Range at the (+) and (-) Input Terminals: 2.5V to 17V;
 $V(+)$ Input - $V(-)$ Input $\geq 50\text{mV}$, Test Circuit 1, unless otherwise specified.)

PARAMETER	CONDITION	MIN	TYP.	MAX.	UNITS
Peak Supply Voltage	S ₁ in dc position	19	21	26	V
	S ₁ in ac position, positive half cycles of ac line	19	21	26	V
	S ₁ in ac position, negative half cycle of ac line	-1.6	-0.95	-0.8	V
Peak Trigger Output Pulse	S ₁ in ac position, beginning of positive half cycles	0.6	0.9		A
	S ₁ in ac or dc position, beginning of negative half cycles	1.0	1.3		A
	S ₁ in dc position beginning of positive half cycles	1.6	2.0		A
Bias Current at (+) and (-) Terminals			15	25	μA
Input Threshold Voltage for Output Pulse Enable		-50	-35	50	mV
ON Voltage at Clamp Terminal	I ₇ = 1 mA		85	200	mV
ON Voltage at Switch Terminal	I ₆ = 5 mA		2.6	3.0	V
Switching Voltage at Switch Terminal		6.0	7.2		V
Switching Current at Switch Terminal			15		μA
Holding Current at Switch Terminal			23	200	μA
ON Voltage at Sync Input Terminal	I ₁₀ = 10 mA		1.9	2.2	V
	I ₁₀ = -10 mA	-2.2	-1.9		V
Switching Voltage at Sync Input Terminal	I ₁₀ = 2 mA, positive half cycles, $V(-)$ Input - $V(+)$ Input > 50 mV	4.5	5.8		V
	I ₁₀ = -2 mA, negative half cycles, $V(-)$ Input - $V(+)$ Input > 50 mV		-7.0	-4.5	V
Sync Input Threshold Current for Trigger Output	Beginning of positive half cycles	180	410	500	μA
	Beginning of negative half cycles	-500	-280	-180	μA
Sync Input Threshold Voltage for Trigger Output	Beginning of positive half cycles	2.0	2.7	4.0	V
	Beginning of negative half cycles	-4.0	-3.3	-2.0	V

DEFINITIONS

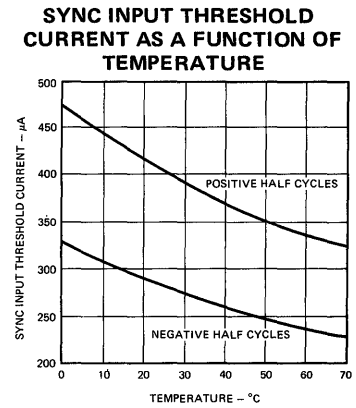
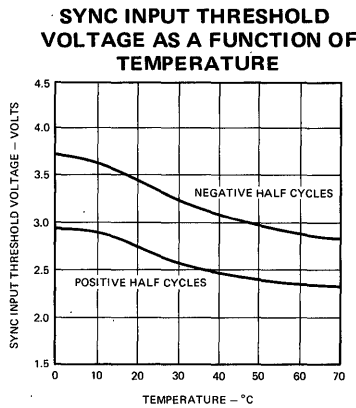
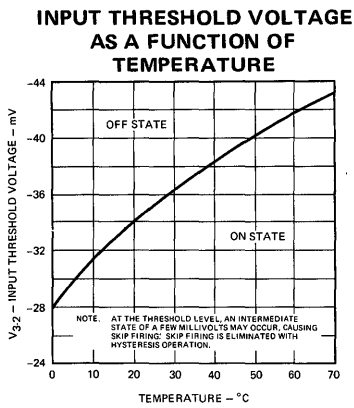
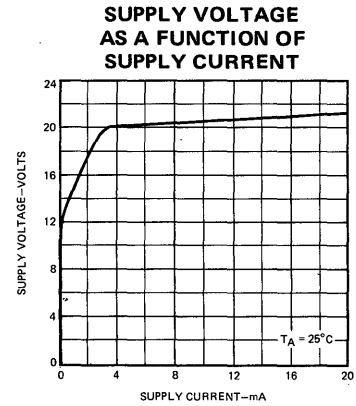
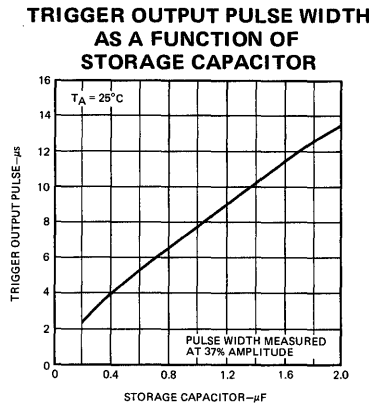
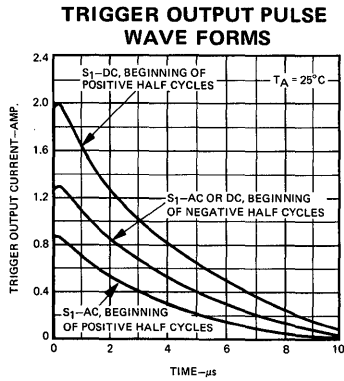
VOLTAGE RANGE: The range of voltage on the (+) or (-) input terminals, which, if exceeded, could cause the TRIGAC to cease functioning.

BIAS CURRENT: The average of the two currents into the (+) and (-) input terminals.

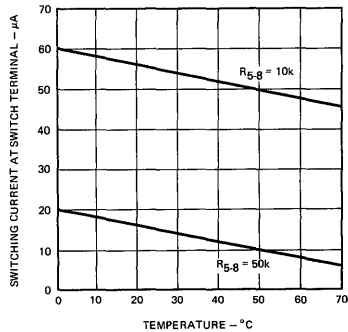
NOTES:

- (1) The maximum voltage should not exceed the instantaneous supply voltage of the $\mu\text{A}742$.
- (2) Rating applies for an external storage capacitor having a value of not more than $2\mu\text{F}$.

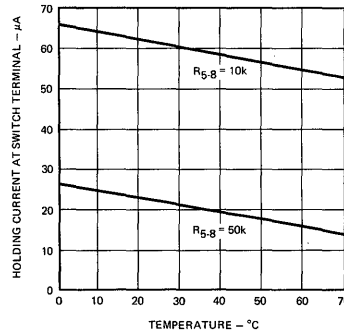
TYPICAL PERFORMANCE CURVES FOR 742C
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)



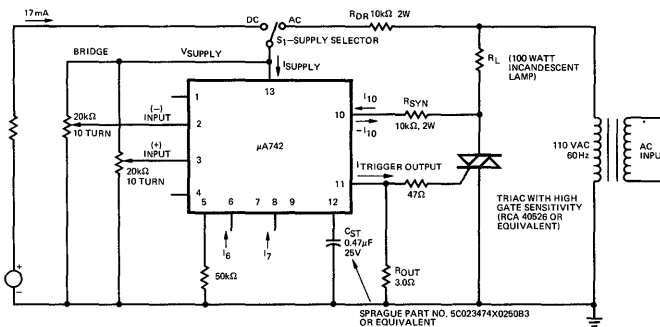
SWITCHING CURRENT AT SWITCH TERMINAL AS A FUNCTION OF TEMPERATURE



HOLDING CURRENT AT SWITCH TERMINAL AS A FUNCTION OF TEMPERATURE

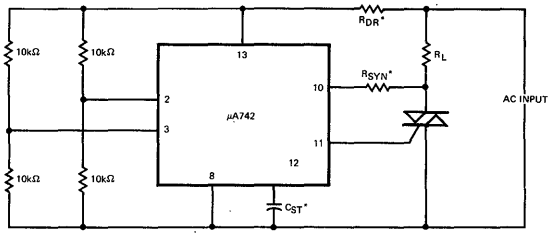


TEST CIRCUIT 1



TYPICAL APPLICATIONS FOR 742C

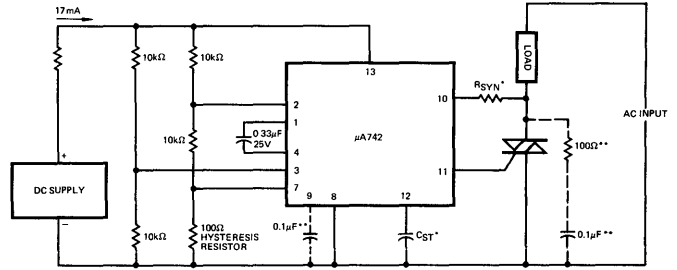
ZERO CROSSING CONTROL CIRCUIT WITHOUT HYSTERESIS



SENSOR BRIDGE***

Fig. 1

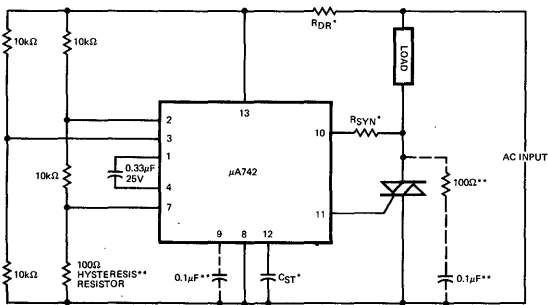
ZERO CROSSING CIRCUIT WITH DC SUPPLY



SENSOR BRIDGE***

Fig. 2

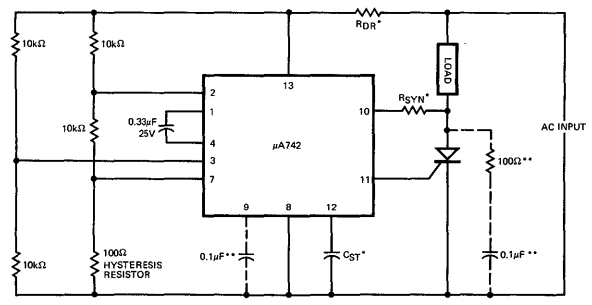
ZERO CROSSING CIRCUIT



SENSOR BRIDGE***

Fig. 3

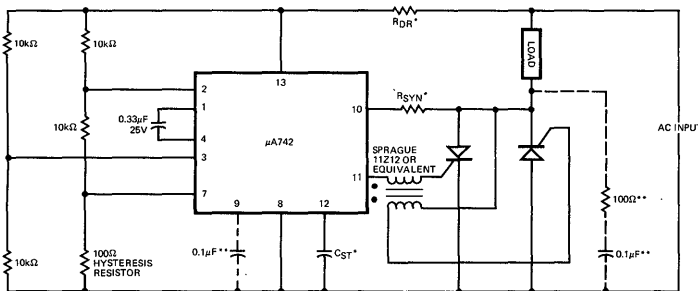
SCR FIRING—HALF WAVE



SENSOR BRIDGE***

Fig. 4

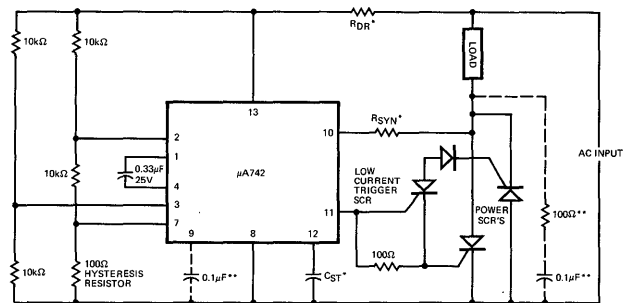
INVERSE PARALLEL SCR PAIR FIRING WITH A PULSE TRANSFORMER



SENSOR BRIDGE***

Fig. 5

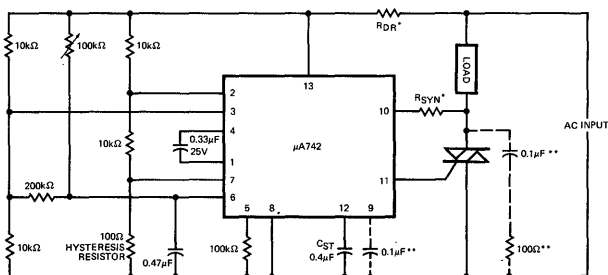
INVERSE PARALLEL SCR PAIR FIRING WITH A THIRD SCR



SENSOR BRIDGE***

Fig. 6

ZERO CROSSING WITH PROPORTIONAL CONTROL



SENSOR BRIDGE***

Fig. 7

*Recommended Values

AC Supply Voltage 60Hz Volts - RMS	R_{DR}	R_{SYN}	C_{ST}
24	1.2 kΩ	2.2 kΩ	0.47 μF/25V
110	10 kΩ	10 kΩ	0.47 μF/25V
220	22 kΩ	22 kΩ	0.47 μF/25V

FOR SUPPLY VOLTAGE FREQUENCY OF 400Hz REDUCE C_{ST} TO .047 μF/25V

** Necessary with inductive loads.

***The sensor resistance will determine the values of the bridge resistors. For the values of R_{DR} shown, the total current into the bridge should not exceed 5 mA at 20V.

μA746

CHROMA DEMODULATOR

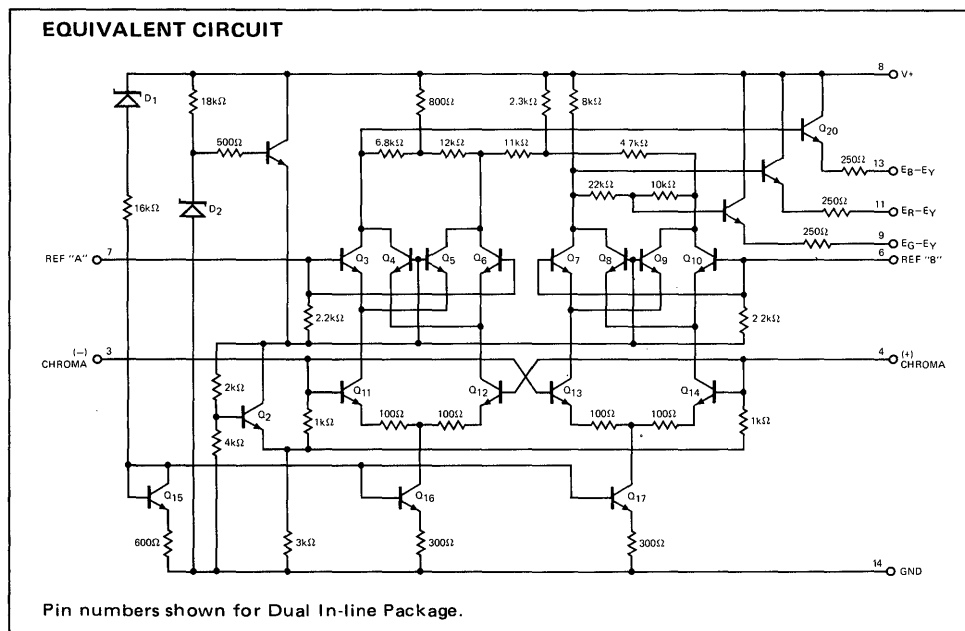
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA746 is a monolithic Chroma Demodulator constructed using the Fairchild Planar* epitaxial process. This device demodulates the chroma subcarrier information contained in a color television video signal and provides color-difference signals at the outputs. The low voltage drift of the dc output insures excellent performance in direct-coupled chrominance output circuitry.

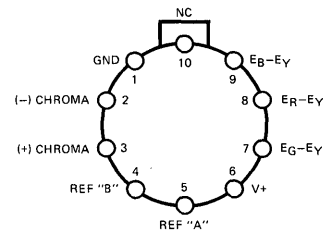
- **LOW OUTPUT VOLTAGE DRIFT WITH TEMPERATURE**
- **DOUBLY BALANCED DEMODULATION**
- **INTERNAL COLOR-DIFFERENCE MATRIX FOR NTSC COLOR TV**
- **10 VOLT PEAK-TO-PEAK E_B-E_Y OUTPUT**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+28V
Minimum Load Resistance	3 kΩ
Peak-to-Peak Reference Input Voltage	5.0V
Peak-to-Peak Chroma Input Voltage	5.0V
Internal Power Dissipation	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	
Molded DIP	-55°C to +125°C
Metal Can and Hermetic DIP	-65°C to +150°C
Lead Temperature	
Metal Can and Hermetic DIP (soldering, 60 seconds)	300°C
Molded DIP (soldering, 10 seconds)	260°C



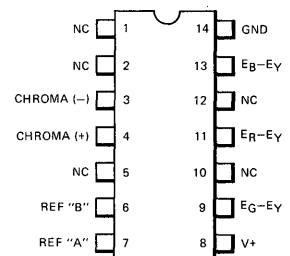
CONNECTION DIAGRAMS
10-LEAD METAL CAN
 (TOP VIEW)
 PACKAGE OUTLINE 5E



ORDER INFORMATION

TYPE	PART NO.
746C	746HC

14-LEAD DIP
 (TOP VIEW)
 PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
746C	746DC
746C	746PC

*Planar is a patented Fairchild Process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A746

746C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_+ = 24\text{V}$, Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_C = 0, R_L = 1\text{M}\Omega$	5.5	9.0	12.5	mA
	$e_C = 0, R_L = 1\text{M}\Omega, T_A = 70^\circ\text{C}$		9.0	13.0	mA
	$e_C = 0$	16.5	22	25.5	mA
	$e_C = 0, T_A = 70^\circ\text{C}$		22		mA
Internal Power Dissipation	$e_C = 0$		340	430	mW
	$e_C = 0, T_A = 70^\circ\text{C}$		340	445	mW
DC Voltage at any Output Terminal	$e_C = 0$	13.2	14.5	15.8	V
	$e_C = 0, T_A = 70^\circ\text{C}$	13.0	14.5	16.0	V
Temperature Coefficient of DC Voltage at any Output Terminal	$e_C = 0$	-5.0	-0.3	+5.0	mV/ $^\circ\text{C}$
Absolute Value of DC Difference Voltage between any Two Outputs	$e_C = 0$		0.15	0.6	V
DC Voltage at either Reference Terminal	$e_A = e_B = e_C = 0$		5.8		V
DC Voltage at either Chroma Terminal	$e_C = 0$		3.2		V
Reference Input Resistance	$e_C = 0$		1.7		k Ω
Reference Input Capacitance	$e_C = 0$		6.0		pF
Chroma Input Resistance			0.8		k Ω
Chroma Input Capacitance			5.0		pF
Peak-to-Peak Chroma Input Voltage	$E_B - E_Y = 5\text{Vp-p}$		0.4	0.7	V
Peak-to-Peak $E_R - E_Y$ Output Voltage	$E_B - E_Y = 5\text{Vp-p}$	3.5	3.8	4.2	V
Peak-to-Peak $E_G - E_Y$ Output Voltage	$E_B - E_Y = 5\text{Vp-p}$	0.75	1.0	1.25	V
Maximum Peak-to-Peak $E_B - E_Y$ Output Voltage	$e_C = 1.5\text{Vp-p}$	8.0	10		V
$E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5\text{Vp-p}$		3		Degrees
$E_R - E_Y$ Demodulation Angle	$E_B - E_Y = 5\text{Vp-p}$		109		Degrees
$E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5\text{Vp-p}$		259		Degrees
$E_R - E_Y$ Demodulation Angle relative to $E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5\text{Vp-p}$	101	106	111	Degrees
$E_B - E_Y$ Demodulation Angle relative to $E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5\text{Vp-p}$	96	104	112	Degrees
Highest AC Unbalance Voltage at any Output Terminal	$e_C = 0$		0.3	0.8	V _{p-p}

DEFINITIONS

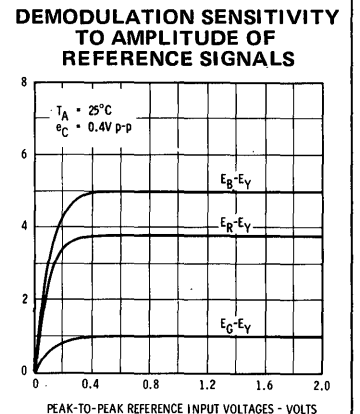
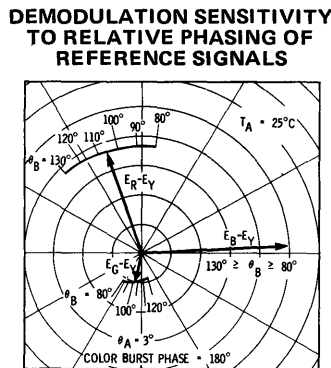
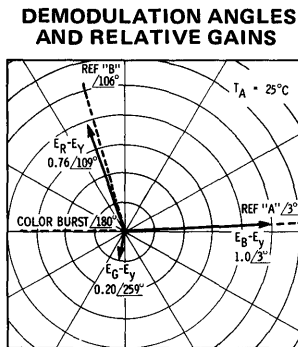
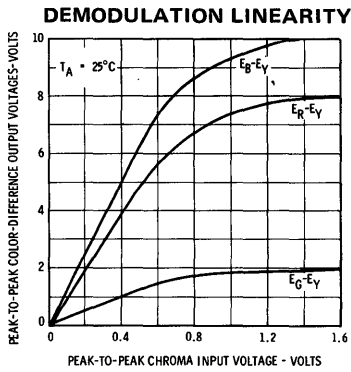
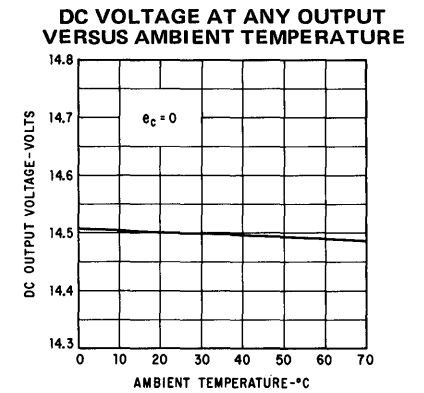
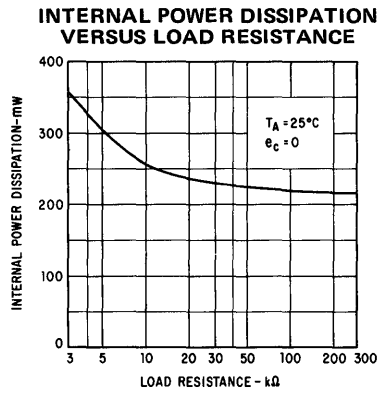
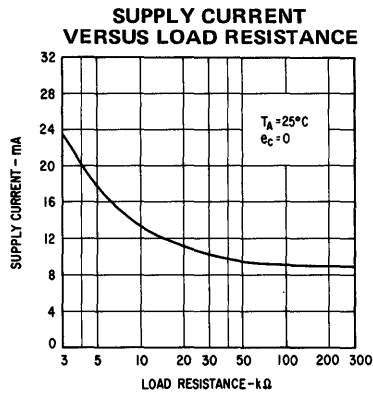
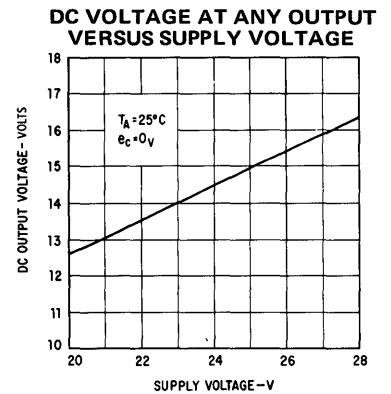
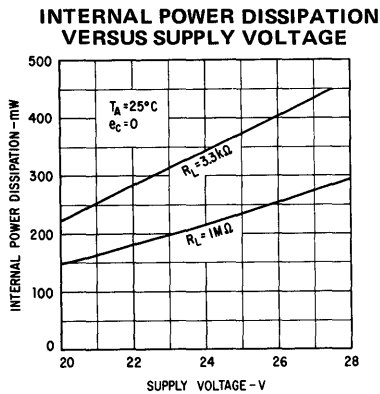
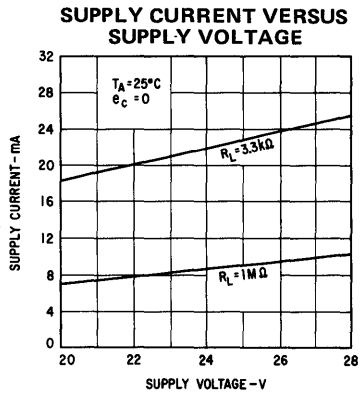
Color-Difference Demodulation Angle – A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

(+) Chroma Input – A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(-) Chroma Input – A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (-) Chroma input.

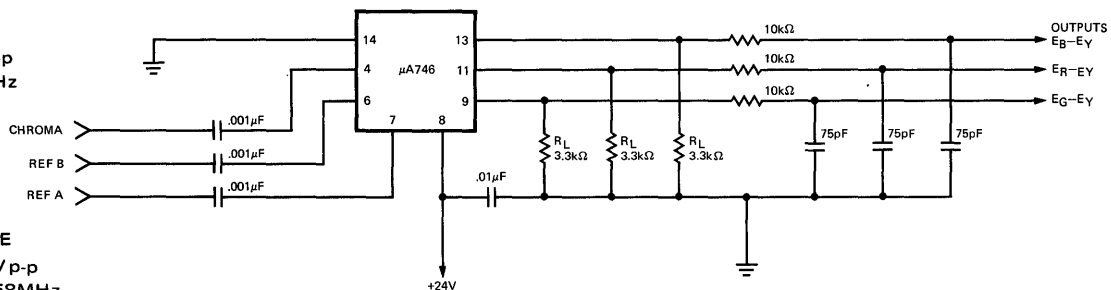
7

TYPICAL PERFORMANCE CURVES FOR 746C
(Test Circuit 1 Unless Otherwise Specified)



TEST CIRCUIT 1

INPUTS
CHROMA:
 $e_C \leq 1.5V$ p-p
 $f_C = 3.59MHz$

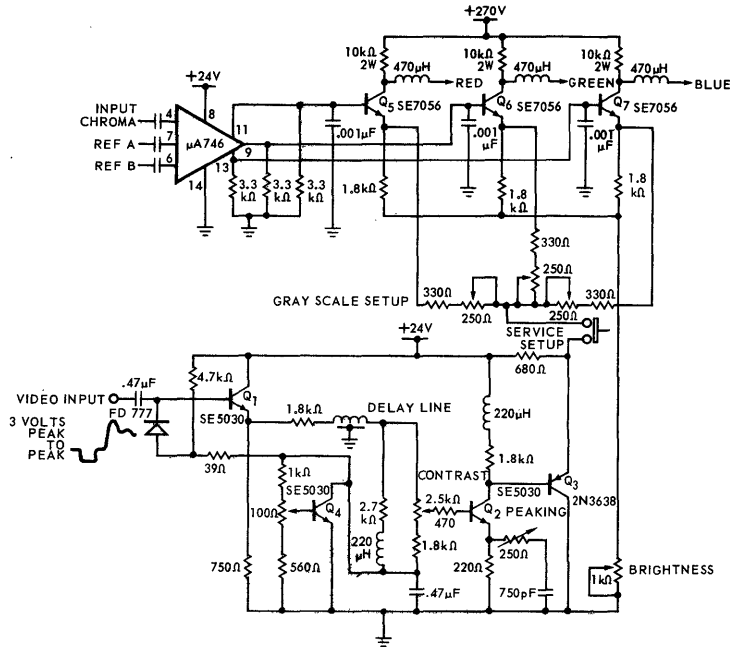


REFERENCE
 $e_A = e_B = 1V$ p-p
 $f_A = f_B = 3.58MHz$
 $\theta_B = \theta_A + 103^\circ$

Pin numbers shown for Dual In-line Package only.

TYPICAL APPLICATION

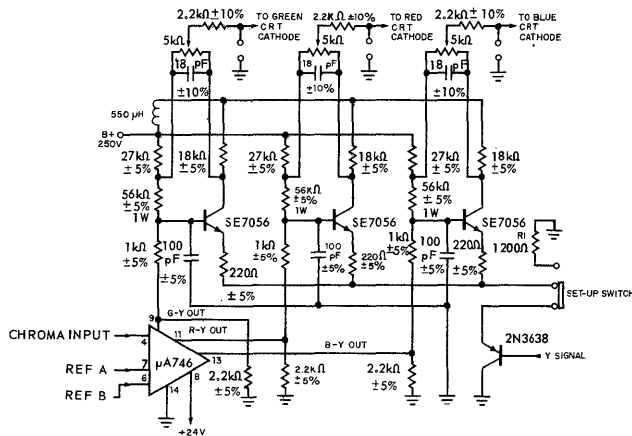
COMPLETE R-G-B VIDEO OUTPUT STAGE



Pin numbers shown for Dual In-line Package only.

Fully dc coupled circuit exhibits negligible drift with temperature, eliminates interaction between contrast and brightness controls, and minimizes gray-scale set-up time.

ALTERNATIVE R-G-B VIDEO OUTPUT STAGE



Pin numbers shown for Dual In-line Package only.

From:
 "A Semiconductor Video Output Amplifier for a Red Blue Green Large Screen Color Television Receiver", by D. Poppy. IEEE Transactions on Broadcast and Television Receivers, BTR-15, #2, pp. 167-70, July 1969.

Reprinted with permission.

μA749

DUAL AUDIO PREAMPLIFIER

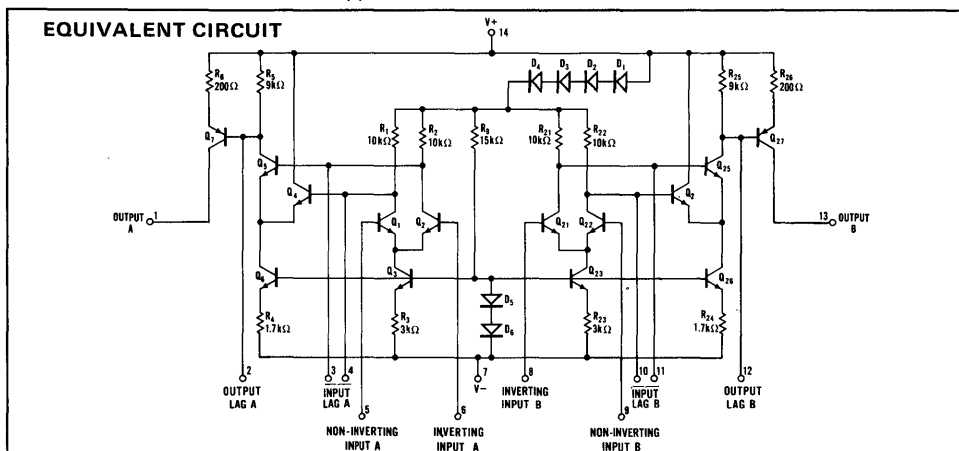
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA749 consists of Two Identical High Gain Operational Amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These three-stage amplifiers use Class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from dc to 10 MHz, where two high performance operational amplifiers are required. In addition, the outputs may be wired-OR for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers, peak detectors, etc.

- SINGLE OR DUAL SUPPLY OPERATION
- LOW POWER CONSUMPTION
- HIGH GAIN, 25,000 V/V
- LARGE COMMON MODE RANGE, +11 V, -13 V
- EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE
- NO LATCH-UP
- OUTPUT SHORT CIRCUIT PROTECTED

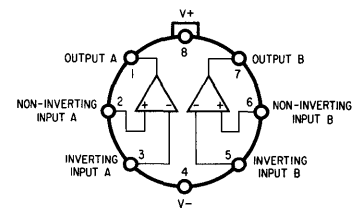
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (749 and 749C)	±18 V
(749D)	±12 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	650 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2) (749 and 749C)	±15 V
(749D)	±12 V
Storage Temperature Range	
Metal Can, Hermetic DIP	-65°C to +150°C
Molded DIP (749PC)	-55°C to +125°C
Operating Temperature Range	
Military (749)	-55°C to +125°C
Commercial (749C and 749D)	0°C to + 70°C
Lead Temperature	
Metal Can, Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C
Output Short-Circuit Duration, T _A = 25°C (Note 3)	30 seconds



Notes on following pages.

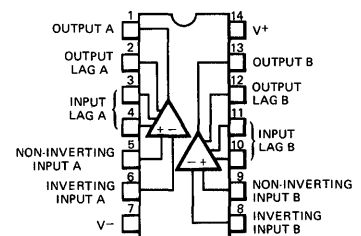
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B



Note: Pin 4 connected to case.

ORDER INFORMATION	
TYPE	PART NO.
749D	749DHC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION	
TYPE	PART NO.
749	749DM
749C	749DC
749C	749PC

*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A749

749

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $R_L = 5$ k Ω to Pin 7, $T_A = 25^\circ$ C unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S = 200 \Omega$		1.0	3.0	mV
Input Offset Current			50	400	nA
Input Bias Current			0.30	0.75	μ A
Input Resistance		100	150		k Ω
Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V	20,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-14	-15		V
Output Resistance	$f = 1.0$ kHz		5.0		k Ω
Common Mode Rejection Ratio	$R_S = 200 \Omega$, $V_{IN} = +11.5$ V to -13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	$R_S = 200 \Omega$		50	200	μ V/V
Negative Supply Voltage Rejection Ratio	$R_S = 200 \Omega$		50	200	μ V/V
Input Voltage Range		-13		+11	V
Internal Power Dissipation	$V_{OUT} = 0$		180	220	mW
Supply Current	$V_{OUT} = 0$		9.0	10.4	mA
Broadband Noise Figure	$R_S = 10$ k Ω , BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μ s
Turn Off Delay (See Fig. 3)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μ s
Slew Rate (unity gain) (See Fig. 2)	$C_1 = 0.02 \mu$ F, $R_1 = 33 \Omega$, $C_2 = 10$ pF		2.0		V/ μ s
Channel Separation (See Fig. 4)	$R_S = 1$ k Ω $f = 10$ kHz		140		dB

The following specifications apply for $V_S = \pm 4.0$ V, $R_L = 10$ k Ω to Pin 7, $T_A = 25^\circ$ C

Input Offset Voltage	$R_S = 200 \Omega$		1.0	3.0	mV
Input Offset Current			50	300	nA
Input Bias Current			0.15	0.75	μ A
Supply Current	$V_{OUT} = 0$		2.5	4.8	mA
Internal Power Dissipation	$V_{OUT} = 0$		20	36	mW
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V	20,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		-3.6	-4.0		V

The following specifications apply for -55° C $\leq T_A \leq +125^\circ$ C, $V_S = \pm 15$ V, $R_L = 5$ k Ω to Pin 7:

Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V, $T_A = +125^\circ$ C	6,500	20,000		V/V
	$V_{OUT} = \pm 10$ V, $T_A = -55^\circ$ C	20,000	30,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-14	-15		V
Input Offset Voltage	$R_S = 200 \Omega$		1.0	6.0	mV
	$T_A = +125^\circ$ C		0.05	1.0	μ A
Input Offset Current	$T_A = -55^\circ$ C		0.05	1.5	μ A
	$T_A = +125^\circ$ C		0.15	0.75	μ A
Input Bias Current	$T_A = -55^\circ$ C		0.3	3.0	μ A
	$R_S = 200 \Omega$, $+25^\circ$ C $\leq T_A \leq +125^\circ$ C		3.0		μ V/ $^\circ$ C
Input Offset Voltage Drift	$R_S = 200 \Omega$, -55° C $\leq T_A \leq +25^\circ$ C		3.0		μ V/ $^\circ$ C
	$+25^\circ$ C $\leq T_A \leq +125^\circ$ C		0.5		nA/ $^\circ$ C
Input Offset Current Drift	-55° C $\leq T_A \leq +25^\circ$ C		2.0		nA/ $^\circ$ C
	-55° C $\leq T_A \leq +125^\circ$ C		5.0		nA/ $^\circ$ C
Supply Current	$V_{OUT} = 0$, $T_A = +125^\circ$ C			9.7	mA
	$V_{OUT} = 0$, $T_A = -55^\circ$ C			13	mA
Internal Power Dissipation	$V_{OUT} = 0$, $T_A = +125^\circ$ C			200	mW
	$V_{OUT} = 0$, $T_A = -55^\circ$ C			300	mW

The following specifications apply for -55° C $\leq T_A \leq +125^\circ$ C, $V_S = \pm 4$ V, $R_L = 10$ k Ω to Pin 7:

Input Offset Voltage	$R_S = 200 \Omega$		1.5	6.0	mV
Input Offset Current			50	750	nA
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V, $T_A = +125^\circ$ C	5,000			V/V
	$V_{OUT} = \pm 2.0$ V, $T_A = -55^\circ$ C	20,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		-3.6	-4.0		V

NOTES:

1. Rating applies to ambient temperatures up to 70° C. Above 70° C ambient derate linearly at 8.3 mW/ $^\circ$ C for the DIP package.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A749

749C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $R_L = 5$ k Ω to Pin 7, $T_A = 25^\circ$ C unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S = 200 \Omega$		1.0	6.0	mV
Input Offset Current			50	750	nA
Input Bias Current			0.30	1.5	μ A
Input Resistance		50	150		k Ω
Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-14	-15		V
Output Resistance	$f = 1.0$ kHz		5.0		k Ω
Common Mode Rejection Ratio	$R_S = 200 \Omega$, $V_{IN} = +11.5$ V to -13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	$R_S = 200 \Omega$		50	350	μ V/V
Negative Supply Voltage Rejection Ratio	$R_S = 200 \Omega$		50	200	μ V/V
Input Voltage Range		-13		+11	V
Internal Power Dissipation	$V_{OUT} = 0$		180	330	mW
Supply Current	$V_{OUT} = 0$		9.0	14	mA
Broadband Noise Figure	$R_S = 10$ k Ω , BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μ s
Turn Off Delay (See Fig. 3)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μ s
Slew Rate (unity gain) (See Fig. 2)	$C_1 = 0.02 \mu$ F, $R_1 = 33 \Omega$, $C_2 = 10$ pF		2.0		V/ μ s
Channel Separation (See Fig. 4)	$R_S = 1$ k Ω , $f = 10$ kHz		140		dB

The following specifications apply for $V_S = \pm 4.0$ V, $R_L = 10$ k Ω to Pin 7, $T_A = 25^\circ$ C:

Input Offset Voltage	$R_S = 200 \Omega$		1.0	6.0	mV
Input Offset Current			50	600	nA
Input Bias Current			0.3	1.5	μ A
Supply Current	$V_{OUT} = 0$		2.5		mA
Internal Power Dissipation	$V_{OUT} = 0$		20		mW
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V	15,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		-3.6	-4.0		V

The following specifications apply for 0° C $\leq T_A \leq +70^\circ$ C, $V_S = \pm 15$ V, $R_L = 5$ k Ω to Pin 7:

Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V, $T_A = +70^\circ$ C	8,000	40,000		V/V
	$V_{OUT} = \pm 10$ V, $T_A = 0^\circ$ C	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-14	-15		V
Input Offset Voltage	$R_S = 200 \Omega$		1.0	9.0	mV
Input Offset Current			0.05	1.5	μ A
Input Bias Current			0.3	3.0	μ A
Input Offset Voltage Drift	$R_S = 200 \Omega$, $+25^\circ$ C $\leq T_A \leq +70^\circ$ C		3.0		μ V/ $^\circ$ C
	$R_S = 200 \Omega$, 0° C $\leq T_A \leq +25^\circ$ C		3.0		μ V/ $^\circ$ C
Input Offset Current Drift	$+25^\circ$ C $\leq T_A \leq +70^\circ$ C		0.5		nA/ $^\circ$ C
	0° C $\leq T_A \leq +25^\circ$ C		2.0		nA/ $^\circ$ C
Input Bias Current Drift	0° C $\leq T_A \leq +70^\circ$ C		4.0		nA/ $^\circ$ C

The following specifications apply for 0° C $\leq T_A \leq +70^\circ$ C, $V_S = \pm 4$ V, $R_L = 10$ k Ω to Pin 7:

Input Offset Voltage	$R_S = 200 \Omega$		1.5	9.0	mV
Input Offset Current			0.05	1.0	μ A
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V, $T_A = 70^\circ$ C	8,000			V/V
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V, $T_A = 0^\circ$ C	15,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		-3.6	-4.0		V

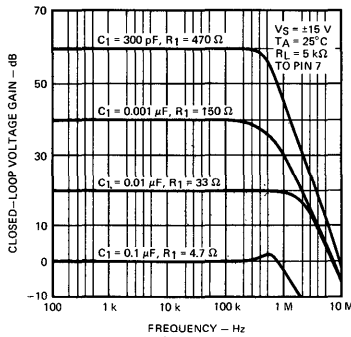
749D

ELECTRICAL CHARACTERISTICS ($V_S = \pm 6$ V, $R_L = 10$ k Ω to pin 4. $T_A = 25^\circ$ C unless otherwise specified)

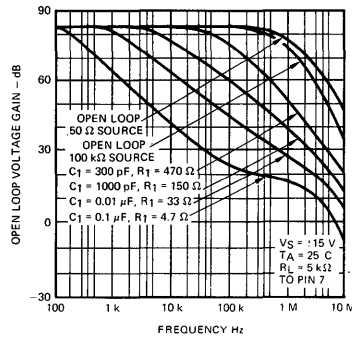
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200 \Omega$		1.0	10	mV
Input Offset Current			50	600	nA
Input Bias Current			300	1500	nA
Input Resistance		50	150		k Ω
Large Signal Voltage Gain	$V_{OUT} = \pm 4.0$ V	10,000	20,000		V/V
Positive Output Voltage Swing		+4.5	+5.0		V
Negative Output Voltage Swing		-5.5	-6.0		V
Output Resistance	$f = 1.0$ kHz		10		k Ω
Input Voltage Range		-4.0		+2.5	V
Common Mode Rejection Ratio	$R_S \leq 10$ k Ω	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ k Ω		50	100	μ V/V
Power Consumption (including load)	$V_{OUT} = 0$	24	36	54	mW
Supply Current (including load)	$V_{OUT} = 0$	2.0	3.0	4.5	mA
Turn On Delay (See Figure 5)	Open Loop, $V_{IN} = \pm 20$ mV, $R_L = 5$ k Ω		0.2		μ s
Turn Off Delay (See Figure 5)	Open Loop, $V_{IN} = \pm 20$ mV, $R_L = 5$ k Ω		0.3		μ s
Channel Separation (See Figure 7)	$R_S \leq 10$ k Ω , $f = 10$ kHz		140		dB

TYPICAL PERFORMANCE CURVES FOR 749 AND 749C

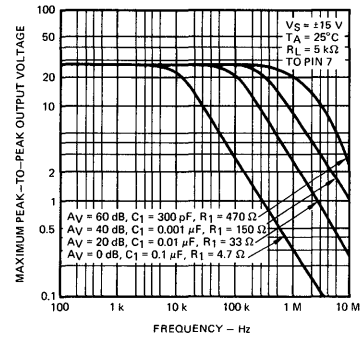
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



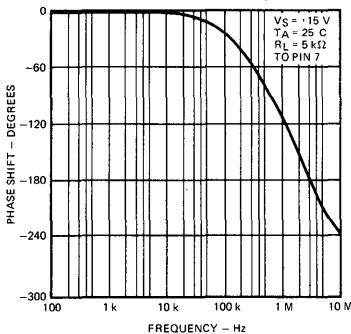
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



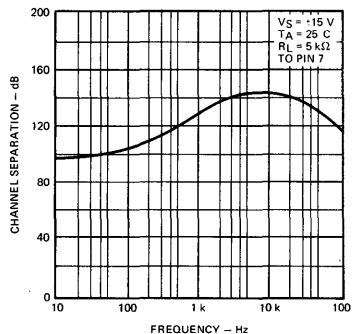
OUTPUT CAPABILITY AS A FUNCTION OF FREQUENCY AND COMPENSATION



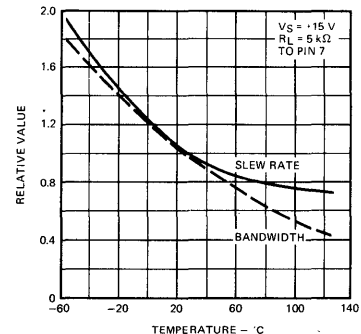
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

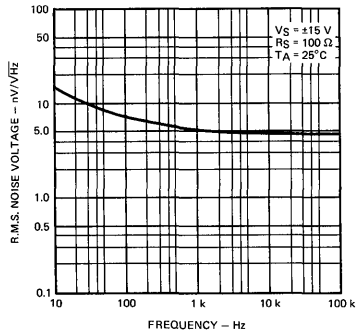


CHANGE OF AC CHARACTERISTICS WITH TEMPERATURE

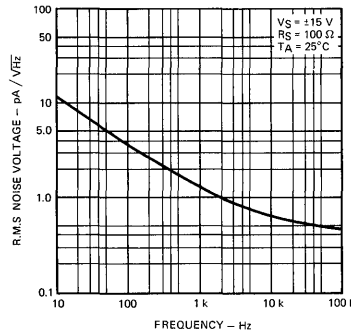


TYPICAL PERFORMANCE CURVES FOR 749 AND 749C

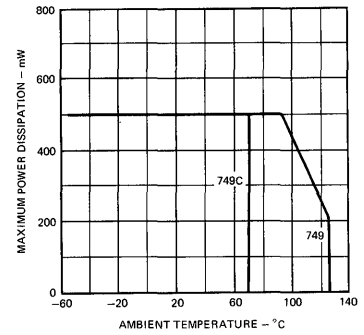
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



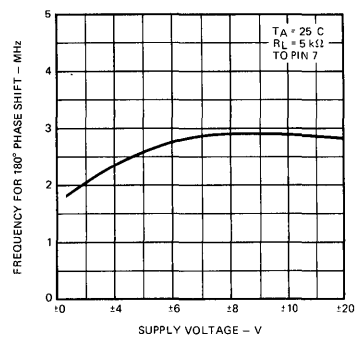
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



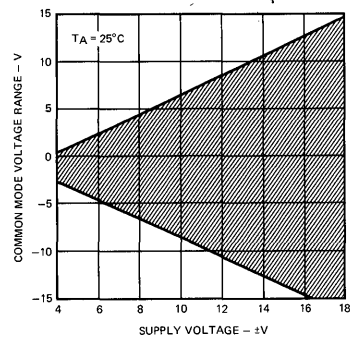
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



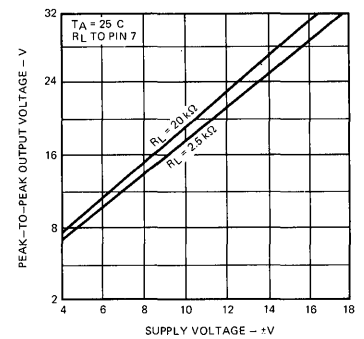
OPEN LOOP 180° PHASE SHIFT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



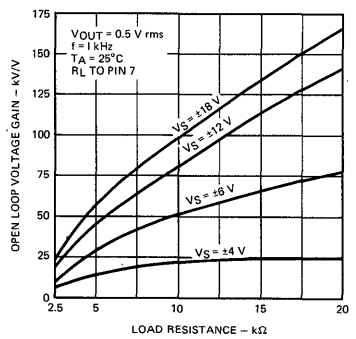
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



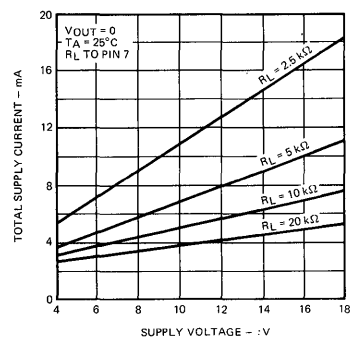
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



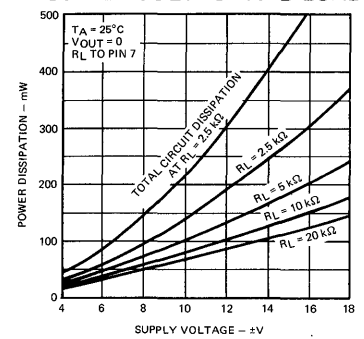
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



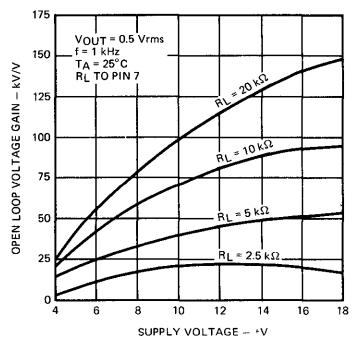
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



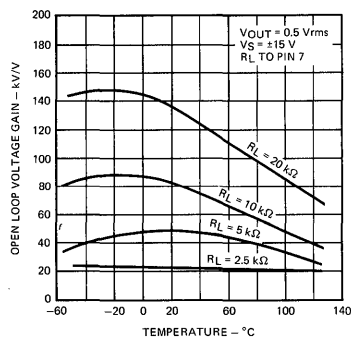
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



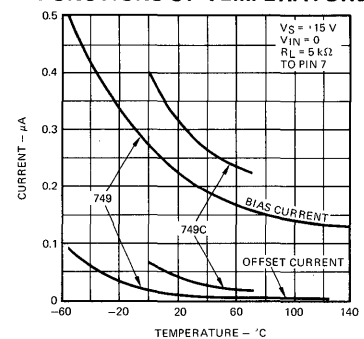
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

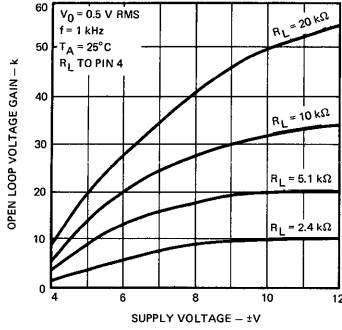


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

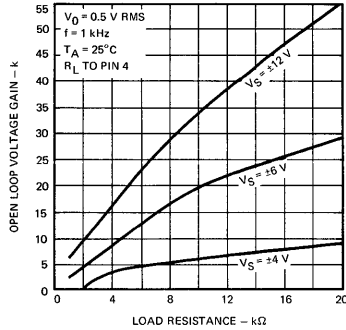


TYPICAL PERFORMANCE CURVES FOR 749D

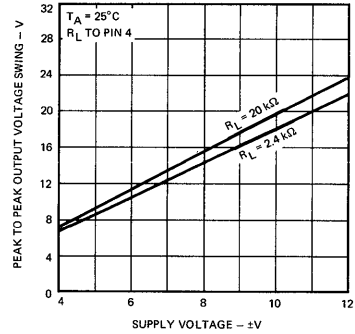
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



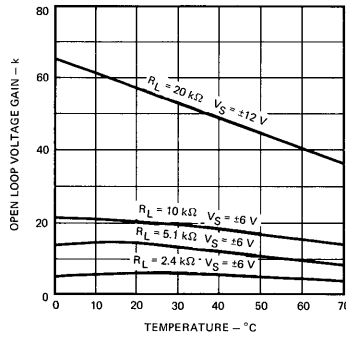
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



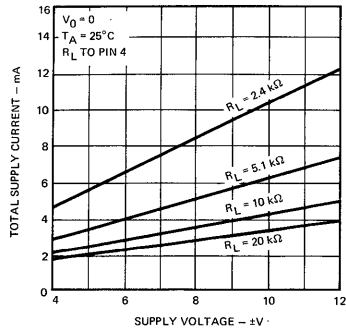
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



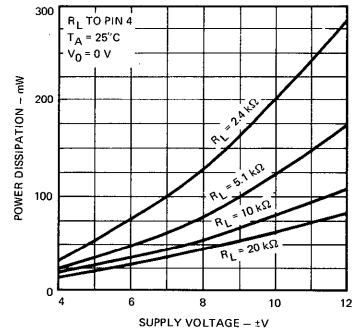
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



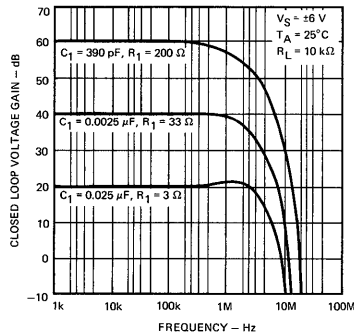
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



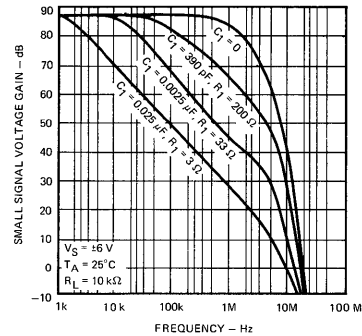
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



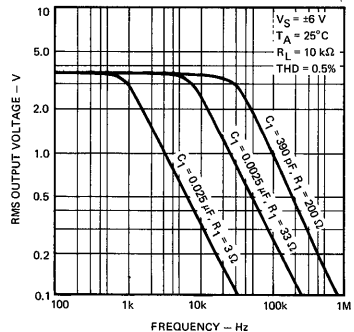
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



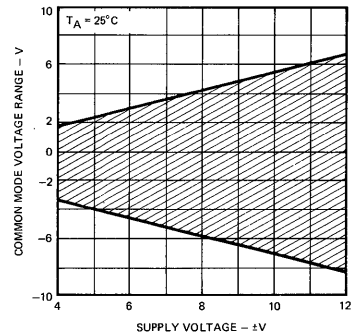
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



**OFFSET NULL *
NETWORK
749 AND 749C**

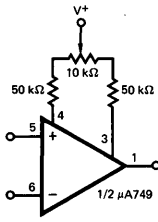


Fig. 1

**FREQUENCY RESPONSE *
TEST CIRCUIT
749 AND 749C**

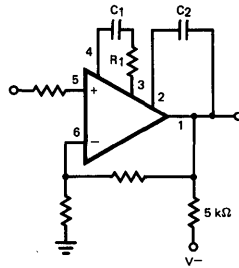


Fig. 2

**PULSE RESPONSE
WAVEFORMS
749 AND 749C**

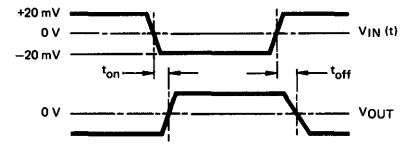


Fig. 3

**CHANNEL SEPARATION *
TEST CIRCUIT
749 AND 749C**

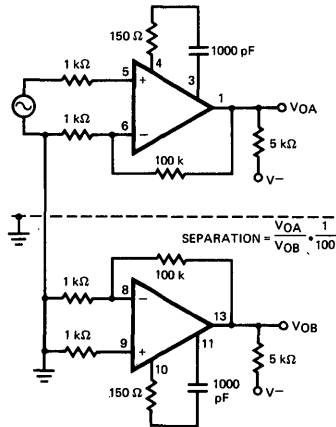


Fig. 4

**PULSE RESPONSE
WAVEFORMS
749D**

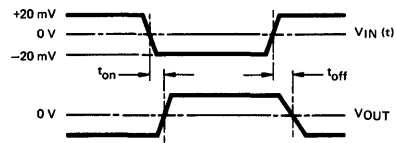


Fig. 5

**FREQUENCY RESPONSE
TEST CIRCUIT
749D**

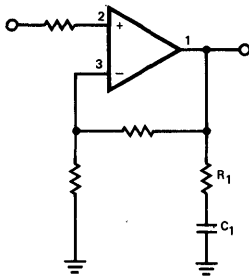


Fig. 6

**CHANNEL SEPARATION
TEST CIRCUIT
749D**

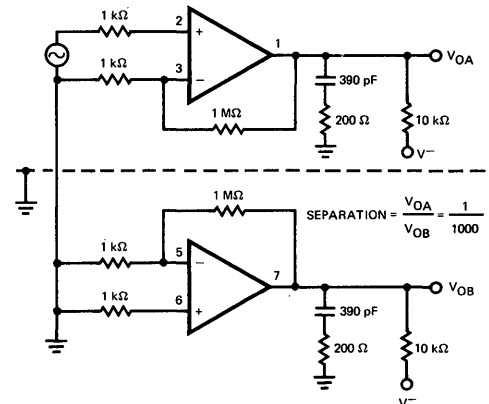
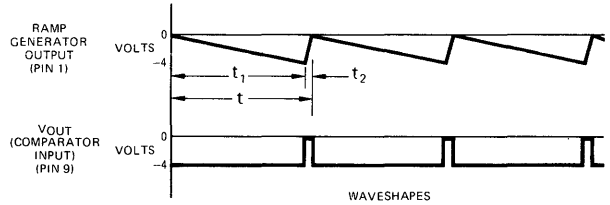
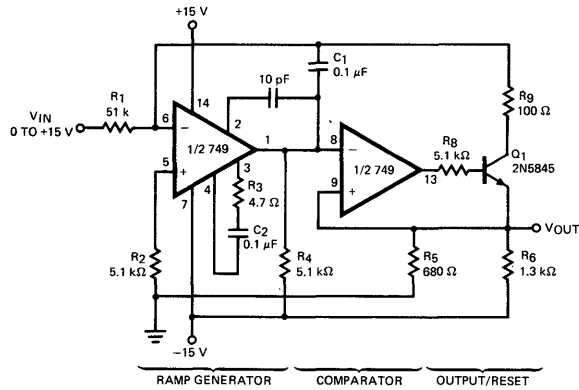


Fig. 7

*Pin numbers refer to Dual-in-line Package

TYPICAL APPLICATIONS

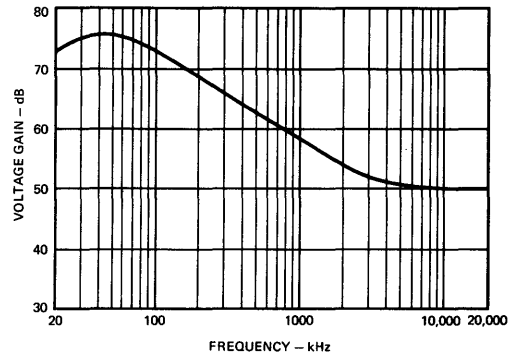
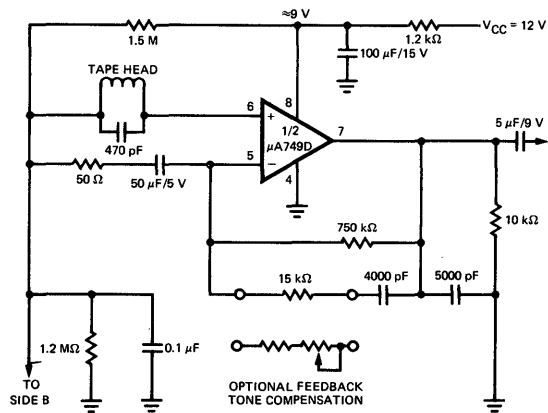
VOLTAGE TO FREQUENCY CONVERTER



$$t = t_1 + t_2 = 4 \frac{R_1 C_1}{V_{IN}} + \frac{4 R^* C_1}{15}$$

$R^* = R_{pin 1} + R_9 + R_{CE Q1} + R_6$ output stage.

STEREO TAPE PREAMPLIFIER



TYPICAL PERFORMANCE

Gain at 1 kHz	60 dB
Output Voltage Swing	2.8 V rms
Power Consumption	30 mW

μA753

FM GAIN BLOCK

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA753 is a high performance monolithic FM Gain Block using the Fairchild Planar* epitaxial process. The FM gain block consists of a three stage direct coupled amplifier with 330Ω input and output terminations and the 7 pF shunting capacitance required for a 10.7 MHz FM IF strip utilizing commercially available ceramic filters. Included on the chip is a 7.8 V active regulator providing up to 10 mA of current to an external load such as an FM tuner.

The μA753 features full temperature compensation for the IF amplifier and the 7.8 V regulator. Excellent power supply rejection eliminates the need for an external regulated supply. An output from the second stage of the IF amplifier provides a means of external gain control without affecting the input or output terminations. The device is packaged in an 8-lead mini DIP.

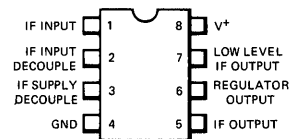
- 50 dB VOLTAGE GAIN AT 10.7 MHz
- 330Ω INPUT AND OUTPUT TERMINATIONS
- OPTIMIZED GAIN VS TEMPERATURE CHARACTERISTICS
- TEMPERATURE COMPENSATED 7.8 V ACTIVE REGULATOR PROVIDING UP TO 10 mA OF CURRENT
- SHORT CIRCUIT PROTECTION FOR ALL EXTERNAL CONNECTIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage at any terminal must not exceed V ⁺	18 V
Supply Voltage (V ⁺)	±3 V
Power Dissipation (P _D) (Note 1)	10 mW
Input Voltage (Pins 1 and 3)	Indefinite
Regulator Output Current (I _{REG})	-40°C to +85°C
Regulator Short Circuit Duration	-55°C to +125°C
Operating Temperature Range (T _A)	
Storage Temperature Range (T _{STG})	
Lead Temperature	
(Soldering, 10 seconds)	260°C

Notes: 1. Rating applies for ambient temperatures to 70°C. Above 70°C derate linearly at 6.3 mW/°C

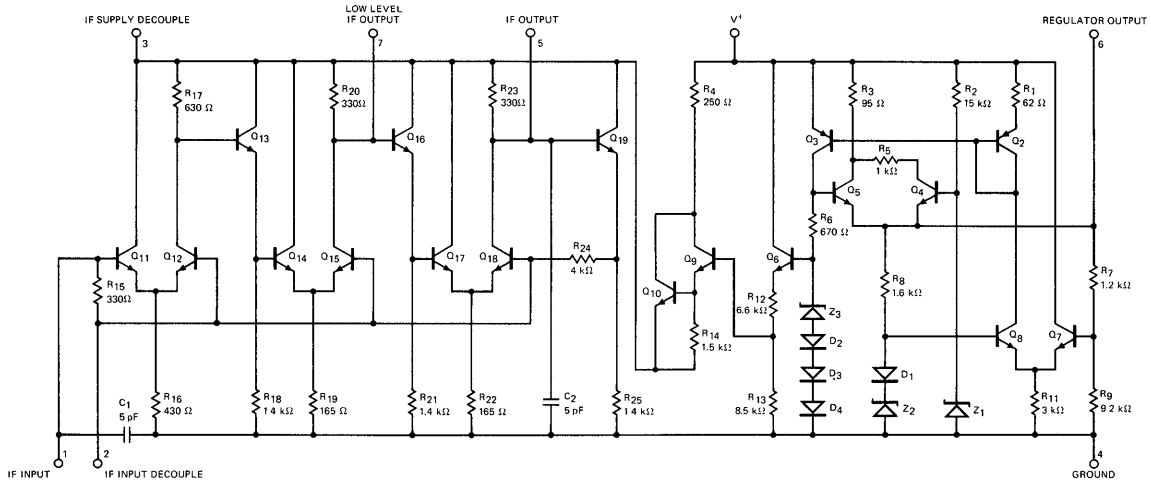
CONNECTION DIAGRAM
8-LEAD MINI DIP
 (TOP VIEW)
 PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
753C	753TC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A753

753C

ELECTRICAL CHARACTERISTICS: ($T_A = 25^\circ\text{C}$, $V_+ = +12\text{ V}$ unless otherwise specified)

PARAMETER	CONDITION	TEST CIRCUIT FIG. NO.	MIN.	TYP.	MAX.	UNITS
DC CHARACTERISTICS						
Supply Voltage Operating Range		3	10		16	V
Supply Current	$R_L = \infty$	3	11	16	19	mA
Power Dissipation	$R_L = \infty$	3		190	230	mW
	$I_L = 5\text{ mA}$	3		210	255	mW
Terminal Voltages	$I_L = 5\text{ mA}$	3				
Pin 1, 2				1.4		V
3				2.6		V
5				2.0		V
6		7.2		7.8	8.3	V
7				2.0		V

AC CHARACTERISTICS IF AMPLIFIER ($f_o = 10.7\text{ MHz}$)

-3 dB Limiting Threshold		1		900		μV
Output Voltage Swing	$V_{IN} = 100\text{ mV}$, $R_L = \infty$	1	1.1	1.4		V_{p-p}
Voltage Gain	$V_{OUT} = 100\text{ mV}$	1	40	50	56	dB
Voltage Gain Change	$-40^\circ\text{C} \leq T_A \leq +25^\circ\text{C}$	1		6.0		dB
	$+25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	1		1.0		dB
Input Impedance:	Pin 1 to Pin 2					
Parallel Input Resistance			230	330	440	Ω
Parallel Input Capacitance			5.0	9.0	14	pF
Output Impedance:	Pin 5 to ground					
Parallel Output Resistance			230	330	440	Ω
Parallel Output Capacitance			5.0	9.0	14	pF
Output Noise Voltage		2		5.0		mV_{RMS}

AC CHARACTERISTICS REGULATOR SECTION

Line Regulation (V_6)	$I_L = 5\text{ mA}$, $V^+ = 10\text{ V to }16\text{ V}$	3		3.0	30	mV
Load Regulation (V_6)	$I_L = 0\text{ to }5\text{ mA}$	3		-10		mV
Temperature Coefficient (V_6)	$I_L = 5\text{ mA}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	3		-0.15		$\text{mV}/^\circ\text{C}$

TEST CIRCUIT FOR DYNAMIC CHARACTERISTICS

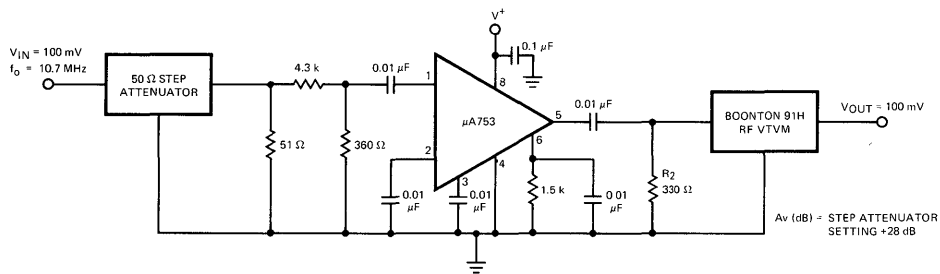


Fig. 1

NOISE MEASUREMENT TEST CIRCUIT

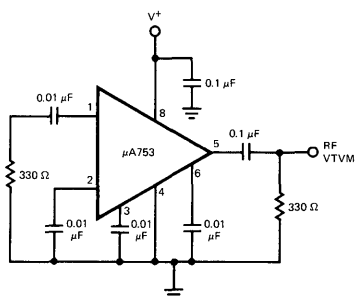


Fig. 2

TEST CIRCUIT FOR STATIC CHARACTERISTICS

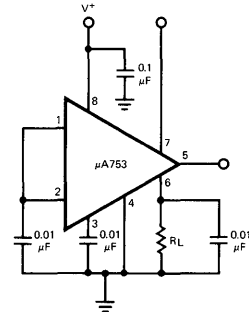
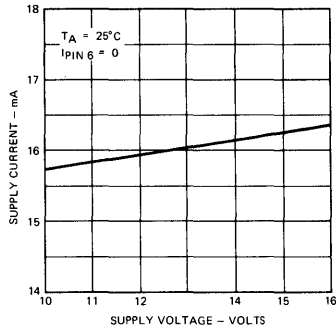


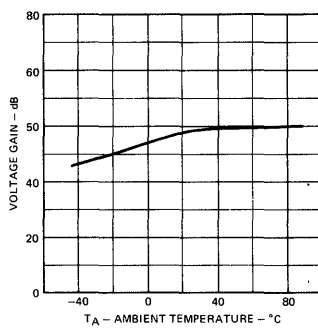
Fig. 3

TYPICAL PERFORMANCE CURVES

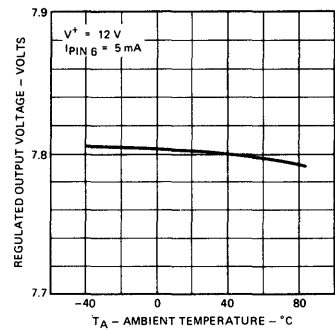
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



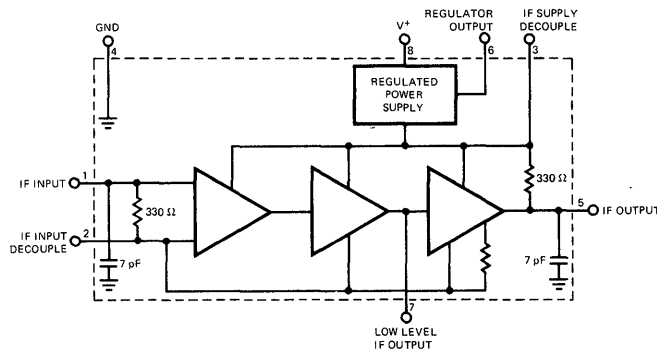
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



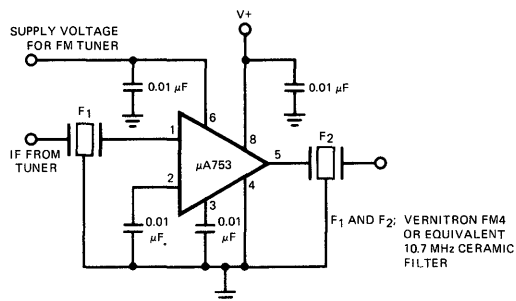
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



BLOCK DIAGRAM



TYPICAL APPLICATION



μA757

GAIN CONTROLLED IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

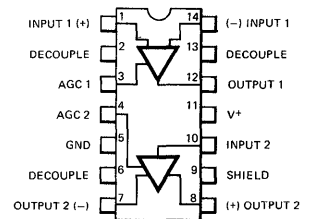
GENERAL DESCRIPTION — The μA757 is a monolithic high performance, Gain Controlled IF Amplifier constructed using the Fairchild Planar* epitaxial process. The amplifier contains two sections which may be operated independently, or in cascade, from audio frequencies to 25 MHz. The μA757 is intended primarily as a gain controlled, intermediate frequency amplifier in AM and FM communications receivers. It also has excellent performance when operated in FM receivers as a limiting amplifier.

- 70 dB GAIN AT 10.7 MHz
- 70 dB AGC RANGE AT 10.7 MHz
- 300 mV SIGNAL HANDLING CAPABILITY AT INPUT
- CONSTANT INPUT AND OUTPUT IMPEDANCE WITH AGC
- STABLE GAIN WITH SUPPLY VOLTAGE AND TEMPERATURE AT ALL LEVELS OF GAIN REDUCTION.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+15V
Voltage at any Output Terminal	+24V
Voltage at either AGC Terminal (Note 1)	±12V
Differential Voltage at either Input (Pins 1 and 14, Pins 2 and 10)	±5V
Internal Power Dissipation (Note 2)	670 mW
Storage Temperature Range	
Hermetic DIP (757, 757C)	-65°C to +150°C
Molded DIP (757C)	-55°C to +125°C
Operating Temperature Range	
Military (757)	-55°C to +125°C
Commercial (757C)	0°C to +70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds) 757	300°C
Molded DIP (Soldering, 10 seconds) 757C	260°C

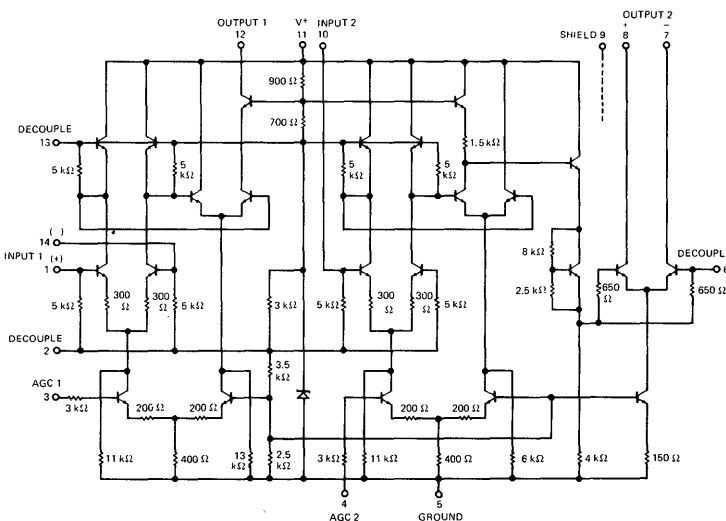
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
757	757DM
757C	757DC
757C	757PC

EQUIVALENT CIRCUIT



7

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A757

757

ELECTRICAL CHARACTERISTICS ($V_+ = +12$ V, $T_A = 25^\circ$ C, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8$ V $V_{AGC\ 1,2} = +3.0$ V	1		13 17	17 20	mA mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8$ V $V_{AGC\ 1,2} = +3.0$ V	1		170 200	210 240	mW mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8$ V, $f = 500$ kHz $V_{AGC\ 1,2} = +0.8$ V, $f = 10.7$ MHz	2 2	65 60	74 70		dB dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, $f = 500$ kHz $V_{AGC\ 1,2} = +1.7$ V, $f = 10.7$ MHz	2 2	20	39 37	46	dB dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, $f = 500$ kHz $V_{AGC\ 1,2} = +3.0$ V, $f = 10.7$ MHz	2 2		2.0 1.0	10 8	dB dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		15	50	μ A
Gain Reduction Sensitivity	$V_{AGC\ 1,2} = +1.7$ V, $f = 500$ kHz	2		50		dB/V
Input Voltage for -3 dB Limiting at Output	$V_{AGC\ 1,2} = +0.8$ V, $f = 500$ kHz	2		0.5		mV
Intermodulation Products	Two-tone signal $f_1 = 500$ kHz, $e_1 = 100$ mV $f_2 = 510$ kHz, $e_2 = 100$ mV $I_{OUT} = 1$ mA p-p	2		-50		dB

SECTION 1

Input Resistance at either Input Terminal	$V_{AGC\ 1} = +0.8$ V, $f = 10.7$ MHz $V_{AGC\ 1} = +3.0$ V, $f = 10.7$ MHz		3.0	5.0 4.5		k Ω k Ω
Input Capacitance at either Input Terminal	$V_{AGC\ 1} = +0.8$ V, $f = 10.7$ MHz $V_{AGC\ 1} = +3.0$ V, $f = 10.7$ MHz			2.5 2.2		pF pF
Output Resistance	$V_{AGC\ 1} = +0.8$ V, $f = 10.7$ MHz $V_{AGC\ 1} = +3.0$ V, $f = 10.7$ MHz			100 100		k Ω k Ω
Output Capacitance	$V_{AGC\ 1} = +0.8$ V, $f = 10.7$ MHz $V_{AGC\ 1} = +3.0$ V, $f = 10.7$ MHz			2.6 2.2		pF pF
Forward Transadmittance	$V_{AGC\ 1} = +0.8$ V, $f = 500$ kHz $V_{AGC\ 1} = +0.8$ V, $f = 10.7$ MHz			14 13		mmho mmho
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, $f = 500$ kHz Output in full limiting		.25	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.0	Volts
Noise Figure	$R_S = 1.0$ k Ω , $f = 10.7$ MHz $R_S = 1.0$ k Ω , $f = 500$ kHz			8.0 8.0		dB dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, $f_c = 500$ kHz Interfering signal, $f_i = 510$ kHz $I_{OUT} = 0.5$ mA p-p, $V_{AGC\ 1} = +0.8$ V			15		mV

SECTION 2

Input Resistance	$V_{AGC\ 2} = +0.8$ V, $f = 10.7$ MHz $V_{AGC\ 2} = +3.0$ V, $f = 10.7$ MHz		3.0	5.0 4.5		k Ω k Ω
Input Capacitance	$V_{AGC\ 2} = +0.8$ V, $f = 10.7$ MHz $V_{AGC\ 2} = +3.0$ V, $f = 10.7$ MHz			2.5 2.2		pF pF
Output Resistance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V, $f = 10.7$ MHz $V_{AGC\ 2} = +3.0$ V, $f = 10.7$ MHz			26 20		k Ω k Ω
Output Capacitance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V, $f = 10.7$ MHz $V_{AGC\ 2} = +3.0$ V, $f = 10.7$ MHz			2.2 2.5		pF pF
Forward Transadmittance	$V_{AGC\ 2} = +0.8$ V, $f = 500$ kHz $V_{AGC\ 2} = +0.8$ V, $f = 10.7$ MHz			440 280		mmho mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, $f = 500$ kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			5.0	6.0	Volts
Power Supply Sensitivity	$V_S = 12$ V to 15 V 0 dB Gain Reduction 30 dB Gain Reduction 60 dB Gain Reduction			0.5 0.8 1.0		dB/V dB/V dB/V

FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A757$

757

ELECTRICAL CHARACTERISTICS ($V_+ = +12\text{ V}$, $T_A = +125^\circ\text{C}$, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8\text{ V}$	1		14	17	mA
	$V_{AGC\ 1,2} = +3.0\text{ V}$			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8\text{ V}$	1		170	210	mW
	$V_{AGC\ 1,2} = +3.0\text{ V}$			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8\text{ V}$, $f = 500\text{ kHz}$	2	55	71		dB
	$V_{AGC\ 1,2} = +0.8\text{ V}$, $f = 10.7\text{ MHz}$	2		62		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7\text{ V}$, $f = 500\text{ kHz}$	2		35		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0\text{ V}$, $f = 500\text{ kHz}$	2		2.0	15	dB
	$V_{AGC\ 1,2} = +3.0\text{ V}$, $f = 10.7\text{ MHz}$	2		-1.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0\text{ V}$	1		15	50	μA

SECTION 1

Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0\text{ V}$, $f = 500\text{ kHz}$ Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1\text{ mA}$, $V_{AGC\ 1} = +3.0\text{ V}$			8.0	9.4	Volts

SECTION 2

Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0\text{ V}$		1.7	2.8	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0\text{ V}$, $f = 500\text{ kHz}$ Output in full limiting		3.8	5.6	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0\text{ mA}$, $V_{AGC\ 2} = +3.0\text{ V}$			6.0	7.0	Volts

757

ELECTRICAL CHARACTERISTICS ($V_+ = +12\text{ V}$, $T_A = -55^\circ\text{C}$, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8\text{ V}$	1		10	17	mA
	$V_{AGC\ 1,2} = +3.0\text{ V}$			14	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8\text{ V}$	1		120	210	mW
	$V_{AGC\ 1,2} = +3.0\text{ V}$			170	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8\text{ V}$, $f = 500\text{ kHz}$	2	55	68		dB
	$V_{AGC\ 1,2} = +0.8\text{ V}$, $f = 10.7\text{ MHz}$	2		64		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7\text{ V}$, $f = 500\text{ kHz}$	2		28		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0\text{ V}$, $f = 500\text{ kHz}$	2		2.0	15	dB
	$V_{AGC\ 1,2} = +3.0\text{ V}$, $f = 10.7\text{ MHz}$	2		-3.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0\text{ V}$	1		30	70	μA

SECTION 1

Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0\text{ V}$, $f = 500\text{ kHz}$ Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1\text{ mA}$, $V_{AGC\ 1} = +3.0\text{ V}$			8.0	9.0	Volts

SECTION 2

Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0\text{ V}$		1.0	1.7	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0\text{ V}$, $f = 500\text{ kHz}$ Output in full limiting		2.3	3.4	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0\text{ mA}$, $V_{AGC\ 2} = +3.0\text{ V}$			4.0	6.0	Volts

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A757

757C

ELECTRICAL CHARACTERISTICS ($V_+ = +12$ V, $T_A = +25^\circ$ C, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC 1,2} = +0.8$ V $V_{AGC 1,2} = +3.0$ V	1		14 18	17 22	mA mA
Internal Power Dissipation	$V_{AGC 1,2} = +0.8$ V $V_{AGC 1,2} = +3.0$ V	1		170 220	210 270	mW mW
Voltage Gain at no Gain Reduction	$V_{AGC 1,2} = +0.8$ V, $f = 500$ kHz $V_{AGC 1,2} = +0.8$ V, $f = 10.7$ MHz	2 2	65 60	74 70		dB dB
Voltage Gain at Partial Gain Reduction	$V_{AGC 1,2} = +1.7$ V, $f = 500$ kHz $V_{AGC 1,2} = +1.7$ V, $f = 10.7$ MHz	2 2	20	39 37	46	dB dB
Voltage Gain at Full Gain Reduction	$V_{AGC 1,2} = +3.0$ V, $f = 500$ kHz $V_{AGC 1,2} = +3.0$ V, $f = 10.7$ MHz	2 2		2.0 1.0	10 8	dB dB
Current into either AGC Terminal	$V_{AGC 1,2} = +3.0$ V	1		15	50	μ A
Gain Reduction Sensitivity	$V_{AGC 1,2} = +1.7$ V, $f = 500$ kHz	2		50		dB/V
Input Voltage for -3 dB Limiting at Output	$V_{AGC 1,2} = +0.8$ V, $f = 500$ kHz	2		0.5		mV
Intermodulation Products	Two-tone signal $f_1 = 500$ kHz, $e_1 = 100$ mV $f_2 = 510$ kHz, $e_2 = 100$ mV $I_{OUT} = 1$ mA p-p	2		-50		dB

SECTION 1

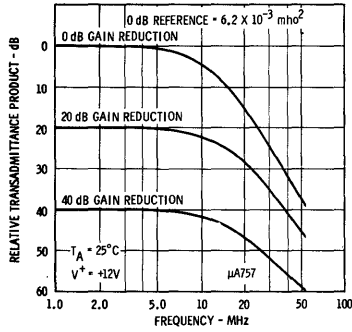
Input Resistance at either Input Terminal	$V_{AGC 1} = +0.8$ V, $f = 10.7$ MHz $V_{AGC 1} = +3.0$ V, $f = 10.7$ MHz		3.0	5.0 4.5		k Ω k Ω
Input Capacitance at either Input Terminal	$V_{AGC 1} = +0.8$ V, $f = 10.7$ MHz $V_{AGC 1} = +3.0$ V, $f = 10.7$ MHz			2.5 2.2		pF pF
Output Resistance	$V_{AGC 1} = +0.8$ V, $f = 10.7$ MHz $V_{AGC 1} = +3.0$ V, $f = 10.7$ MHz			100 100		k Ω k Ω
Output Capacitance	$V_{AGC 1} = +0.8$ V, $f = 10.7$ MHz $V_{AGC 1} = +3.0$ V, $f = 10.7$ MHz			2.6 2.2		pF pF
Forward Transadmittance	$V_{AGC 1} = +0.8$ V, $f = 500$ kHz $V_{AGC 1} = +0.8$ V, $f = 10.7$ MHz			14 13		mmho mmho
Peak-to-Peak Output Current	$V_{AGC 1} = +3.0$ V, $f = 500$ kHz Output in full limiting		.25	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC 1} = +3.0$ V			8.0	9.0	V
Noise Figure	$R_S = 1.0$ k Ω , $f = 10.7$ MHz $R_S = 1.0$ k Ω , $f = 500$ kHz			8.0 8.0		dB dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, $f_c = 500$ kHz Interfering signal, $f_i = 510$ kHz $I_{OUT} = 0.5$ mA p-p, $V_{AGC 1} = +0.8$ V			15		mV

SECTION 2

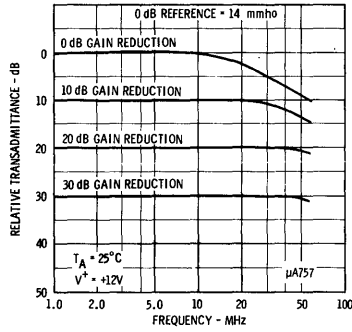
Input Resistance	$V_{AGC 2} = +0.8$ V, $f = 10.7$ MHz $V_{AGC 2} = +3.0$ V, $f = 10.7$ MHz		3.0	5.0 4.5		k Ω k Ω
Input Capacitance	$V_{AGC 2} = +0.8$ V, $f = 10.7$ MHz $V_{AGC 2} = +3.0$ V, $f = 10.7$ MHz			2.5 2.2		pF pF
Output Resistance at either Output Terminal	$V_{AGC 2} = +0.8$ V, $f = 10.7$ MHz $V_{AGC 2} = +3.0$ V, $f = 10.7$ MHz			26 20		k Ω k Ω
Output Capacitance at either Output Terminal	$V_{AGC 2} = +0.8$ V, $f = 10.7$ MHz $V_{AGC 2} = +3.0$ V, $f = 10.7$ MHz			2.2 2.5		pF pF
Forward Transadmittance	$V_{AGC 2} = +0.8$ V, $f = 500$ kHz $V_{AGC 2} = +0.8$ V, $f = 10.7$ MHz			440 280		mmho mmho
Quiescent Output Current at either Output Terminal	$V_{AGC 2} = +3.0$ V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC 2} = +3.0$ V, $f = 500$ kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC 2} = +3.0$ V			5.0	6.0	V
Power Supply Sensitivity	$V_S = 12$ V to 15 V 0 dB Gain Reduction 30 dB Gain Reduction 60 dB Gain Reduction			0.5 0.8 1.0		dB/V dB/V dB/V

TYPICAL PERFORMANCE CURVES FOR 757 AND 757C

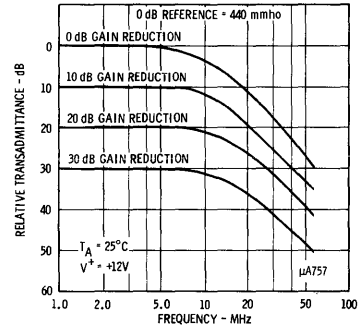
PRODUCT OF SECTIONS 1 AND 2 FORWARD TRANSMITTANCE AS A FUNCTION OF FREQUENCY



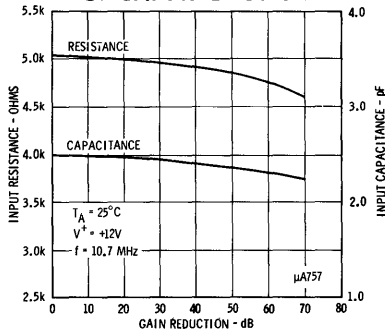
SECTION 1 FORWARD TRANSMITTANCE AS A FUNCTION OF FREQUENCY



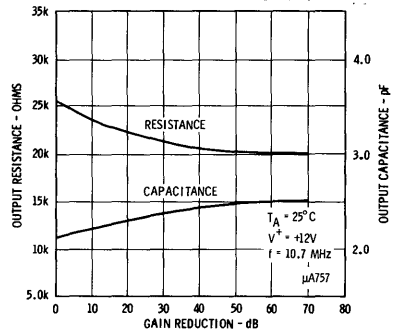
SECTION 2 FORWARD TRANSMITTANCE AS A FUNCTION OF FREQUENCY



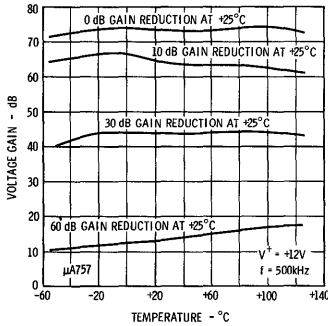
SECTION 1 AND 2 INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



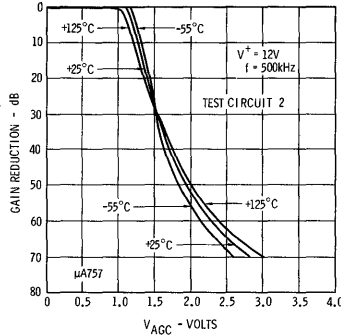
SECTION 2 OUTPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



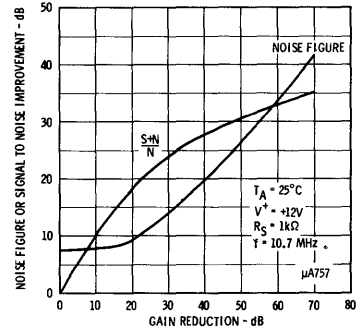
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



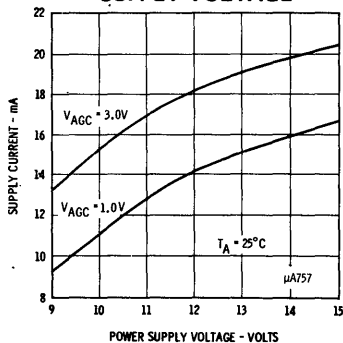
GAIN REDUCTION AS A FUNCTION OF GAIN CONTROL VOLTAGE



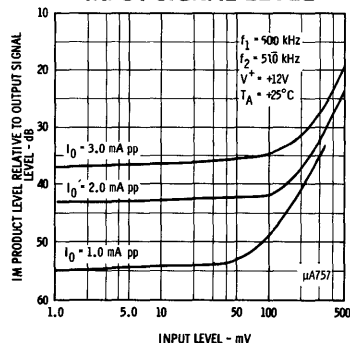
SIGNAL TO NOISE RATIO IMPROVEMENT AND NOISE FIGURE AS A FUNCTION OF GAIN REDUCTION



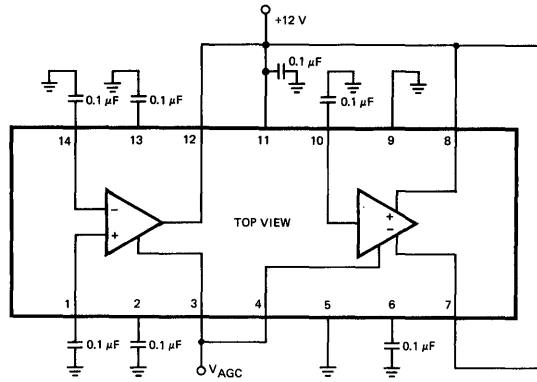
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



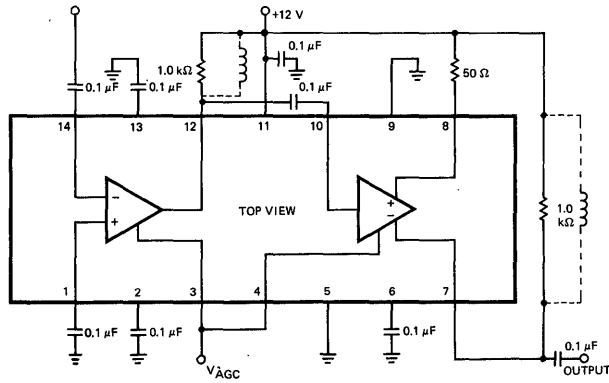
TWO TONE IM DISTORTION PRODUCTS AS A FUNCTION OF INPUT SIGNAL LEVEL



TEST CIRCUIT 1 (NOTE 3)



TEST CIRCUIT 2 (NOTE 2)



NOTES

1. For supply voltages less than +12 V, the absolute maximum voltage at either AGC terminal is equal to the supply voltage.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C.
3. For 10.7 MHz measurements, interstage capacitance and Section 2 output capacitance are tuned out. Pin 9 should be connected to GND.

μA758

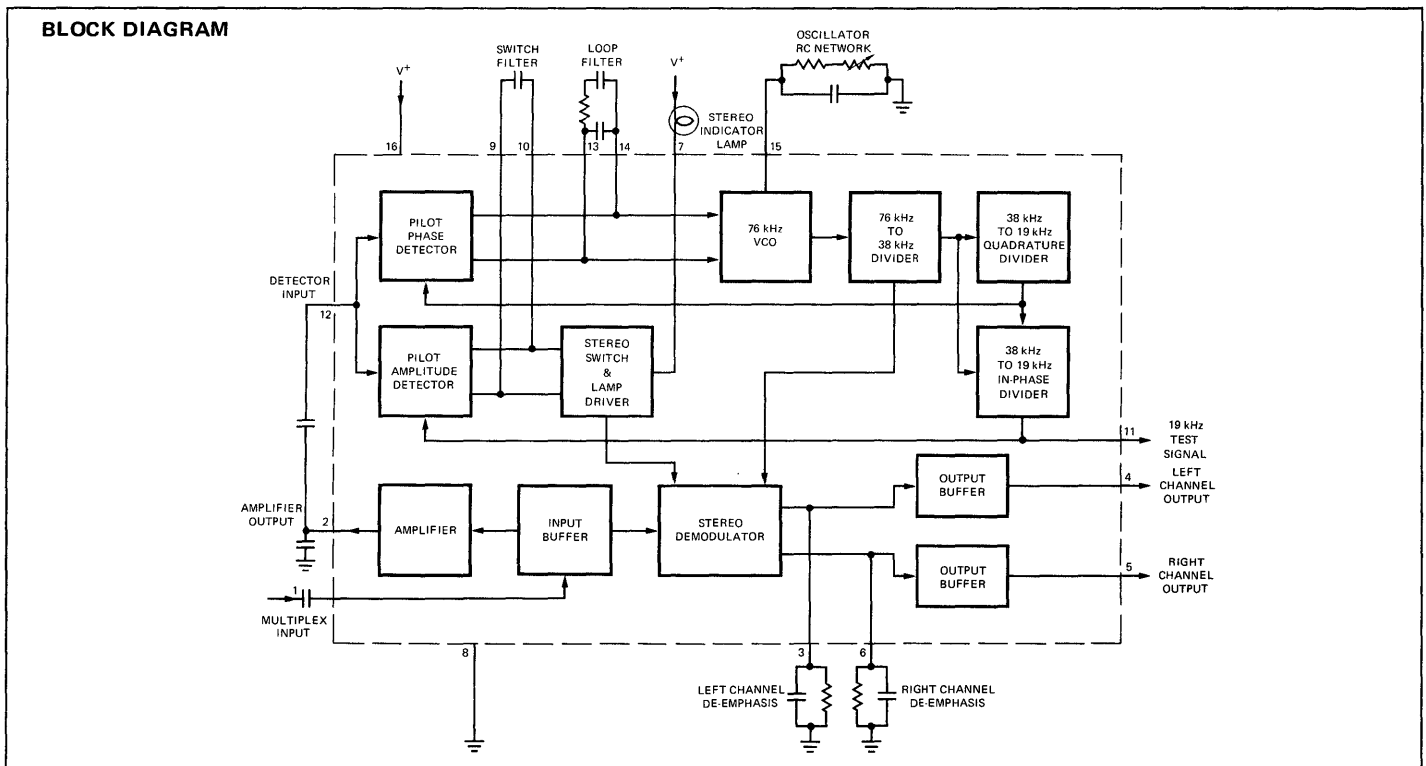
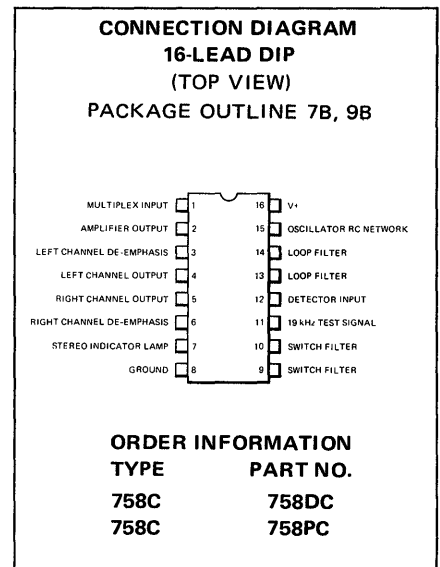
PHASE LOCKED LOOP FM STEREO MULTIPLEX DECODER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA758 is a monolithic Phase Locked Loop FM Stereo Multiplex decoder using the Fairchild Planar* epitaxial process. This integrated circuit decodes an FM Stereo Multiplex Signal into Right and Left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. Internal functions include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust: a potentiometer to set oscillator frequency. No external coils are required. The μA758 is suitable for all line-operated and automotive FM Stereo Receivers.

- 45 dB CHANNEL SEPARATION
- AUTOMATIC STEREO/MONO SWITCHING
- STEREO INDICATOR LAMP DRIVER WITH CURRENT LIMITING
- HIGH IMPEDANCE INPUT — LOW IMPEDANCE OUTPUTS
- 70 dB SCA REJECTION
- ONE ADJUSTMENT FOR COMPLETE ALIGNMENT
- LOW NUMBER OF EXTERNAL PARTS — NO COILS
- 10 V TO 16 V SUPPLY VOLTAGE RANGE



Notes on following page.

*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Supply Voltage (\leq 15 Seconds)	+22 V
Voltage at Lamp Driver Terminal (Lamp OFF)	+22 V
Internal Power Dissipation (Note 1)	730 mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C

758C

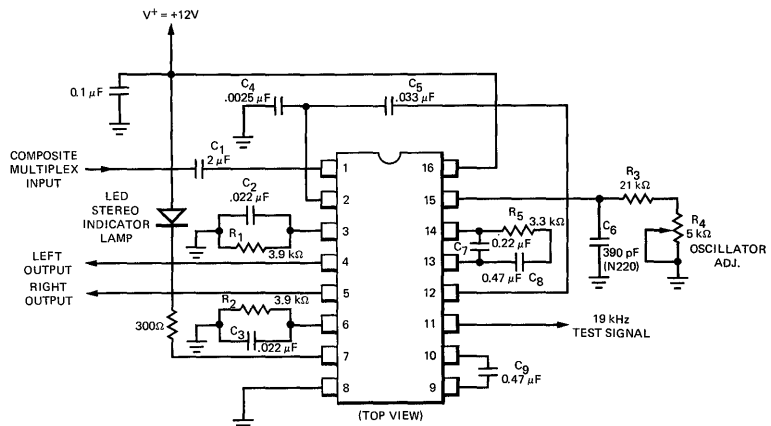
ELECTRICAL CHARACTERISTICS [$T_A = 25^\circ\text{C}$, $V^+ = +12\text{ V}$, 19 kHz pilot level = 30 mV_{RMS}, Multiplex Signal (L = R, pilot OFF) = 300 mV_{RMS}, Modulation Frequency = 400 Hz or 1 kHz, Test Circuit 1, unless otherwise specified]

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
Supply Current	Lamp OFF		26	35	mA
Maximum Available Lamp Current		75	150		mA
Voltage at Lamp Driver Terminal	$I_{LAMP} = 50\text{ mA}$		1.3	1.8	V
DC Voltage Shift at Either Output Terminal	Stereo to Mono Operation		30	150	mV
Power Supply Ripple Rejection	200 Hz, 200 mV _{RMS}	35	45		dB
Input Resistance		20	35		k Ω
Output Resistance		0.9	1.3	2.0	k Ω
Channel Separation	100 Hz		40		dB
	400 Hz	30	45		dB
	10 kHz		45		dB
Channel Balance			0.3	1.5	dB
Voltage Gain	1 KHz	0.5	0.9	1.4	V/V
Pilot Input Level	Lamp Turn-On		15	20	mV _{RMS}
	Lamp Turn-Off	2.0	7.0		mV _{RMS}
Pilot Input Level Hysteresis	Lamp Turn-Off to Turn-On	3.0	7.0		dB
Capture Range		2.0	4.0	6.0	%
Total Harmonic Distortion	Multiplex Level = 600 mV _{RMS} Pilot OFF		0.4	1.0	%
19 kHz Rejection		25	35		dB
38 kHz Rejection		25	45		dB
SCA Rejection (Note 2)			70		dB
VCO Tuning Resistance (Note 3)		21.0	23.3	25.5	k Ω
VCO Frequency Drift	$0^\circ\text{C} \leq T_A \leq 25^\circ\text{C}$		+0.1	± 2	%
	$25^\circ \leq T_A \leq +70^\circ\text{C}$		-0.4	± 2	%

NOTES:

- (1) Rating applied for ambient temperatures to 70°C. Derate at 9.1 mW/°C from 70°C to 85°C.
- (2) Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
- (3) Total resistance from pin 15 to ground, in test circuit 1, required to set reference frequency at pin 11 to 19 KHz ± 10 Hz.

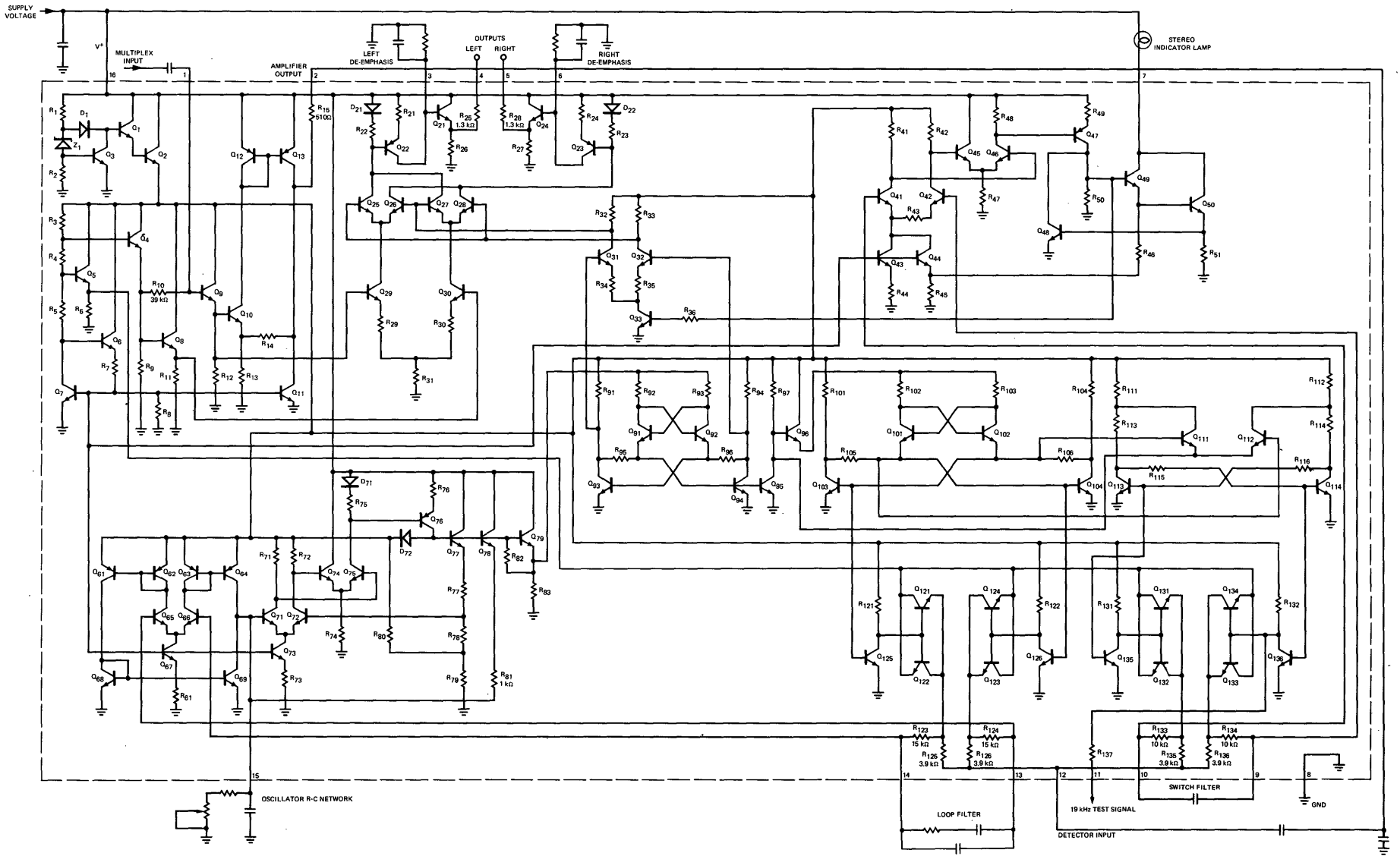
TEST CIRCUIT 1 AND TYPICAL APPLICATION



NOTE:

Tolerance on resistors is $\pm 5\%$ and tolerance on capacitors is $\pm 20\%$ unless otherwise specified.

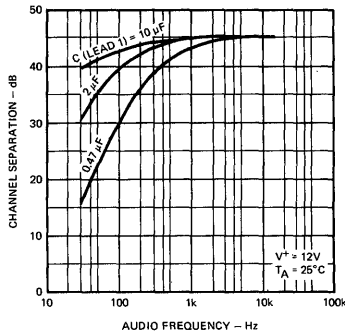
- C_1 Tolerance = +100%, -20%
- C_6 Tolerance = $\pm 1\%$ in test circuit and $\pm 5\%$ in typical application
- R_3 Tolerance = $\pm 1\%$
- R_4 Tolerance = $\pm 10\%$
- R_1 and R_2 Tolerances = $\pm 1\%$ in test circuit and $\pm 5\%$ in typical application.



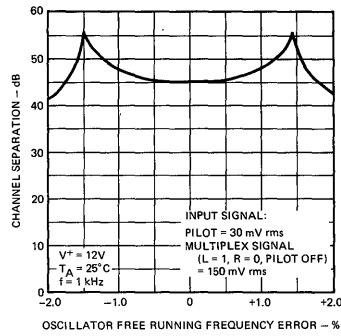
EQUIVALENT CIRCUIT

TYPICAL PERFORMANCE CURVES FOR 758C
(Test Circuit 1 unless Otherwise Specified)

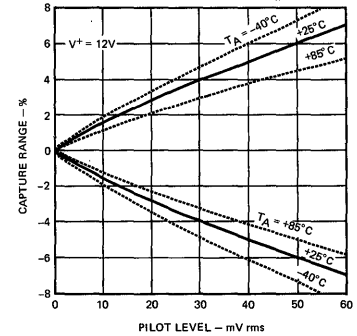
CHANNEL SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



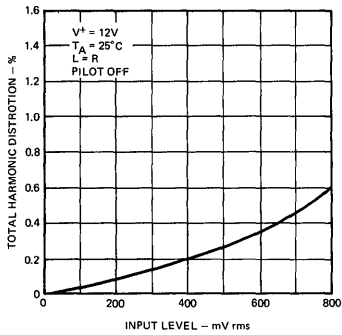
CHANNEL SEPARATION AS A FUNCTION OF OSCILLATOR FREE RUNNING FREQUENCY ERROR



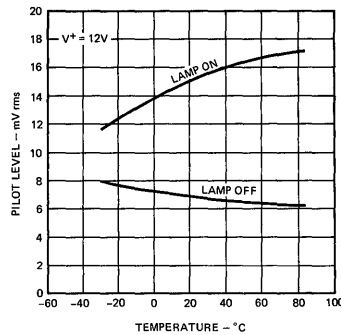
CAPTURE RANGE AS A FUNCTION OF PILOT LEVEL



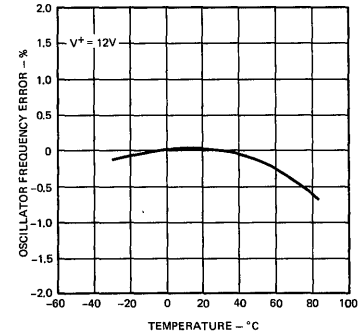
TOTAL HARMONIC DISTORTION AS A FUNCTION OF INPUT LEVEL



LAMP TURN ON AND TURN OFF SENSITIVITY AS A FUNCTION OF AMBIENT TEMPERATURE



OSCILLATOR FREE RUNNING FREQUENCY ERROR AS A FUNCTION OF AMBIENT TEMPERATURE



μA767 • μA769

FM STEREO MULTIPLEX DECODERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

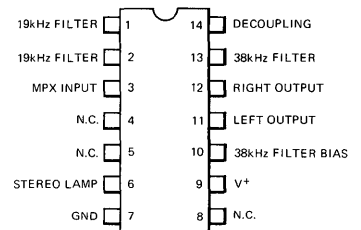
GENERAL DESCRIPTION — The μA767 and μA769 are monolithic FM Stereo Multiplex Decoder systems constructed using the Fairchild Planar* epitaxial process. They are electrically identical; however, the right and left stereo outputs are reversed for the μA769. These integrated circuits demodulate a stereo multiplex signal into the right and left audio channels while inherently suppressing SCA frequency components. Internal provision is made for driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement make the μA767 • μA769 suitable for all line-operated and automotive FM stereo multiplex applications.

- 45 dB CHANNEL SEPARATION
- 55 dB STORECAST REJECTION WITHOUT SCA FILTERS
- HIGH CURRENT STEREO INDICATOR LAMP DRIVER
- OPERATION WITH 8 V TO 14 V SUPPLIES

ABSOLUTE MAXIMUM RATINGS

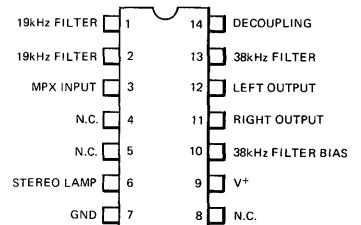
Supply Voltage (Note 1)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver Terminal (Note 2)	100 mA
Internal Power Dissipation	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	767C, 769C +300°C
Molded DIP (Soldering, 10 seconds)	767C, 769C +260°C

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A
μA767



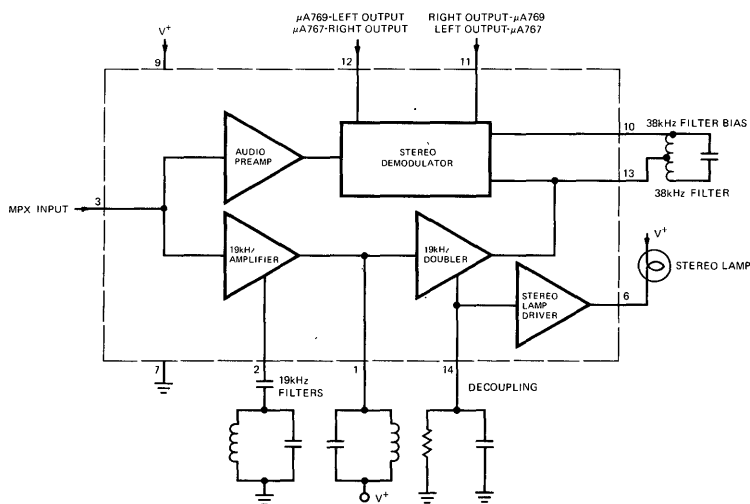
ORDER INFORMATION	
TYPE	PART NO.
767C	767DC
767C	767PC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A
μA769



ORDER INFORMATION	
TYPE	PART NO.
769C	769DC
769C	769PC

BLOCK DIAGRAM (μA767 and μA769)



Notes on following page.

*Planar is a patented Fairchild process.

767C AND 769C

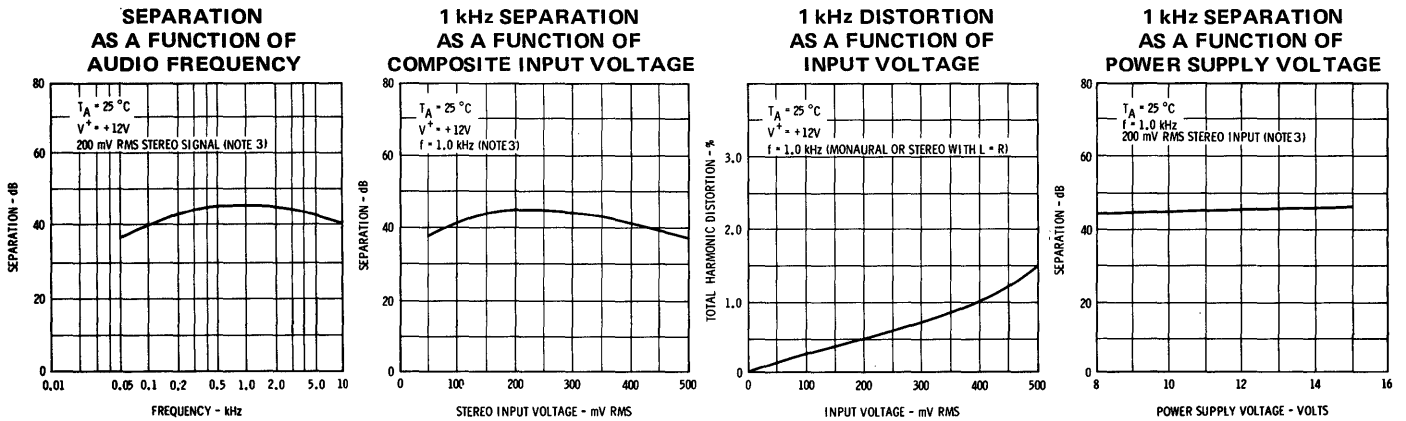
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V^+ = +12\text{V}$, 200 mV RMS standard stereo multiplex signal applied to input, unless otherwise specified (Note 3). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Current		12	18	mA
Input Resistance	12	20		k Ω
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz	30	45		dB
f = 10 kHz	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 4)		55		dB
19 kHz Pilot Level Required at Input for:			22	
Stereo Indicator Lamp on		12		mV RMS
Stereo Indicator Lamp off	4.0	8.0		mV RMS
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

- (1) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.
- (2) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.
- (3) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L=1 and R=1 as described in the FCC Rules on FM Broadcasting.
- (4) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES FOR 767C AND 769C



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A767 • μ A769

μ A767 • μ A769 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

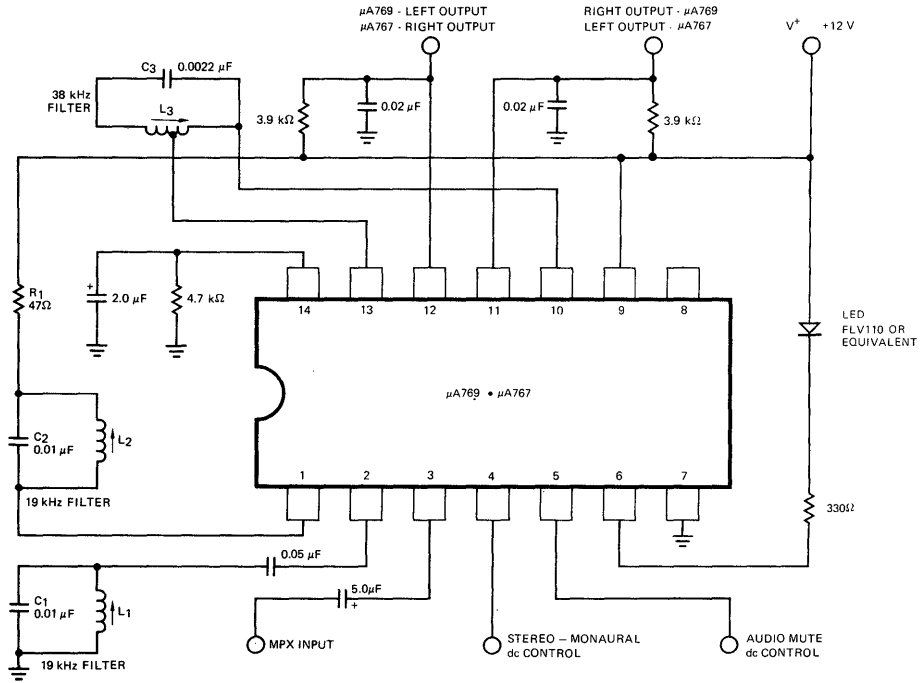
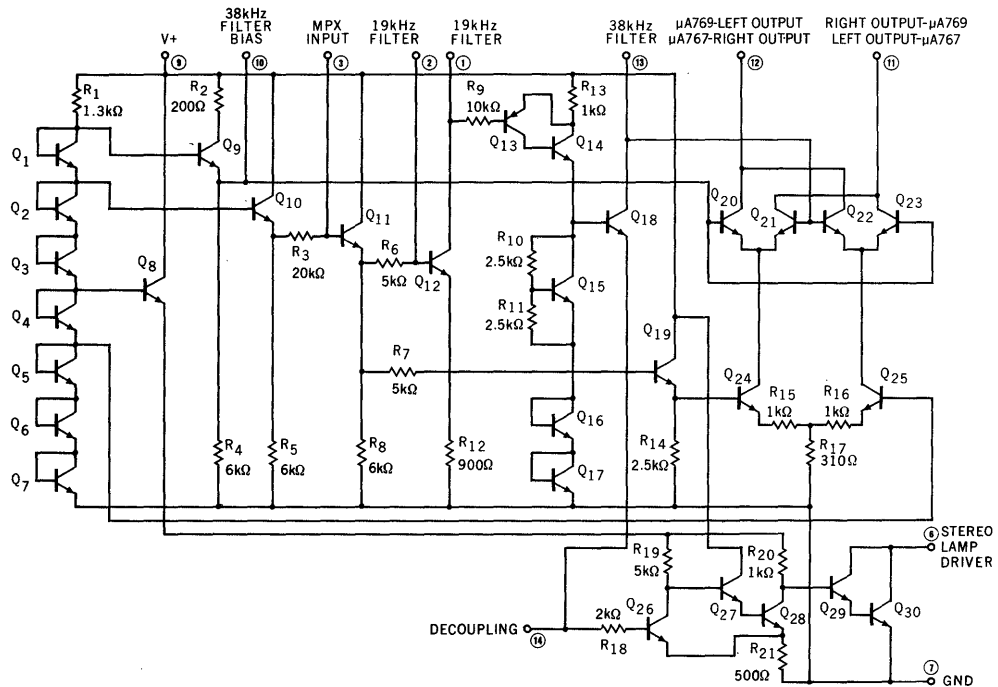


Fig. 1

NOTES:

- (1) Capacitors C_1 , C_2 , and C_3 should be polystyrene or mylar.
- (2) Coils L_1 and L_2 are 7.0 mH nominal with $Q_{UL} = 60$ (Miller #1361 or equivalent).
- (3) Coil L_3 is 8.0 mH nominal with $Q_{UL} = 80$, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
- (4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μ A767 • μ A769 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA780

CHROMA SUBCARRIER REGENERATOR (PHASE LOCKED LOOP)

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA780 is a monolithic Phase Locked Loop designed for use as a color TV subcarrier regenerator and is constructed using the Fairchild Planar* epitaxial process. This integrated circuit, which uses an automatic phase control (APC) loop, accepts the composite NTSC color video signal, extracts the color subcarrier reference and generates a CW signal suitable for use as a chroma demodulation reference. Other features include control of the CW phase (tint) by a dc voltage, blanking of the CW output during burst time and synchronous generation of an automatic color control (ACC) voltage.

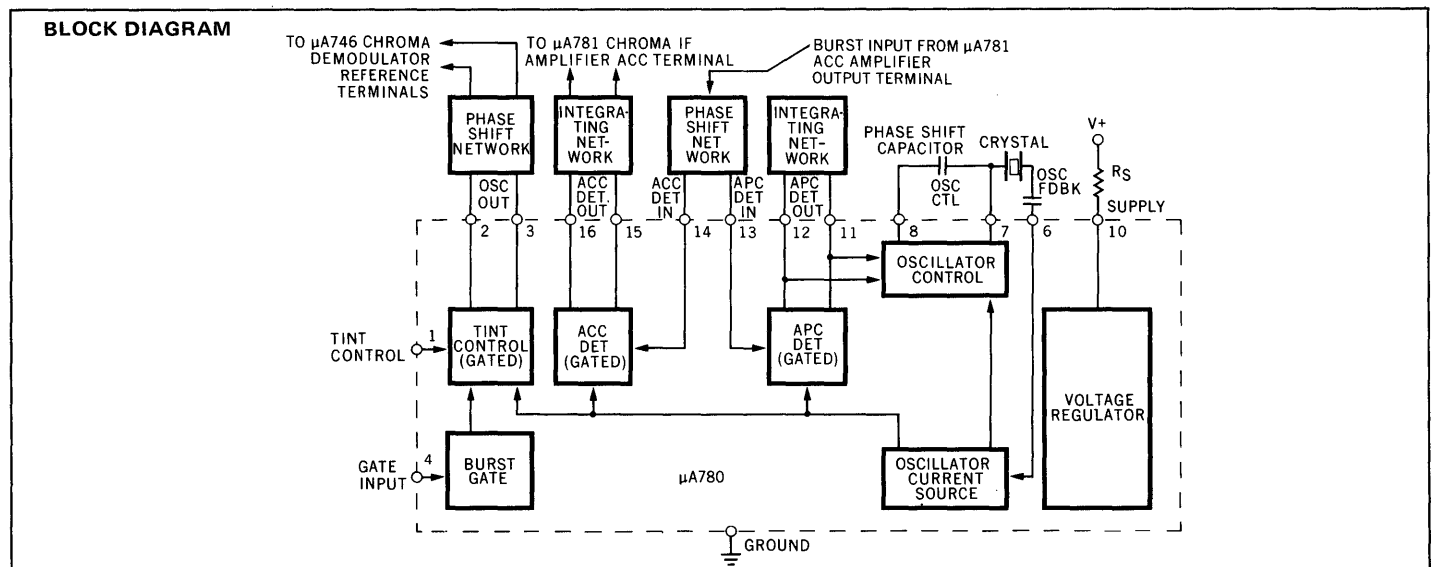
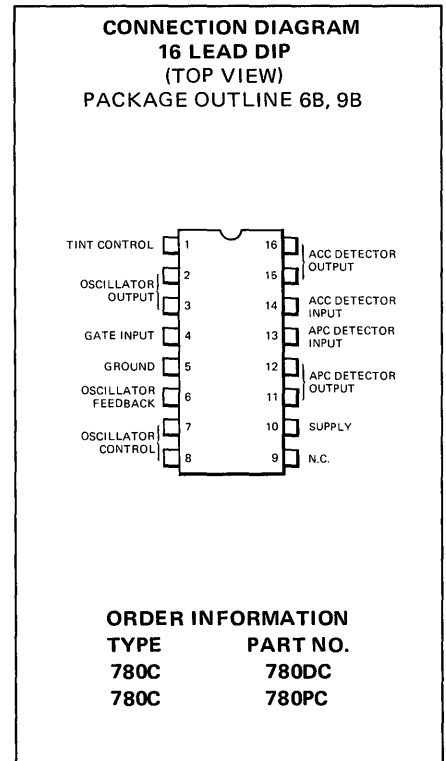
The μA780 in combination with the μA781 Chroma IF Amplifier and the μA746 Chroma Demodulator forms a complete low cost, high quality chroma processing system for color TV receivers.

The μA780 is also useful as a communications phase locked loop system to select, amplify and demodulate AM, FM, FSK and SSB signals.

- COMPLETE COLOR TV SUBCARRIER REGENERATOR
- AUTOMATIC PHASE CONTROL LOOP
- DC TINT CONTROL
- SYNCHRONOUS ACC/KILLER DETECTOR
- COLOR BURST GATING AND BLANKING
- INTERNALLY REGULATED SUPPLY

ABSOLUTE MAXIMUM RATINGS

Supply Current	40 mA
Current into Gate Input Terminal	5 mA
Peak-to-Peak Voltage at either APC or ACC Detector Input Terminals	5 V
Internal Power Dissipation	730 mW
Storage Temperature Range	-55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A780

780C

DC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Gate "ON", Test Circuit 1 unless otherwise specified)

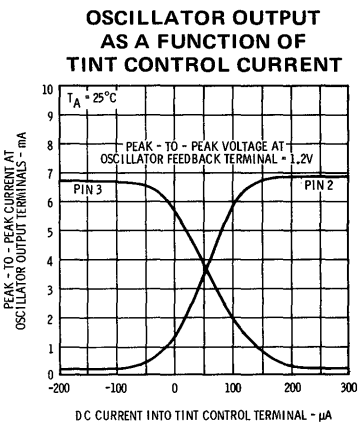
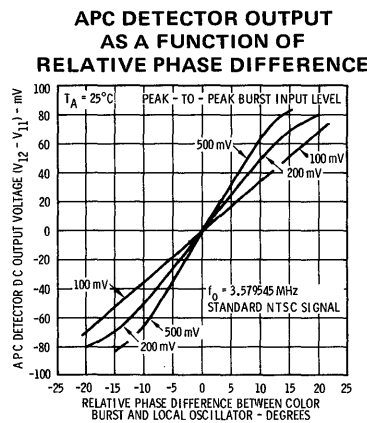
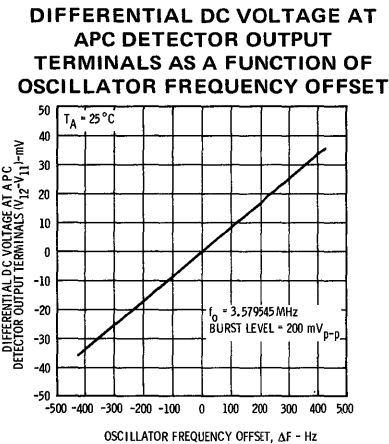
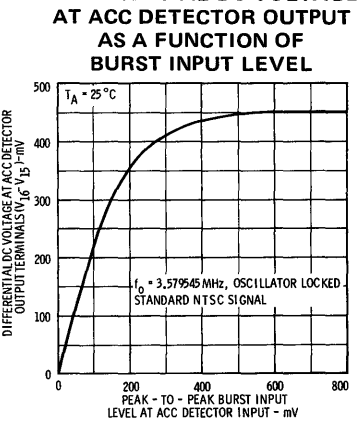
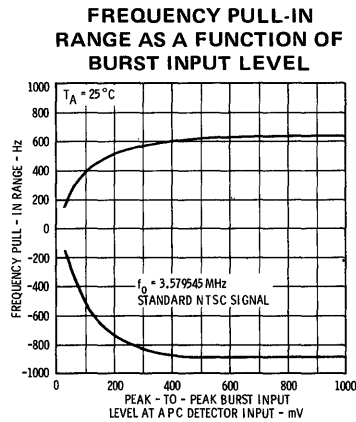
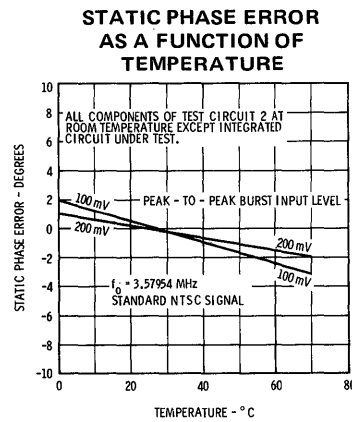
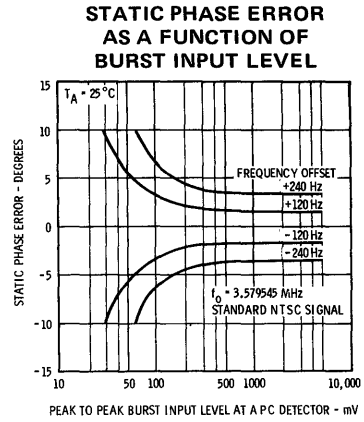
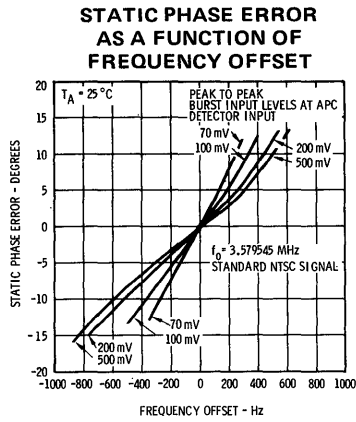
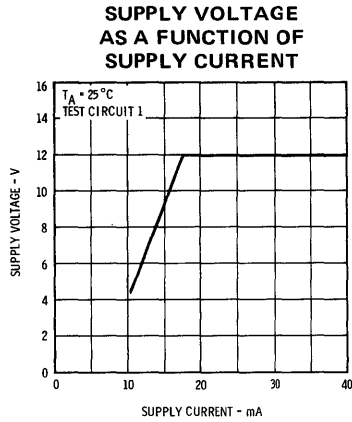
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current			26		mA
Voltage at Supply Terminal		11.3	12.0	12.6	V
Supply Regulation (ΔV_{10})	$V_+ = 22\text{ V}$ to $V_+ = 27\text{ V}$		40	200	mV
Total Current into Oscillator Output Terminals	Gate "OFF", 50 k Ω resistor connected between Pin 10 and Pin 6, Pin 2 shorted to Pin 3	4.2	5.8	7.6	mA
Current into Either APC Detector Output Terminal	12 k Ω resistor connected between Pin 6 and Ground		12	40	μ A
Offset Voltage between ACC Detector Output Terminals ($V_{15} - V_{16}$)	50 k Ω resistor connected between Pin 10 and Pin 6	-330	-70	+330	mV
Offset Voltage between APC Detector Output Terminals ($V_{11} - V_{12}$)	50 k Ω resistor connected between Pin 10 and Pin 6	-375	-50	+375	mV
Offset Voltage between Oscillator Control Terminals ($V_7 - V_8$)	12 k Ω resistor connected between Pin 6 and Ground, $V_{11} = V_{12} = 9.5\text{ V}$	-330	-20	+330	mV
Offset Voltage between Oscillator Output Terminals ($V_2 - V_3$)	Gate "OFF"	-200	+300	+800	mV
Voltage at Oscillator Feedback Terminal			2.8		V
Voltage at ACC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at APC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at Tint Control Terminal			200	300	mV
Voltage at Tint Control Terminal	Gate "OFF"	7.3	7.6	8.2	V
Internal Power Dissipation			310	400	mW

780C

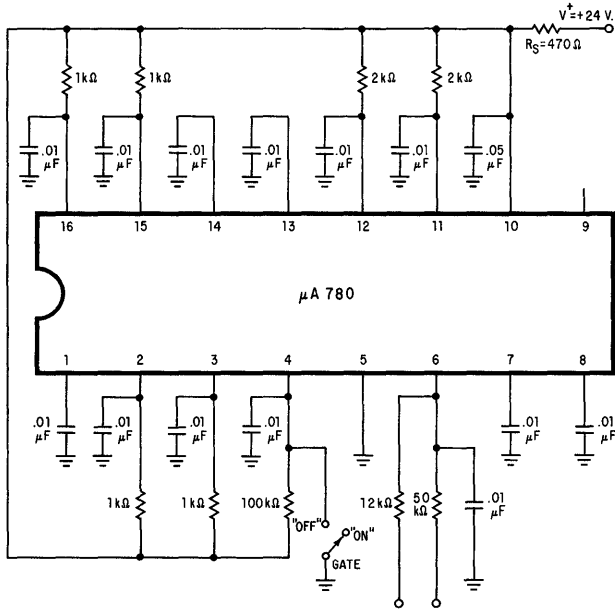
AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, peak-to-peak burst level at APC Detector Input Terminal = 200 mV. Standard NTSC Signal, $f_o = 3.579545\text{ MHz}$, Test Circuit 2 unless otherwise specified.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Oscillator Pull-in Range	$f_{\text{free run}} > f_o$		400		Hz
	$f_{\text{free run}} < f_o$		-400		Hz
Oscillator Static Phase Error	$f_{\text{free run}} = f_o + 120\text{ Hz}$		+2.2		Degree
	$f_{\text{free run}} = f_o - 120\text{ Hz}$		-2.2		Degree
Oscillator Control Sensitivity			12		Hz/mV
Input Resistance at Oscillator Feedback Terminal			2.2		k Ω
Input Capacitance at Oscillator Feedback Terminal			4.5		pF
Peak-to-Peak Current at Oscillator Output Terminal (Pin 3)	Tint Control Wiper at Ground		6.8		mA
ACC Detector Input Resistance			2.2		k Ω
ACC Detector Input Capacitance			4.5		pF
ACC Detector Sensitivity	100 mV _{p-p} burst level at ACC Detector Input Terminal, Oscillator Locked		+2.2		mVdc/mV _{p-p}
APC Detector Input Resistance			2.2		k Ω
APC Detector Input Capacitance			4.5		pF
APC Detector Sensitivity			5.0		mV/Degree

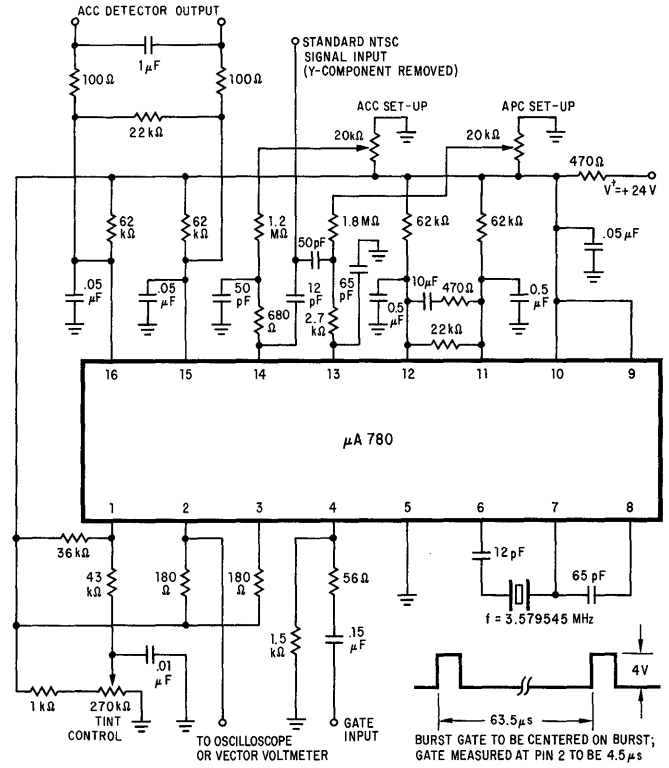
TYPICAL PERFORMANCE CURVES FOR 780C
(Test Circuit 2 unless otherwise specified)



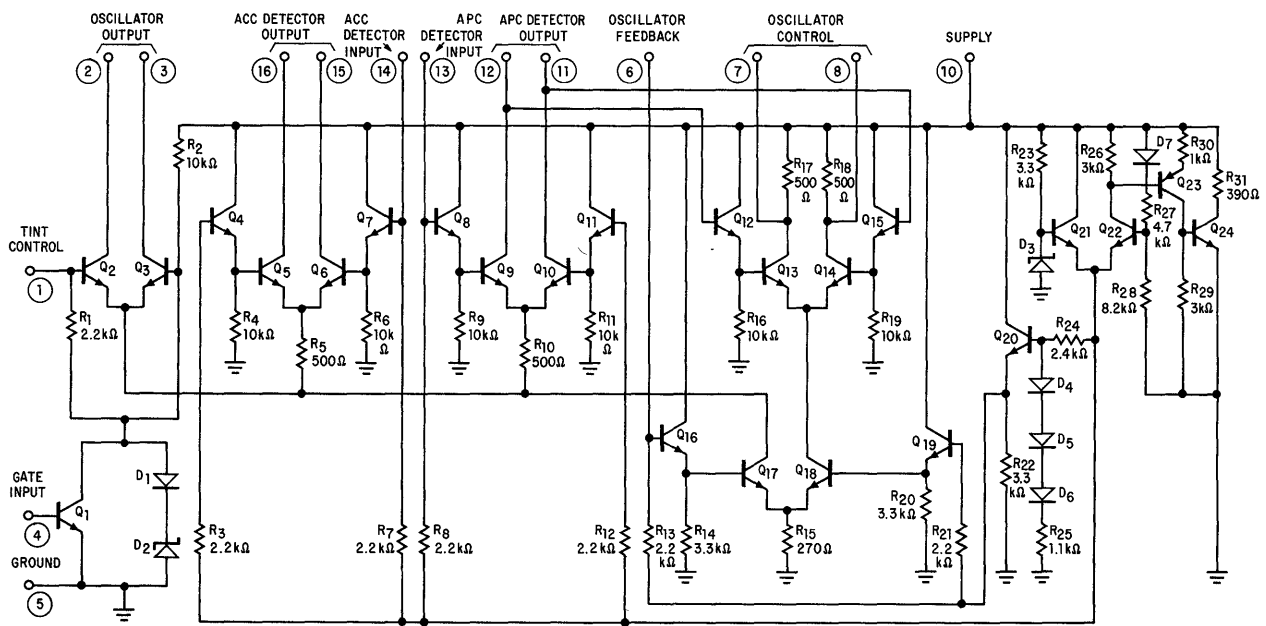
TEST CIRCUIT 1



TEST CIRCUIT 2

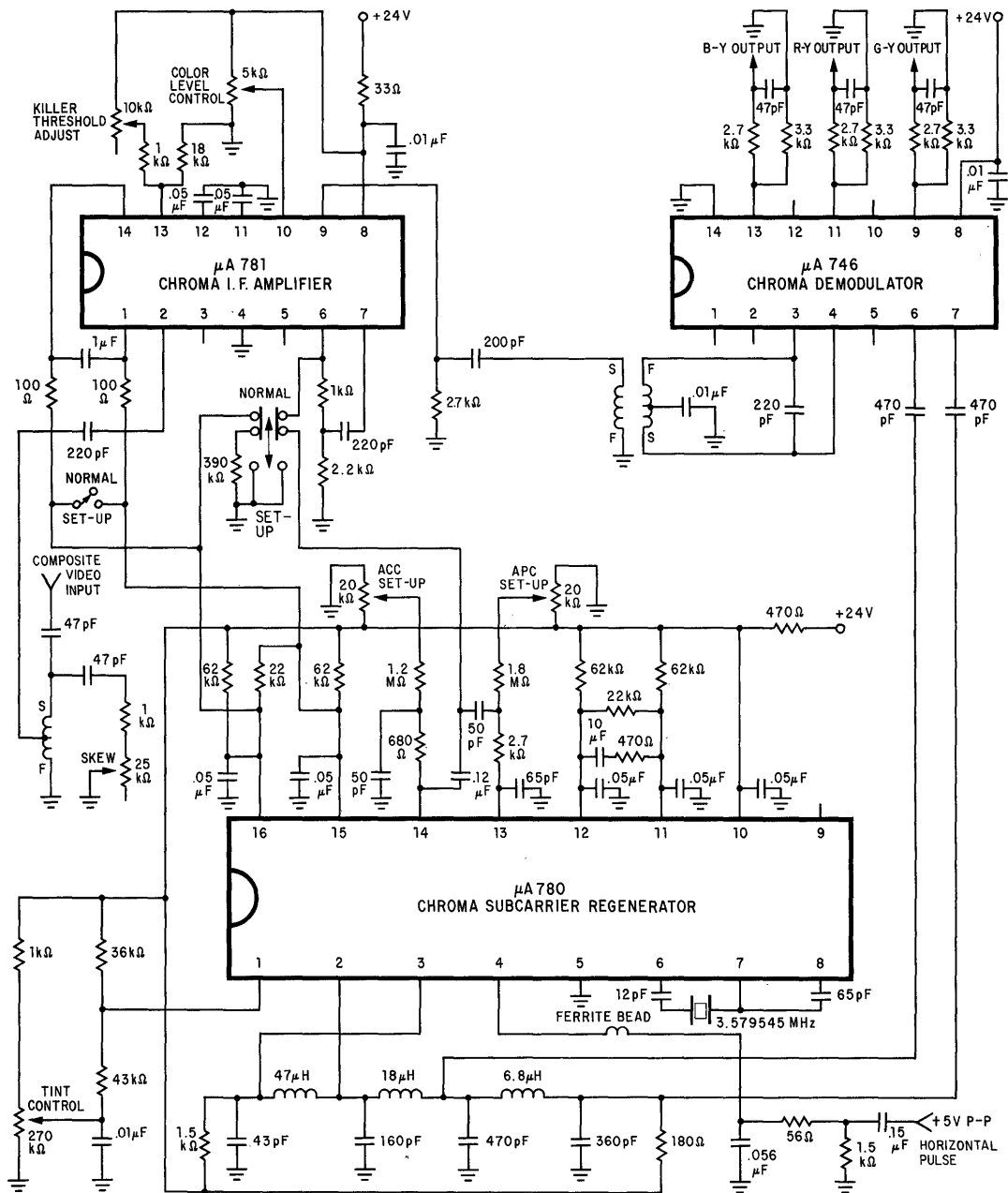


EQUIVALENT CIRCUIT

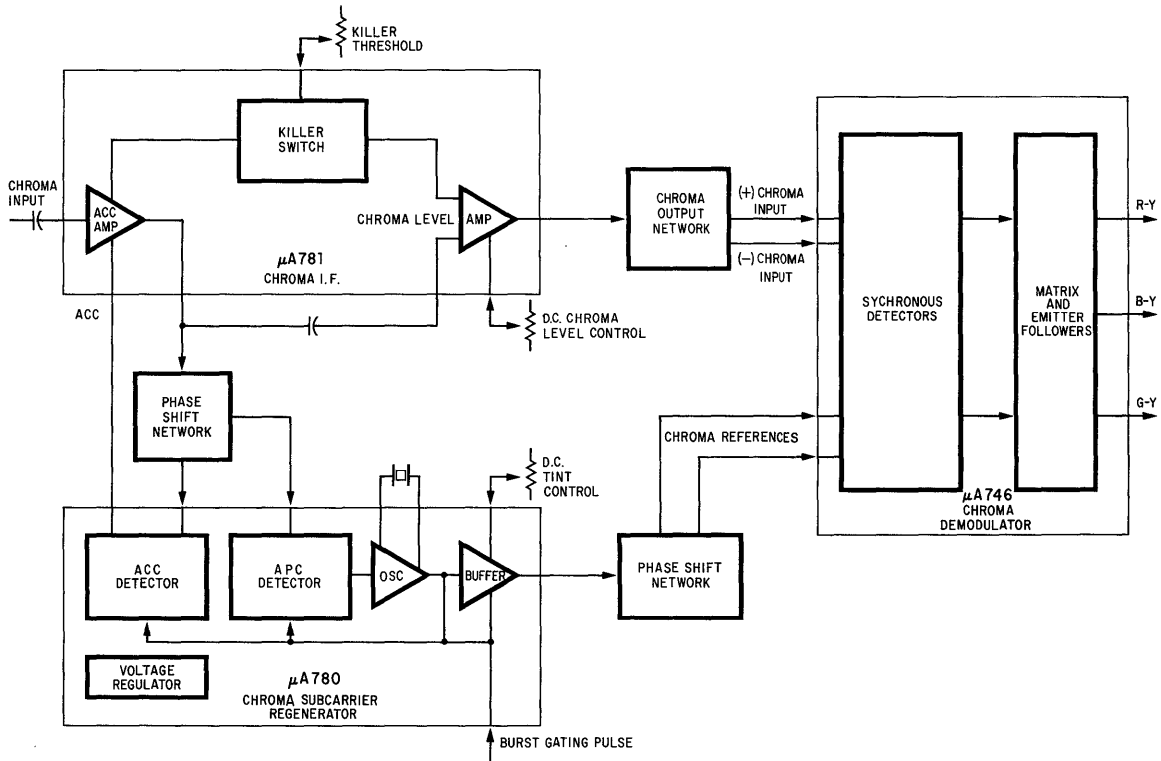


○ = Pin Numbers

INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM
(COMPLETE SCHEMATIC)



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM
(BLOCK DIAGRAM)



μA781

GAIN CONTROLLED IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA781 is a monolithic Gain Controlled IF Amplifier for color TV constructed using the Fairchild Planar* epitaxial process. The first section is a gain controlled chroma signal amplifier whose output is used to drive a subcarrier regenerator circuit. The gain of the second section is controlled by means of an external dc voltage to set chroma level. In addition, the second stage may be gated off to provide "color killing" action in the absence of a color signal with the trip point of the gate adjusted externally.

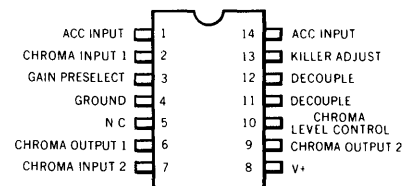
The μA781 in combination with the μA780 Phase Locked Loop Subcarrier Regenerator and the μA746 Chroma Demodulator forms a complete low cost, high quality chroma processing system for color TV receivers.

- COMPLETE COLOR TV CHROMA IF AMPLIFIER
- 10 MHz BANDWIDTH
- AUTOMATIC COLOR CONTROL (ACC) AMPLIFIER
- DC CHROMA LEVEL CONTROL
- ADJUSTABLE COLOR KILLER
- OUTPUT SHORT CIRCUIT PROTECTION

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30 V
Internal Power Dissipation	670 mW
Storage Temperature Range	-55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C
Output Short Circuit Duration	30 seconds

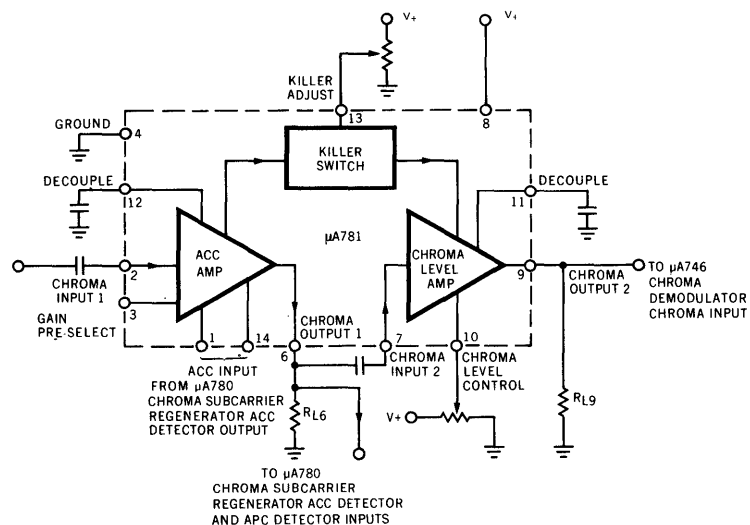
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
781C	781DC
781C	781PC

BLOCK DIAGRAM



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A781

781C

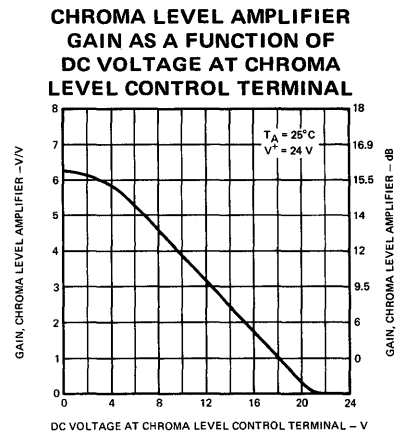
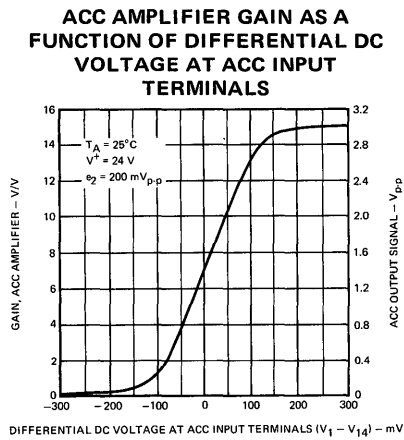
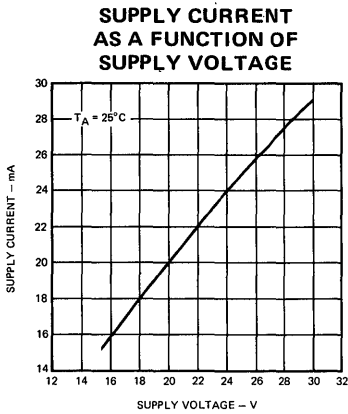
ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
Supply Current	$R_{L6} = R_{L9} = 1 \text{ M}\Omega$ (Note 1)	8.0	13	18	mA
		17	24	31	mA
Internal Power Dissipation			400	550	mW
Short Circuit Load Current, Chroma Output 1	$R_{L6} = 0 \Omega$	20	42		mA
Short Circuit Load Current, Chroma Output 2	$R_{L9} = 0 \Omega$	20	36		mA
DC Voltage at Chroma Output 1 Terminal		15.5	17.5	20	V
DC Voltage at Chroma Output 2 Terminal		17.5	18	18.5	V
Gain, ACC Amplifier Stage		14	17	19	dB
Output Voltage Sensitivity of ACC Amplifier to ACC Control Voltage	$V_{ACC} = V_1 - V_{14} = 0 \text{ mV}$ to $V_1 - V_{14} = -75 \text{ mV}$	11	14	16	mV _{p-p} /mV _{dc}
Maximum Gain, Chroma Level Amplifier Stage		12	15.8	17	dB
DC Voltage at Chroma Level Control Terminal for 90% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control Set for 90% Maximum Output	3.0	5.0	5.5	V
DC Voltage at Chroma Level Control Terminal for 10% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control Wiper set for 10% of Maximum Output	17	19.5	22	V
Killer "ON" Threshold (Pin 13)			16.6	17	V
Killer "OFF" Threshold (Pin 13)		16	16.3		V
DC Voltage at Decouple Terminal, Pin 11		15	15.5	16	V
DC Voltage at Decouple Terminal, Pin 12		14.5	15.3	16	V
DC Voltage at Gain Preselect Terminal		0.7	1.0	1.2	V
DC Voltage at Chroma Input 1 Terminal			1.7		V
DC Voltage at Chroma Input 2 Terminal			1.4		V
Gain Change with Temperature, Chroma Level Amplifier Stage	$T_A = 25^\circ\text{C}$ to $T_A = 70^\circ\text{C}$ Adjust Input Level at Chroma Input 2 for Output Level = 1.0 V RMS at Maximum Gain. Set Chroma Level Control Wiper for Output Level = 100 mV RMS		0.7		dB
Chroma Input 1 Resistance			2.4		k Ω
Chroma Input 1 Capacitance			6.2		pF
Chroma Input 2 Resistance			2.4		k Ω
Chroma Input 2 Capacitance			4.2		pF

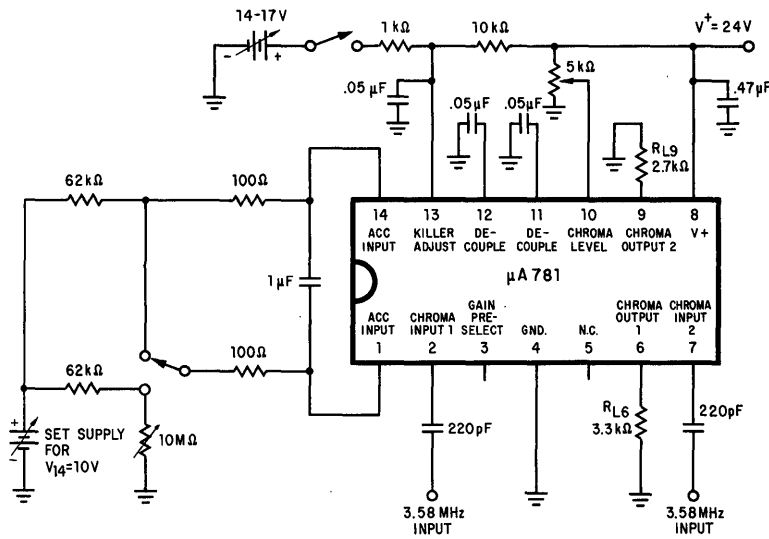
NOTE (1)

$T_A = 25^\circ\text{C}$, $V^+ = 24 \text{ V}$, $R_{L6} = 3.3 \text{ k}\Omega$, $R_{L9} = 2.7 \text{ k}\Omega$, Chroma Level Control Wiper at Ground, Voltage at ACC Input Terminals = 10 V, zero Differential Voltage between ACC Input Terminals, $f = 3.58 \text{ MHz}$, Peak-to-Peak Input at Chroma Input 1 = 200 mV, Peak-to-Peak Input at Chroma Input 2 = 400 mV, unless otherwise specified. Refer to Test Circuit 1.

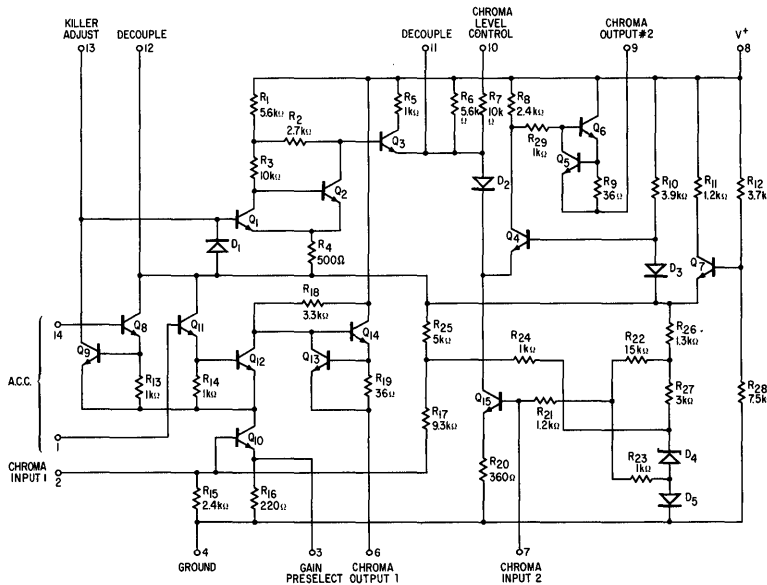
TYPICAL PERFORMANCE CURVES FOR 781C



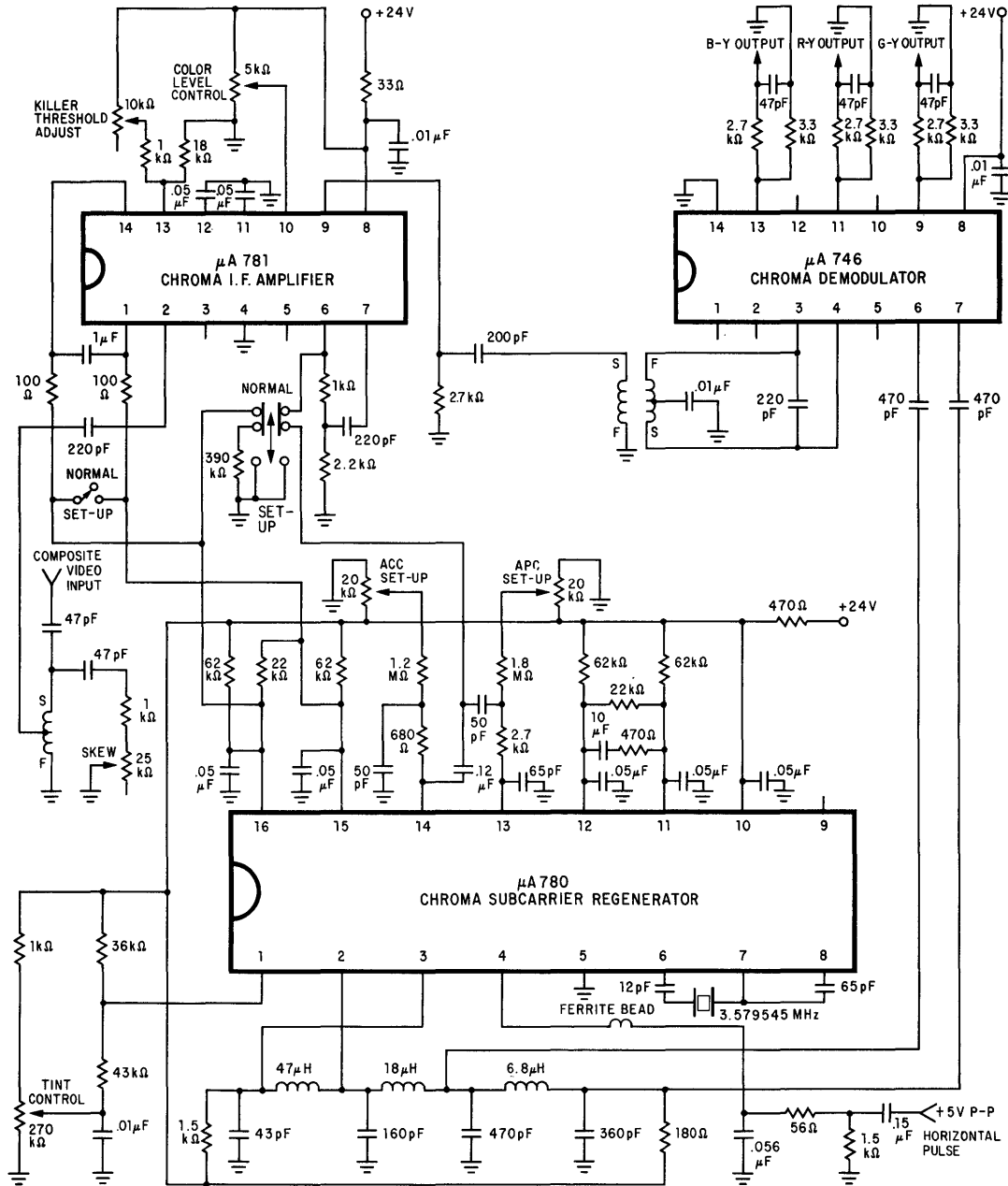
TEST CIRCUIT



EQUIVALENT CIRCUIT

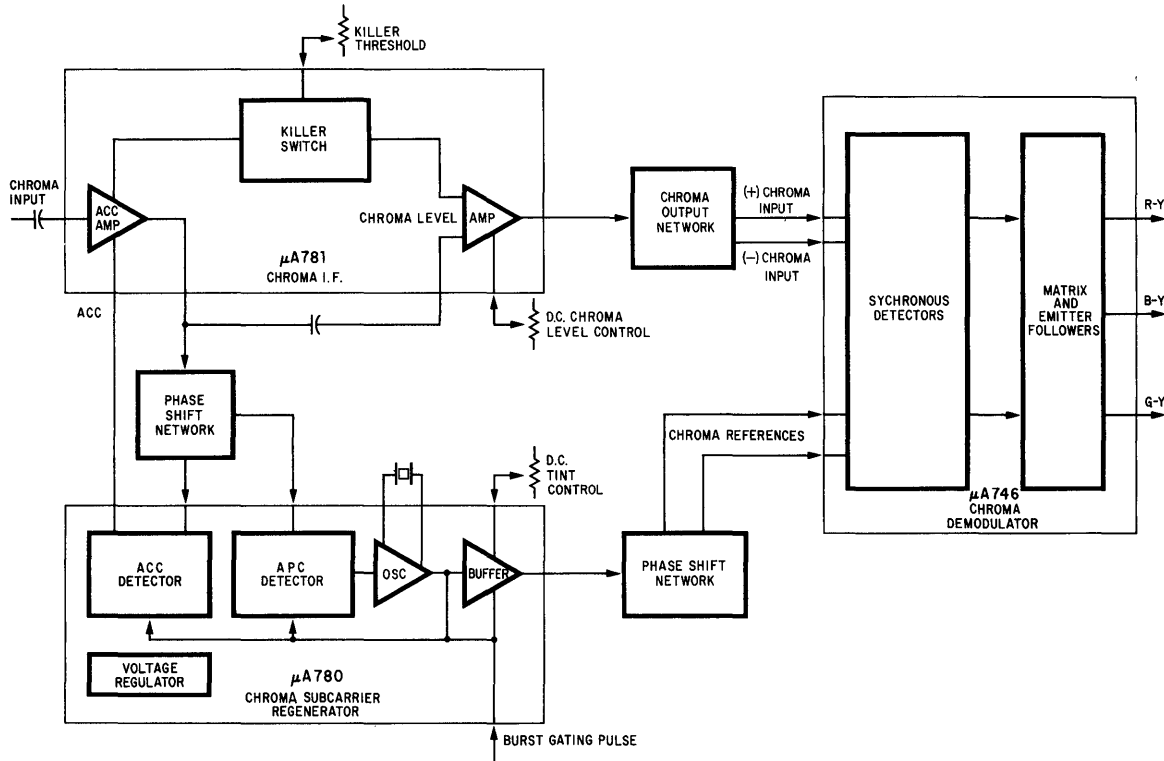


INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM

(BLOCK DIAGRAM)



μA786

PAL TV CHROMA DEMODULATOR

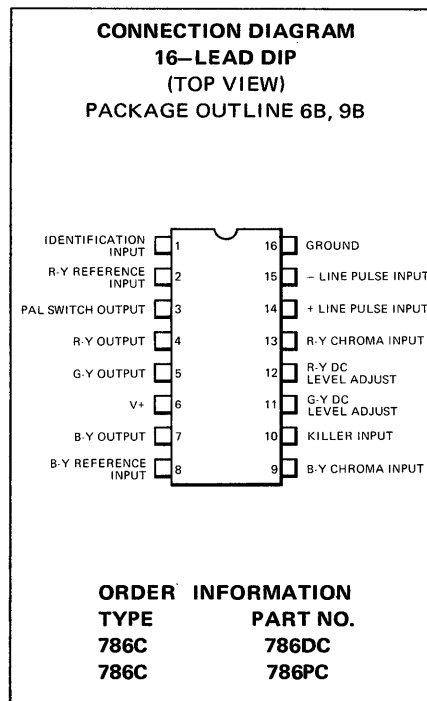
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA786 is a Synchronous Demodulator for direct drive of color video output stages. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The μA786 is designed for use in color television receivers operating on the Phase Alternate Line (PAL) system. The circuit consists of two synchronous demodulators, a decoding matrix, a PAL switch with internal multivibrator and a color killer switch.

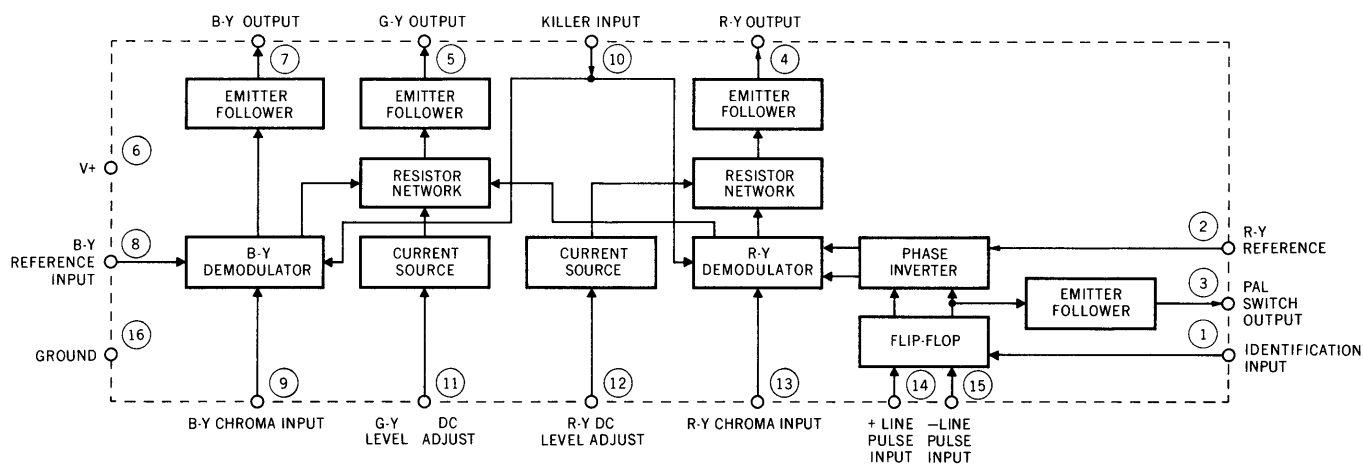
- **DOUBLE-BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **EMITTER FOLLOWER OUTPUTS**
- **INTERNAL PAL SWITCH**
- **INTERNAL COLOR KILLER**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	13.2 V
Internal Power Dissipation (Note 2)	730 mW
Color Difference Output Currents	5 mA
Voltage on Identification Input	±5 V
Current into Identification Input	5 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C



BLOCK DIAGRAM



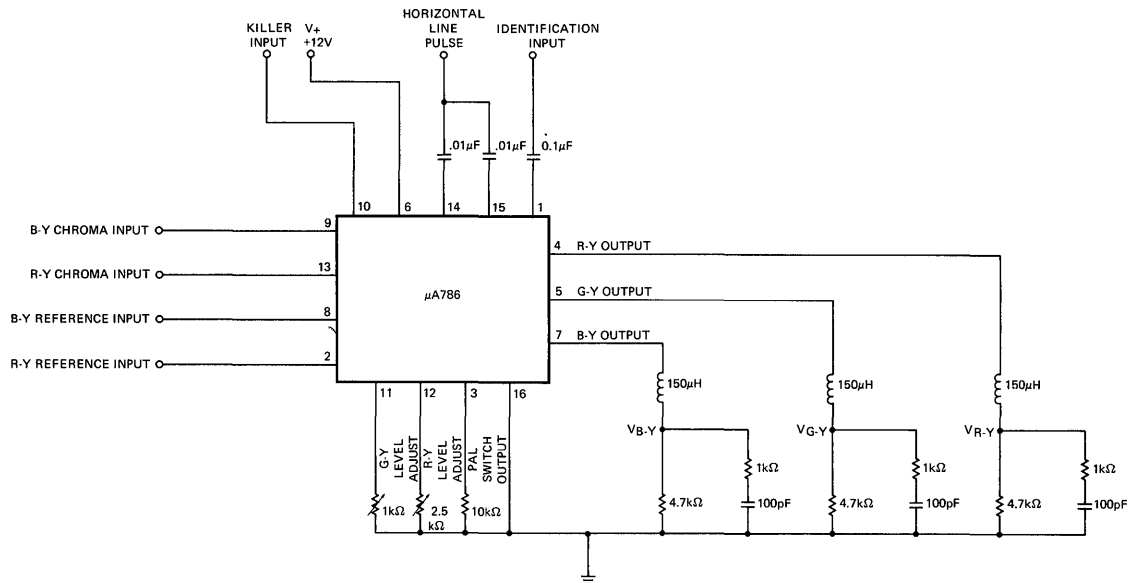
FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A786

786 C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_+ = 12\text{V}$, Test Circuit 1, unless otherwise specified. See Note 3)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (I_G)			33	40	mA
DC Voltage at B-Y Output	(Note 4)	6.8	7.4	7.8	V
Output Resistance at Color Difference Terminals (R_4, R_5, R_7)				100	Ω
Color Difference Gain					
R-Y Channel			7.0		V/V
B-Y Channel			12.5		V/V
G-Y Channel			(Note 5)		
Maximum Color Difference Output Voltage	(Note 6)				
R-Y Output (V_4)			3.2		Vp-p
B-Y Output (V_7)			4.0		Vp-p
G-Y Output (V_5)			1.8		Vp-p
Input Resistance of Chroma Inputs (R_9, R_{13})			1000		Ω
Input Capacitance of Chroma Inputs (C_9, C_{13})			10		pF
DC Voltage at Chroma Inputs (V_9, V_{13})			3.2		V
Input Resistance of Reference Inputs (R_2, R_8)			900		Ω
DC Voltage at Reference Inputs (V_2, V_8)			2.2		V
Color Killer Voltage Threshold (V_{10})				0.9	V
Color "ON"					V
Color "OFF"		0.3			V
Peak-To-Peak PAL Switch Output Voltage (V_3)		2.0	3.0		Vp-p

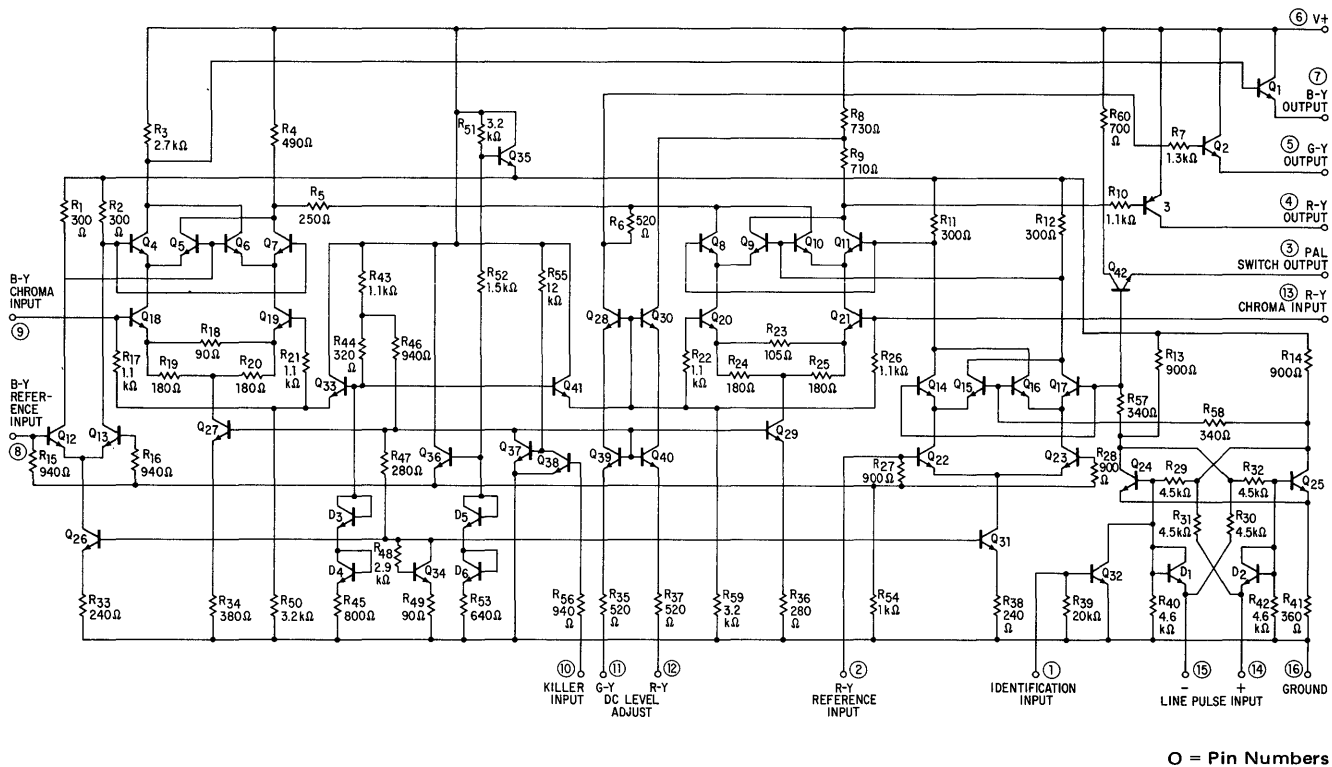
TEST CIRCUIT 1



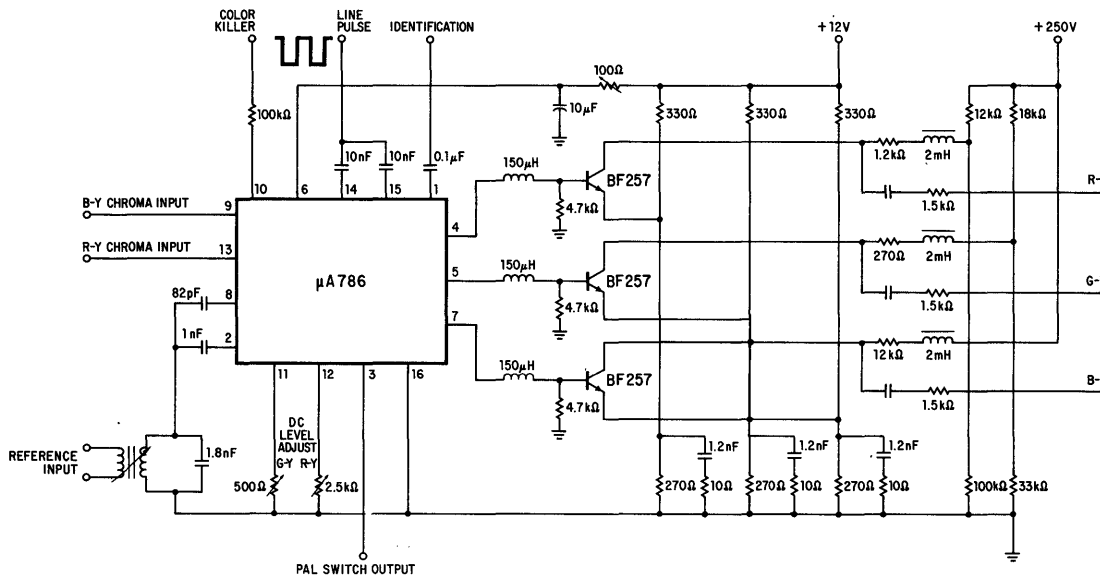
NOTES

- 16 volts is permissible during warmup.
- Rating applies for ambient temperatures to 70°C . Derate linearly at $9.1\text{ mW}/^\circ\text{C}$ above 70°C .
- Killer Voltage, $V_{10} = 0.9\text{ V}$; Reference Voltages V_2 and $V_8 = 1\text{ Vp-p}$ @ 4.4 MHz , V_2 leads by 90° ; Line Input Pulses, V_{14} and $V_{15} = -2.5\text{ V}$ peak; Chroma Input voltages V_9 and $V_{13} = 50\text{ mVp-p}$; Identification Input Voltage, $V_1 = 4\text{ Vp-p}$.
- DC Output Levels at R-Y and G-Y outputs are adjustable to B-Y level with a variable voltage ($V \leq 1.2\text{ V}$) or with variable resistors connected between pins 11 and 12 to ground. See typical application.
- G-Y Output is typically equal to $0.51\text{ (R-Y)} - 0.19\text{ (B-Y)}$.
- Gain Linearity is greater than 0.7.

EQUIVALENT CIRCUIT



TYPICAL APPLICATION – PAL COLOR TV SYSTEM



μA796

DOUBLE-BALANCED MODULATOR/DEMODULATOR

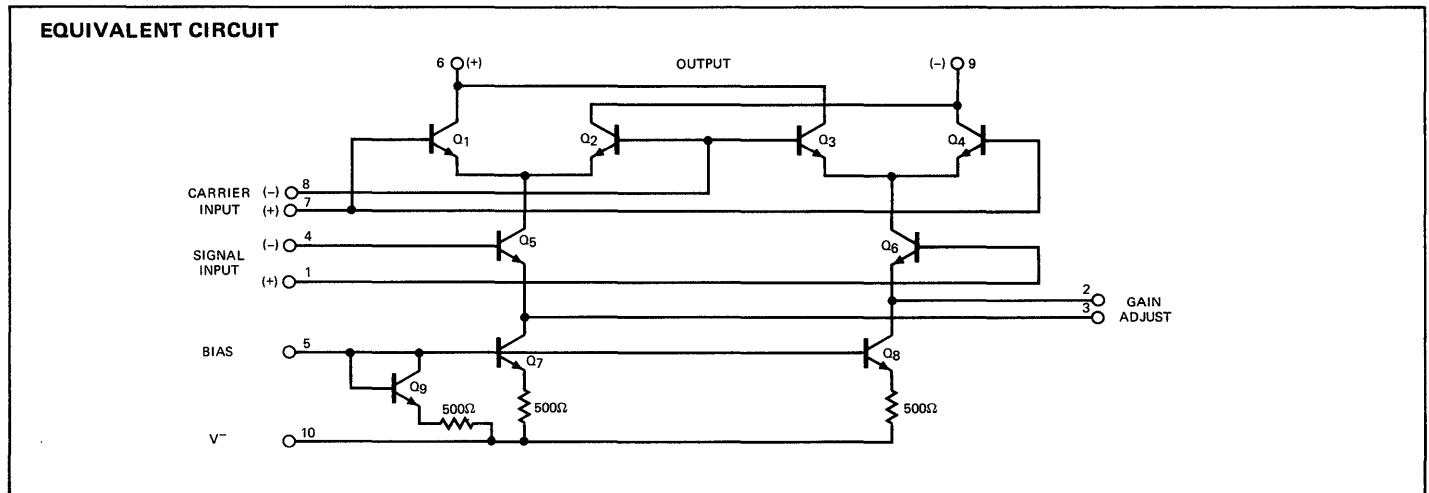
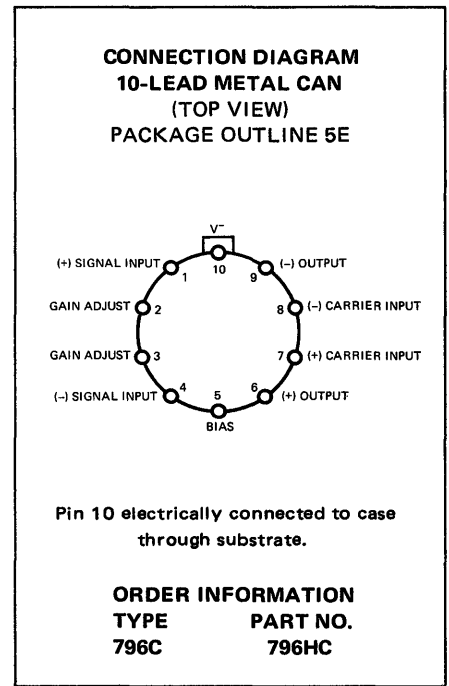
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA796 is a monolithic Double-Balanced Modulator/Demodulator using the Fairchild Planar* epitaxial process. This circuit produces an output voltage which is the product of an input voltage (signal) and a switching function (carrier). Communications applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Signal conditioning techniques possible include frequency doubling and halving, linear mixing and chopping, with additional uses as phase detectors in phase locked loops and as differentiators in NRZ and phase encoded digital tape and disk memories.

- EXCELLENT CARRIER SUPPRESSION
- LOW OFFSETS AND DRIFT
- FULLY BALANCED INPUTS AND OUTPUT
- USEFUL TO 100 MHz
- WIDE RANGE OF APPLICATION

ABSOLUTE MAXIMUM RATINGS

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30 V
Differential Input Signal ($V_7 - V_8$)	±5.0 V
Differential Input Signal ($V_4 - V_1$)	±(5 + $I_5 R_g$) V
Input Signal ($V_2 - V_1, V_3 - V_4$)	5.0 V
Bias Current (I_5)	12 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C



FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A796

796C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Figure 1 unless otherwise specified)

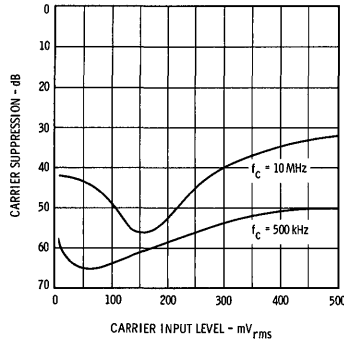
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Carrier Feedthrough	$V_C = 60\text{ mV (rms) sine wave}$ $f_C = 1.0\text{ kHz, offset adjusted}$		40		$\mu\text{V (rms)}$
	$V_C = 60\text{ mV (rms) sine wave}$ $f_C = 10\text{ MHz, offset adjusted}$		140		$\mu\text{V (rms)}$
	$V_C = 300\text{ mV}_{pp}\text{ square wave}$ $f_C = 1.0\text{ kHz, offset adjusted}$		0.04	0.2	mV (rms)
	$V_C = 300\text{ mV}_{pp}\text{ square wave}$ $f_C = 1.0\text{ kHz, offset not adjusted}$		20	150	mV (rms)
Carrier Suppression	$f_S = 10\text{ kHz, } 300\text{ mV (rms)}$ $f_C = 500\text{ kHz, } 60\text{ mV (rms) sine wave}$ offset adjusted	50	65		dB
	$f_S = 10\text{ kHz, } 300\text{ mV (rms)}$ $f_C = 10\text{ MHz, } 60\text{ mV (rms) sine wave}$ offset adjusted		50		dB
Transadmittance Bandwidth	$R_L = 50\Omega$ Carrier Input Port, $V_C = 60\text{ mV (rms) sine wave}$ $f_S = 1.0\text{ kHz, } 300\text{ mV (rms) sine wave}$		300		MHz
	Signal Input Port, $V_S = 300\text{ mV (rms) sine wave}$ $V_7 - V_8 = 0.5\text{ V dc}$		80		MHz
Voltage Gain, Signal Channel	$V_S = 100\text{ mV (rms), } f = 1.0\text{ kHz}$ $V_7 - V_8 = 0.5\text{ V dc}$	2.5	3.5		V/V
Input Resistance, Signal Port	$f = 5.0\text{ MHz}$ $V_7 - V_8 = 0.5\text{ V dc}$		200		$k\Omega$
Input Capacitance, Signal Port	$f = 5.0\text{ MHz}$ $V_7 - V_8 = 0.5\text{ V dc}$		2.0		pF
Single Ended Output Resistance	$f = 10\text{ MHz}$		40		$k\Omega$
Single Ended Output Capacitance	$f = 10\text{ MHz}$		5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	30	μA
	$(I_7 + I_8)/2$		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0	μA
	$(I_7 - I_8)$		0.7	5.0	μA
Average Temperature Coefficient of Input Offset Current	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		2.0		$\text{nA}/^\circ\text{C}$
Output Offset Current	$(I_6 - I_9)$		14	60	μA
Average Temperature Coefficient of Output Offset Current	$0^\circ\text{C} < T_A < +70^\circ\text{C}$		90		$\text{nA}/^\circ\text{C}$
Signal Port Common Mode Input Voltage Range	$f_S = 1.0\text{ kHz}$		5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8 = 0.5\text{ V dc}$		-85		dB
Common Mode Quiescent Output Voltage			8.0		Vdc
Differential Output Swing Capability			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0	mA
Power Dissipation			33		mW

NOTES

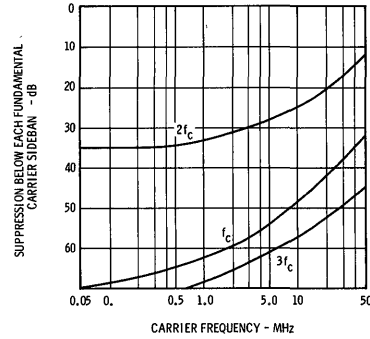
1. Rating applies to ambient temperatures up to 70°C . Above 70°C ambient derate linearly at $6.3\text{ mW}/^\circ\text{C}$.
2. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

TYPICAL PERFORMANCE CURVES FOR 796C

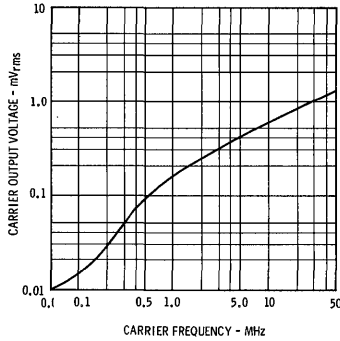
CARRIER SUPPRESSION AS A FUNCTION OF CARRIER INPUT LEVEL



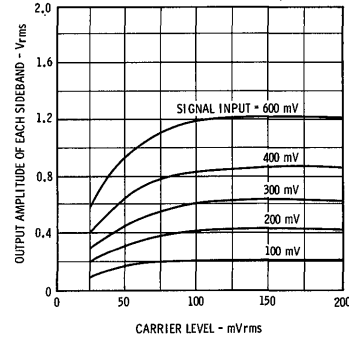
CARRIER SUPPRESSION AS A FUNCTION OF FREQUENCY



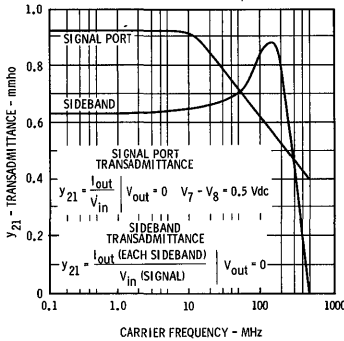
CARRIER FEEDTHROUGH AS A FUNCTION OF FREQUENCY



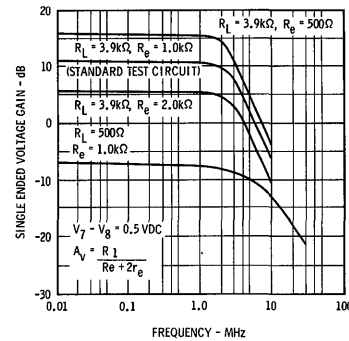
SIGNAL-PORT FREQUENCY RESPONSE



SIDEBAND OUTPUT AS A FUNCTION OF CARRIER LEVELS

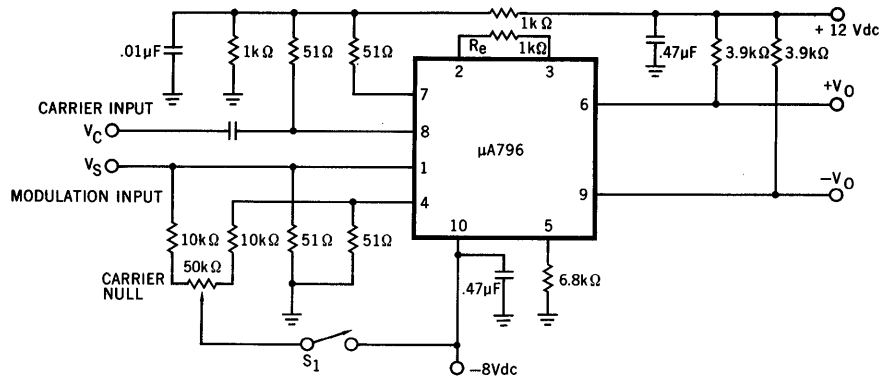


SIDEBAND AND SIGNAL PORT TRANSMITTANCES AS A FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

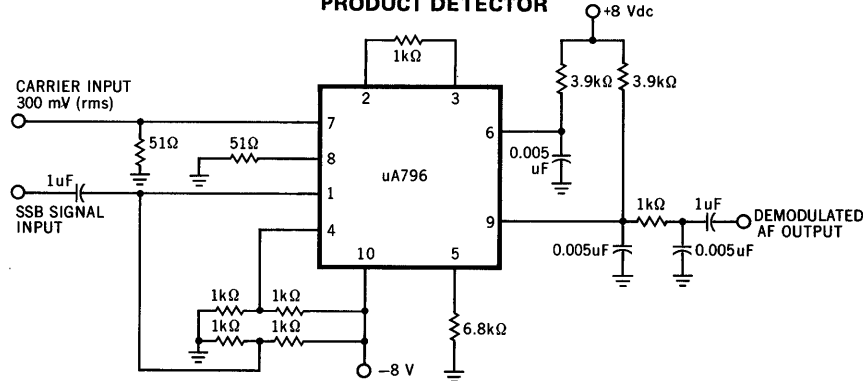
TYPICAL MODULATOR CIRCUIT



Note: S_1 is closed for "adjusted" measurements.

Fig. 1

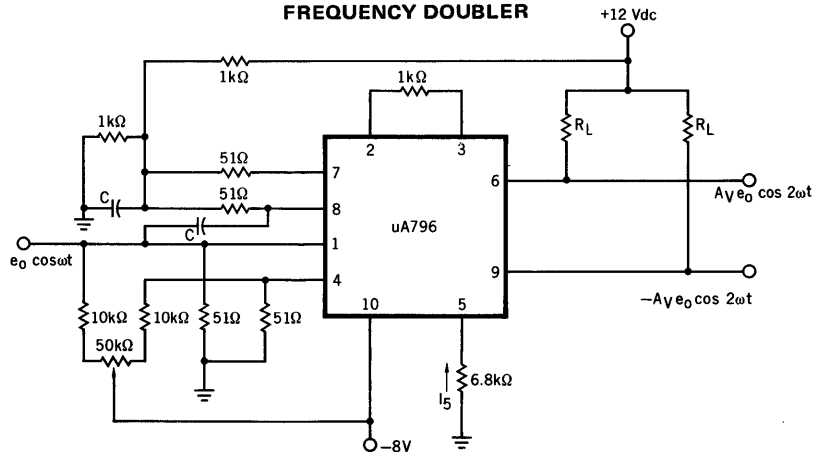
PRODUCT DETECTOR



This figure shows the $\mu A796$ used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mV(rms) is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mV(rms). All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

Fig. 2

FREQUENCY DOUBLER



The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

Fig. 3

3064

TV AUTOMATIC FINE-TUNING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3064 is a monolithic TV Automatic Fine-Tuning Circuit constructed using the Fairchild Planar* epitaxial process. The 3064 combines all of the automatic fine-tuning circuitry, except transformers, in one integrated circuit. Systems with low level IF amplifiers can now achieve tuning accuracies of ± 25 kHz due to the 3064's high sensitivity. Internal voltage regulation improves overall performance and reduces system cost.

- HIGH SENSITIVITY
- 25 kHz MAX. FREQUENCY DEVIATION
- INTERNAL VOLTAGE REGULATOR
- INTERNAL AGC

ABSOLUTE MAXIMUM RATINGS (Note 1)

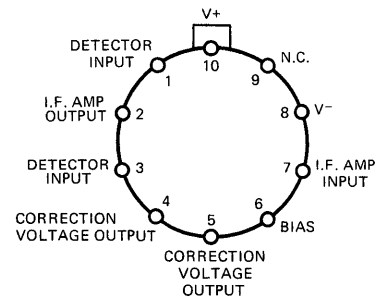
- Supply Voltage
- Internal Power Dissipation (Note 3)
- Detector Differential Voltage ($V_{1,3}$)
- Detector Input Voltage Range (V_1, V_3)
- I.F. Amp Output (V_2)
- Bias Voltage (V_6)
- Storage Temperature Range
- Operating Temperature Range
- Lead Temperature (Soldering, 60 seconds)

- Note 2**
 700 mW
 $\pm 10V$
 +5V, -6V
 +20V, 0V
 +2V, 0V
 $-65^\circ C$ to $+150^\circ C$
 $-40^\circ C$ to $+85^\circ C$
 300°C

NOTES:

- (1) All voltages referenced to V_- except as noted.
- (2) V_+ terminal may be connected to any positive voltage source through a suitable dropping resistor, provided the dissipation rating is not exceeded.
- (3) Derate linearly at 5.6 mW/°C for ambient temperatures above $+25^\circ C$.

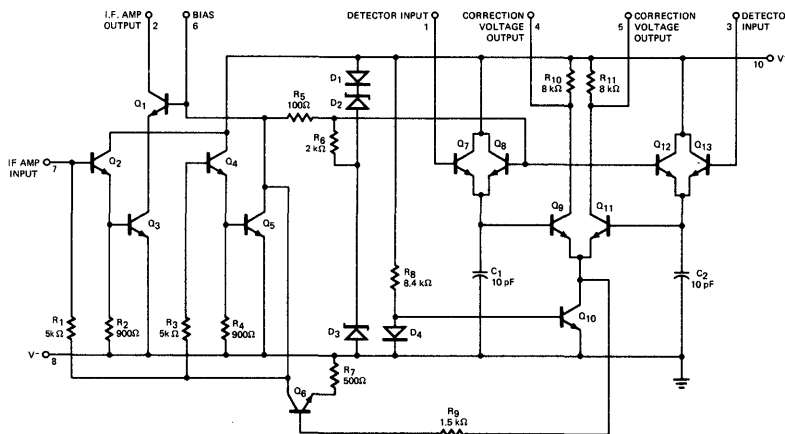
CONNECTION DIAGRAM
10-LEAD METAL CAN
 (TOP VIEW)
 PACKAGE OUTLINE 5E



ORDER INFORMATION

TYPE	PART NO.
3064	CA3064T

EQUIVALENT CIRCUIT



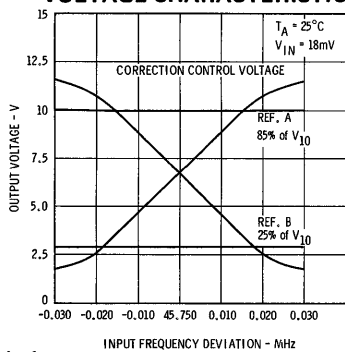
FAIRCHILD LINEAR INTEGRATED CIRCUITS • 3064

ELECTRICAL CHARACTERISTICS ($V_+ = +30V$, $R_S = 1.5\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, Test Circuit 1, unless otherwise specified.)

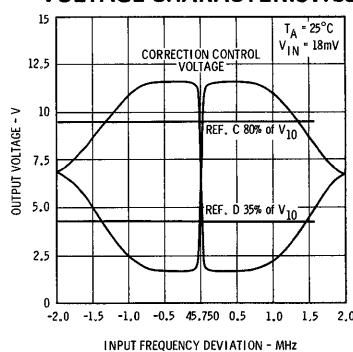
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Consumption	$T_A = +25^\circ\text{C}$	130	140	150	mW
	$T_A = -25^\circ\text{C}$		135	150	mW
	$T_A = +85^\circ\text{C}$		145	150	mW
Supply Current – I_+	$V_{10} = +10.5V$ Test Ckt 2	4.0	6.5	9.5	mA
Regulated Supply Voltage – V_+	Test Ckt 2	10.9	11.8	12.8	V
Quiescent Operating Current – I_2		1.0	2.0	4.0	mA
Quiescent Operating Voltages – V_4, V_5		5.0	6.9	8.0	V
Output Offset Voltage – ($V_4 - V_5$)		-1.0	0	1.0	V
Input Admittance – Y_{11}	$f = 45.75\text{ MHz}$		$0.41 + j\ 1.0$		mmho
Reverse Transfer Admittance – Y_{12}	$f = 45.75\text{ MHz}$		$0 + j\ 3.4$		μmho
Forward Transfer Admittance – Y_{21}	$f = 45.75\text{ MHz}$		$24.5 - j\ 29$		mmho
Output Admittance – Y_{22}	$f = 45.75\text{ MHz}$		$0.04 + j\ 0.9$		mmho
Correction Control Voltage – V_4 (Test Circuit 1)	$V_{IN} = 18\text{ mV RMS}$ $f_o = 45.750\text{ MHz}$ Δf as listed (MHz)				
	-0.030	85			% V_+
	+0.030			25	% V_+
	-0.900	80			% V_+
	+0.900			35	% V_+
	-1.500			80	% V_+
Correction Control Voltage – V_5 (Test Circuit 1)	$V_{IN} = 18\text{ mV RMS}$ $f_o = 45.750\text{ MHz}$ Δf as listed (MHz)				
	-0.030			25	% V_+
	+0.030	85			% V_+
	-0.900			35	% V_+
	+0.900	80			% V_+
	-1.500	35			% V_+
	+1.500			80	% V_+

TYPICAL PERFORMANCE CURVES FOR 3064

NARROW-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

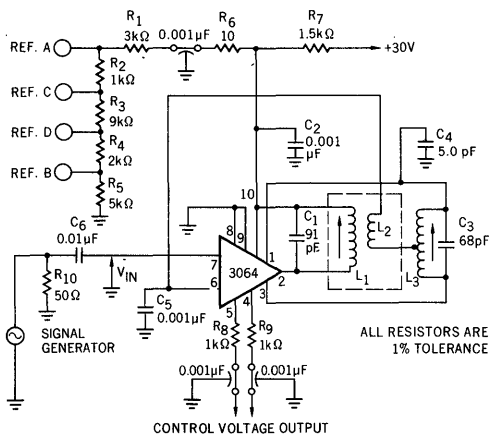


WIDE-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS



NOTE: See test circuit 1.

**TEST CIRCUIT 1
CORRECTION VOLTAGES**



NOTE: Parts placement is critical. Use P.C. board layout on last page for best results.

L_1 is aligned for symmetrical bandwidth on either side of 45.750 MHz.
 L_2 tertiary winding wound on L_1 coil form.
 L_3 is aligned for zero differential output between terminals 4 and 5 at $f_o = 45.750$ MHz.

REFERENCE VOLTAGE PERCENTAGES

Ref. A	85% of V_{10}
Ref. B	25% of V_{10}
Ref. C	80% of V_{10}
Ref. D	35% of V_{10}

COIL DATA FOR DISCRIMINATOR WINDINGS

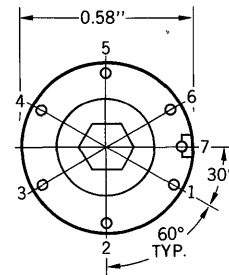
L_1 – Discriminator Primary: 3 1/16 turns; #20, Enamel-covered wire—close-wound, at bottom of coil form. Inductance of $L_1 = 0.165 \mu\text{H}$; $Q_o = 120$ at $f_o = 45.75$ MHz. Start winding at Terminal #6; finish at Terminal #1. See Notes below.

L_2 – Tertiary Windings: 2 1/16 turns; #20 Enamel-covered wire—close wound over bottom end of L_1 . Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 – Discriminator Secondary: 3 1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of $L_3 = 0.180 \mu\text{H}$; $Q_o = 150$ at $f_o = 45.75$ MHz. Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

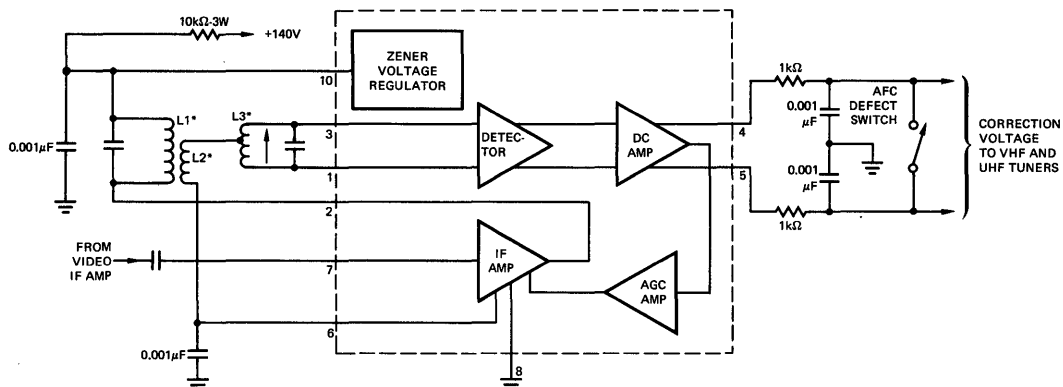
- NOTES:**
1. Coil Forms; Cylindrical; 0.30" Dia. max.
 2. Tuning Core: 0.250" Dia. x 0.37" Length.
: Material: Carbinol J or equivalent.
 3. Coil Form Base: See drawing below.
 4. End of coil nearest terminal board to be designated the winding start end.

COIL FORM BASE TERMINAL DIAGRAM

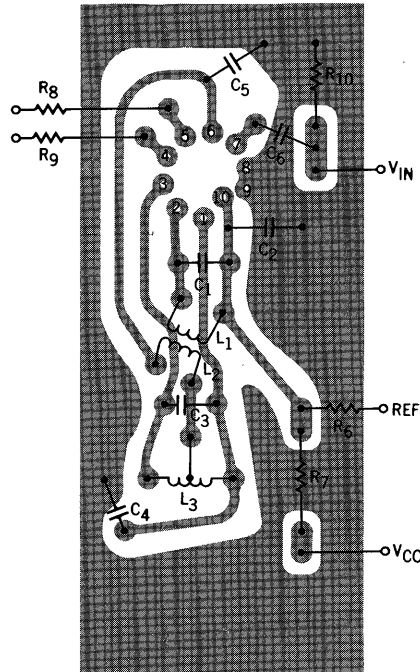


Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

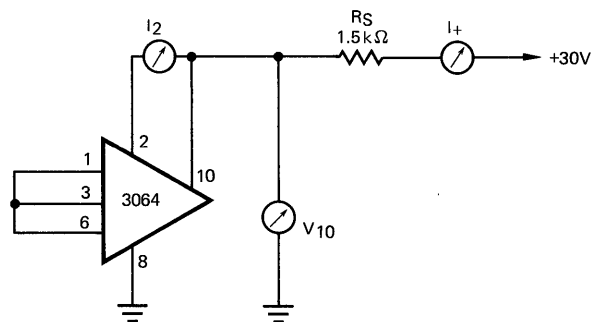
BLOCK DIAGRAM



**PRINTED CIRCUIT BOARD FOR CORRECTION
VOLTAGE TEST CIRCUIT
(Full Size Bottom View)**



**TEST CIRCUIT 2
Regulated Voltage, Total Supply Current and
Quiescent Current at Terminal 2**



3065

TV SOUND SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3065 is a monolithic TV Sound System constructed using the Fairchild Planar* epitaxial process. It contains a multi-stage limiting IF amplifier, dc gain (volume) control, FM detector and an audio driver. Excellent sensitivity, high AM rejection and an internally regulated supply, coupled with low external component requirements make the 3065 ideally suited for TV sound channels.

- DC VOLUME CONTROL ELIMINATES NEED FOR SHIELDED CABLES
- EXCELLENT AM REJECTION — 50 dB TYPICAL AT 4.5 MHz
- DIFFERENTIAL PEAK DETECTOR REQUIRES ONLY ONE SINGLE-TUNED COIL
- INTERNAL ZENER DIODE REGULATED SUPPLY
- LOW HARMONIC DISTORTION

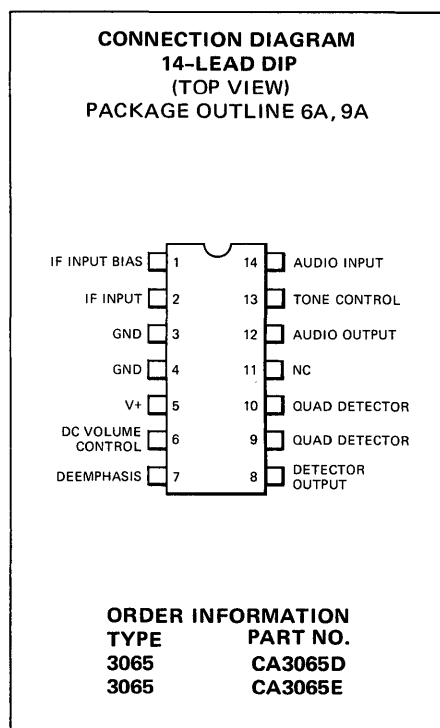
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Internal Power Dissipation (Note 2)	670 mW
Power Supply Current	50 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds) CA3064D	300°C
Molded DIP (Soldering, 10 seconds) CA3065E	260°C

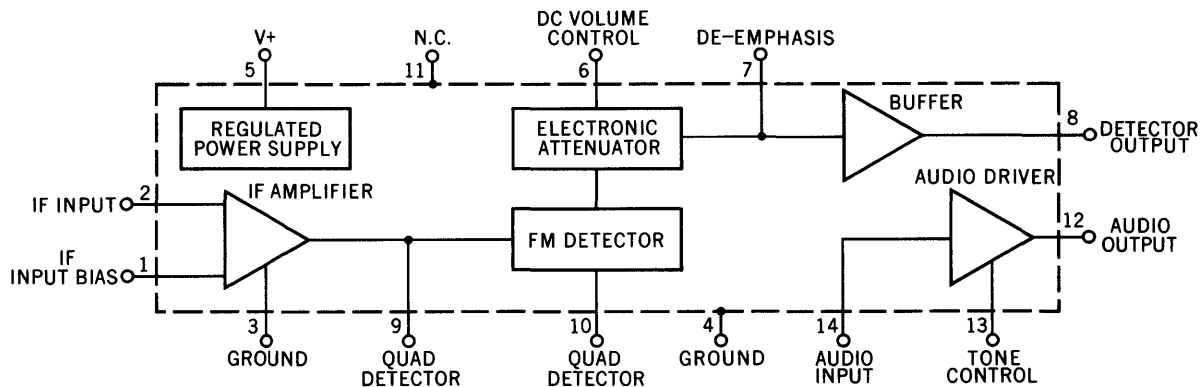
Note 1
670 mW
50 mA
-40°C to +85°C
-55°C to +125°C

NOTES

1. V₊ terminal may be connected to any positive voltage through a suitable dropping resistor, provided the dissipation rating is not exceeded.
2. Rating applies to ambient temperature up to 70°C. Derate linearly at 8.3 mW/°C above 70°C.



BLOCK DIAGRAM



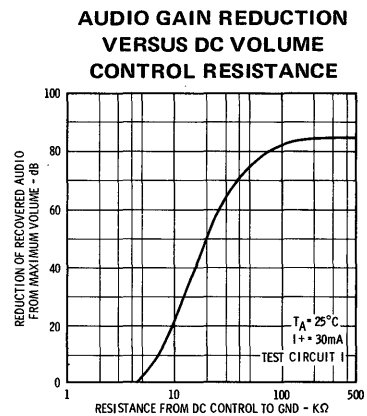
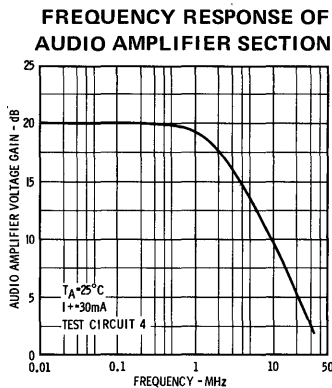
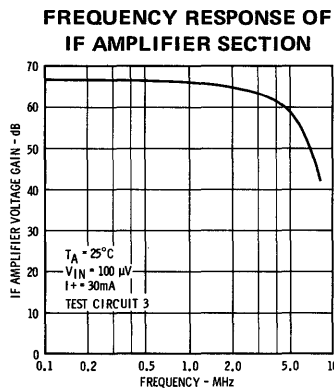
FAIRCHILD LINEAR INTEGRATED CIRCUITS • 3065

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $I_+ = 30\text{ mA}$ unless otherwise specified)

PARAMETER	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Zener Regulating Voltage (V_5)			10.3	11.2	12.2	V
Supply Current (I_5)	$V_+ = 9.0\text{V}$		10	16	24	mA
Internal Power Dissipation	$I_+ = 33\text{ mA}$		343	370	400	mW
Voltage at IF Input Bias (V_1)				2.0		V
Voltage at DC Volume Control (V_6)				4.8		V
Voltage at De-emphasis (V_7)				6.1		V
Voltage at Quad Detector (V_9)				3.7		V
Voltage at Audio Output (V_{12})			4.0	5.1	5.8	V
AC CHARACTERISTICS						
IF AMPLIFIER						
Input Limiting Voltage at -3 dB point	$f = 4.5\text{ MHz}$	1		200	400	μV
AM Rejection	$f_o = 4.5\text{ MHz}$, FM $\pm 25\text{ kHz}$ at 400 Hz, $V_{IN} = 100\ \mu\text{V}$ AM = 30% at 1 kHz	1	40	50		dB
IF Transconductance Magnitude	$f = 4.5\text{ MHz}$			500		mmho
Phase Angle				45		degrees
Feedback Capacitance	$f = 1.0\text{ MHz}$, Pin 2 to Pin 9			<0.02		pF
Input Impedance Components	$f = 4.5\text{ MHz}$, Pin 1 to Pin 2					
Parallel Input Resistance				17		k Ω
Parallel Input Capacitance				4.0		pF
Output Impedance Components	$f = 4.5\text{ MHz}$, Pin 9 to Ground					
Parallel Output Resistance				3.25		k Ω
Parallel Output Capacitance				75		pF
DETECTOR						
Recovered AF Voltage	($f_o = 4.5\text{ MHz}$, FM $\pm 25\text{ kHz}$ at 400 Hz, $V_{IN} = 100\text{ mV}$)	1	0.5	0.75		V _{rms}
Total Harmonic Distortion		1		0.9	2.0	%
Output Resistance						
De emphasis Output				7.5		k Ω
Detector Output				300		Ω
ATTENUATOR						
Max. Attenuation	$R_x = \infty$	1	60	80		dB
Max. Play-through Voltage*	$R_x = \infty$	1		0.075	1.0	mV
AUDIO AMPLIFIER						
Voltage Gain	$V_{14} = 0.1\text{ V}_{rms}$, $f = 400\text{ Hz}$	2	17.5	20		dB
Total Harmonic Distortion	$V_{12} = 2\text{ V}_{rms}$, $f = 400\text{ Hz}$	2		1.5		%
Undistorted Output Voltage	THD = 5%, $f = 400\text{ Hz}$	2	2.0	2.5		V _{rms}
Input Resistance	$f = 400\text{ Hz}$			70		k Ω
Output Resistance	$f = 400\text{ Hz}$			270		Ω

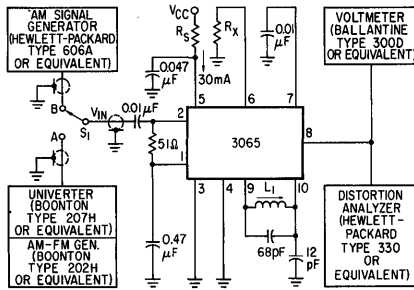
* Play-through voltage is the unwanted signal, measured at the detected output (Pin 8), when the volume control is set for minimum output.

TYPICAL PERFORMANCE CURVES FOR 3065



TEST CIRCUITS

INPUT LIMITING VOLTAGE, AM REJECTION, RECOVERED AUDIO, TOTAL HARMONIC DISTORTION, MAXIMUM ATTENUATION, MAXIMUM "PLAY-THROUGH" TEST CIRCUIT.

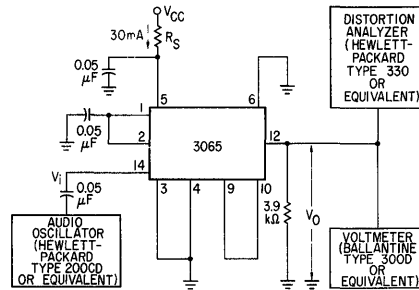


PINS 11, 12, 13, 14 NO CONNECTION

* $L_1 = 16\mu\text{H}$ NOMINAL
 $Q(\text{UNLOADED}) = 50$

TEST CIRCUIT 1

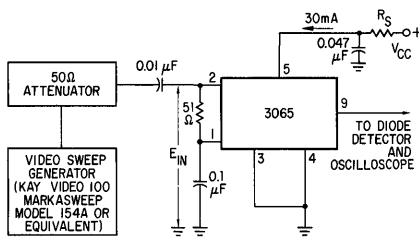
AUDIO VOLTAGE GAIN (UNDISTORTED OUTPUT)



PINS 7, 8, 11, 13 NO CONNECTION

TEST CIRCUIT 2

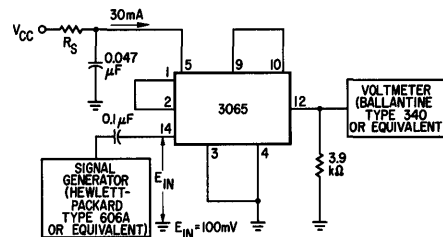
IF AMPLIFIER SECTION



$E_{IN} = 100\mu\text{Vrms}$

TEST CIRCUIT 3

AUDIO AMPLIFIER SECTION

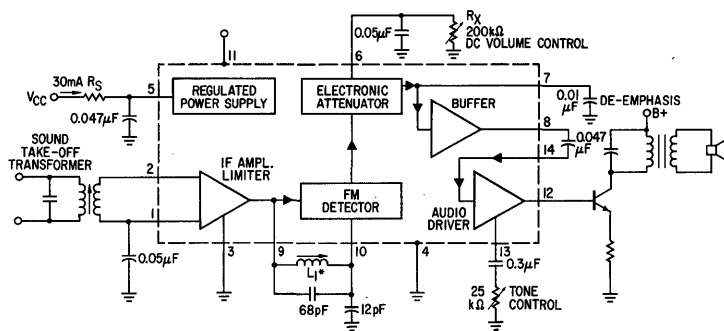


$E_{IN} = 100\text{ mV}$

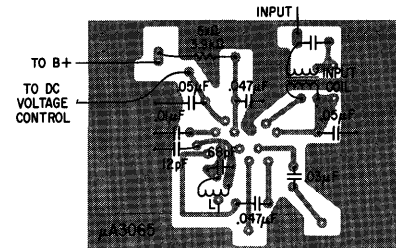
TEST CIRCUIT 4

TYPICAL APPLICATION

TV SOUND SYSTEM



SUGGESTED CIRCUIT LAYOUT COMPONENT SIDE



* $L_1 = 16\mu\text{H}$ NOMINAL, $Q(\text{UNLOADED}) = 50$

3066

TV CHROMA PROCESSOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3066 is a monolithic integrated circuit using the Fairchild Planar* epitaxial process. It provides complete chroma processing except for tint control and demodulation.

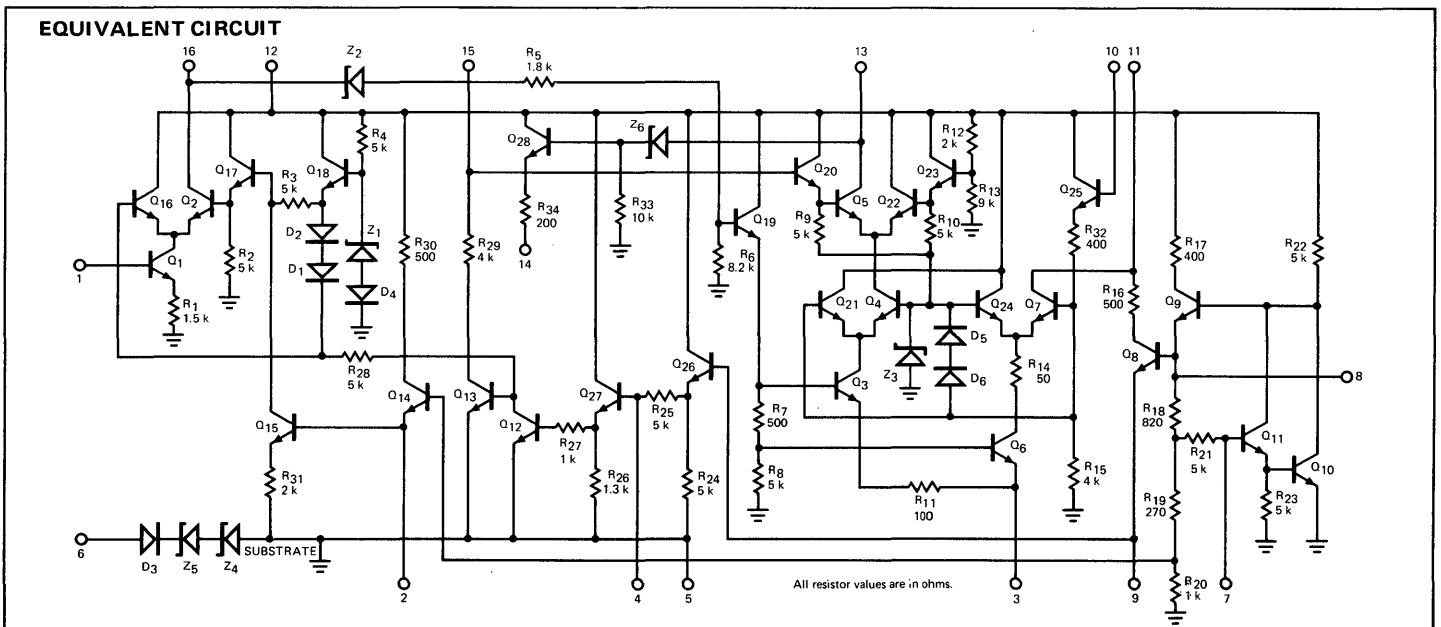
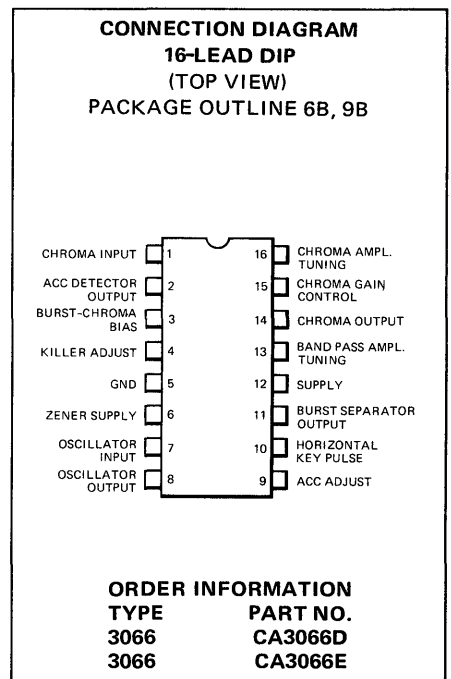
- BLANKED CHROMA AMPLIFIER
- CHROMA BAND PASS AMPLIFIER
- DC CHROMA CONTROL
- COLOR KILLER
- ACC DETECTOR
- CHROMA SUBCARRIER REGENERATION

ABSOLUTE MAXIMUM RATINGS

Supply Current and Voltages (see chart)
 Internal Power Dissipation (Note 1)
 Operating Temperature Range
 Storage Temperature
 Lead Temperature

730 mW
 -40°C to +85°C
 -55°C to +125°C
 300°C
 260°C

Hermetic DIP (Soldering, 60 seconds) CA3066D
 Molded DIP (Soldering, 10 seconds) CA3066E



Notes on following page.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • 3066

MAXIMUM RATINGS

(with respect to Terminal No. 5)

SYMBOL	TERMINAL NO.	MIN.	MAX.	UNITS
I_{IN} (Note 2)	6		20	mA
Voltage	10	-5.0	Note 3	V
Voltage	11	0.0	18	V
Voltage	12	0.0	12	V
Voltage	15	0.0	Note 3	V
Voltage	16	0.0	15	V
Voltage	1	-5.0	5.0	V

- NOTES 1. Rating applies to ambient temperature up to 70°C. Above 70°C derate linearly at 6.67 mW/°C.
 2. Terminal No. 6 is internally connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 6.
 3. The upper voltage limit cannot exceed the power supply input voltage at pin 12.

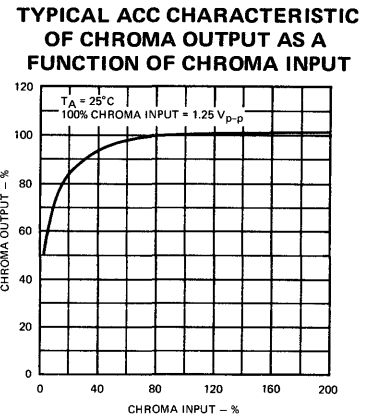
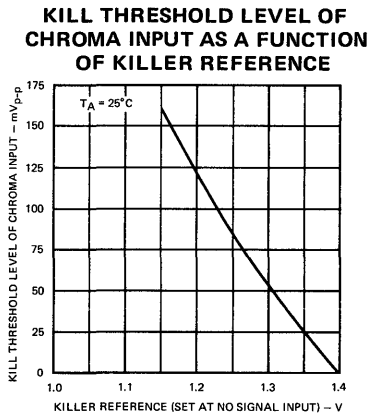
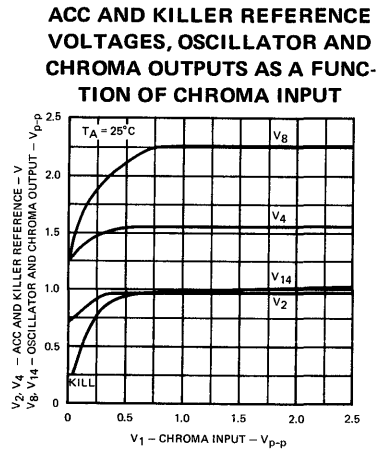
ELECTRICAL CHARACTERISTICS ($V_{12} = 11.2$ V, $T_A = 25^\circ$ C, Test Circuit Figure 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
DC CHARACTERISTICS					
ACC Reference	V_2		0.5		V
Burst-Chroma Amp Bias Current Term	V_3		2.9		V
Killer Reference	V_4		1.0		V
Zener Regulator Reference	V_6	10.6	11.9	12.6	V
Oscillator Input	V_7		1.4		V
Oscillator Output	V_8		2.35		V
Balance ACC Control	V_9		1.65		V
Chroma Output	V_{14}		4.6		V
Supply Current	I_5	14	24	33	mA
Burst Separator Output (S_1 Closed)	I_{11}		6.5		mA
Band-Pass Amp. Output	I_{13}		4.8		mA
Chroma Amp Output	I_{16}		1.27		mA

AC CHARACTERISTICS (Test Circuit Figure 2)

Oscillator Output	$V_1 = 0$	V_8	0.7	1.2		V_{p-p}
	$V_1 = 1.25 V_{p-p}$			2.5	3.5	V_{p-p}
Chroma Output	100%: $V_1 = 1.25 V_{p-p}$	V_{14}	0.5	1.0		V_{p-p}
	Killed: $V_1 = 0.025$ V				60	mV _{p-p}
ACC Detector Output	$V_1 = 1.25 V_{p-p}$	V_2		0.9		V
Small Signal Input Resistance Pin 1		R_i		50		Ω
Small Signal Input Capacitance Pin 1		C_i		2.4		pF
Small Signal Output Resistance Pin 14		R_o		250		Ω

TYPICAL PERFORMANCE CURVES



DC TEST CIRCUIT

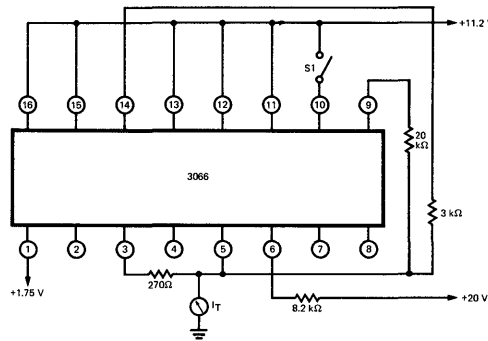
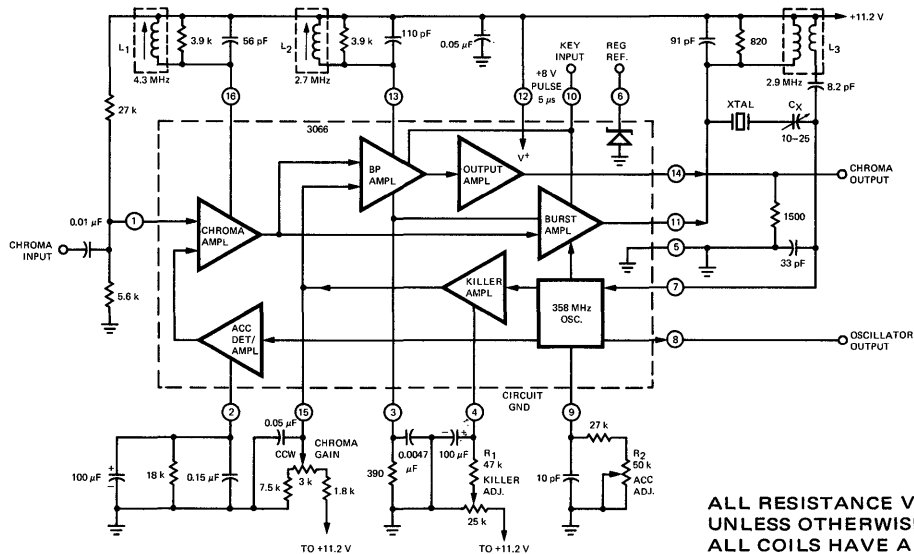


Fig. 1

AC TEST CIRCUIT



ALL RESISTANCE VALUES ARE IN OHMS UNLESS OTHERWISE INDICATED. ALL COILS HAVE A Q ≥ 30.

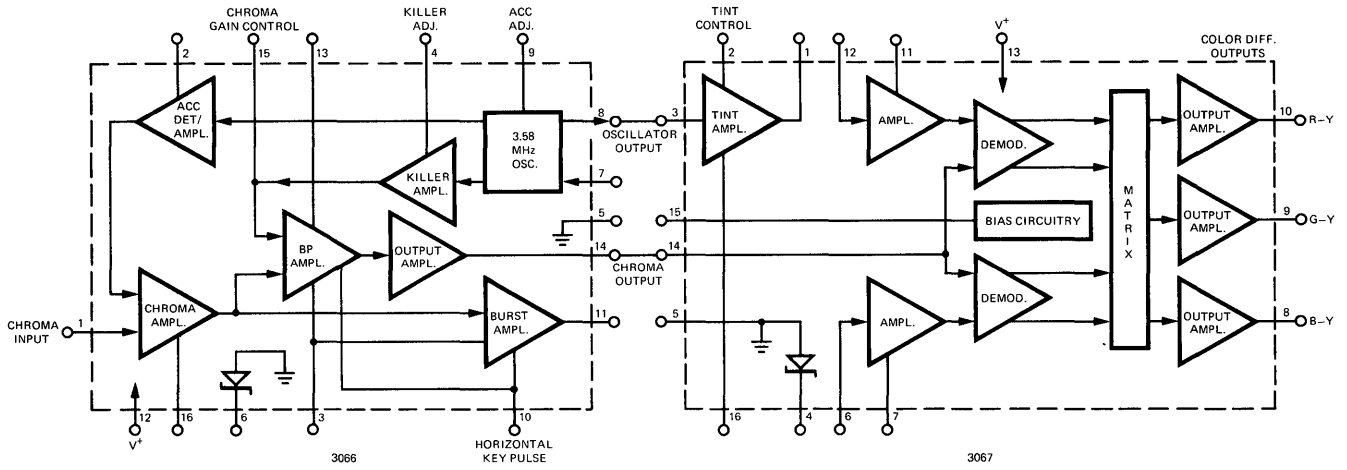
DYNAMIC TEST PROCEDURE

Steps 1, 2, and 3 are performed with no Chroma input ($V_1 = 0$).

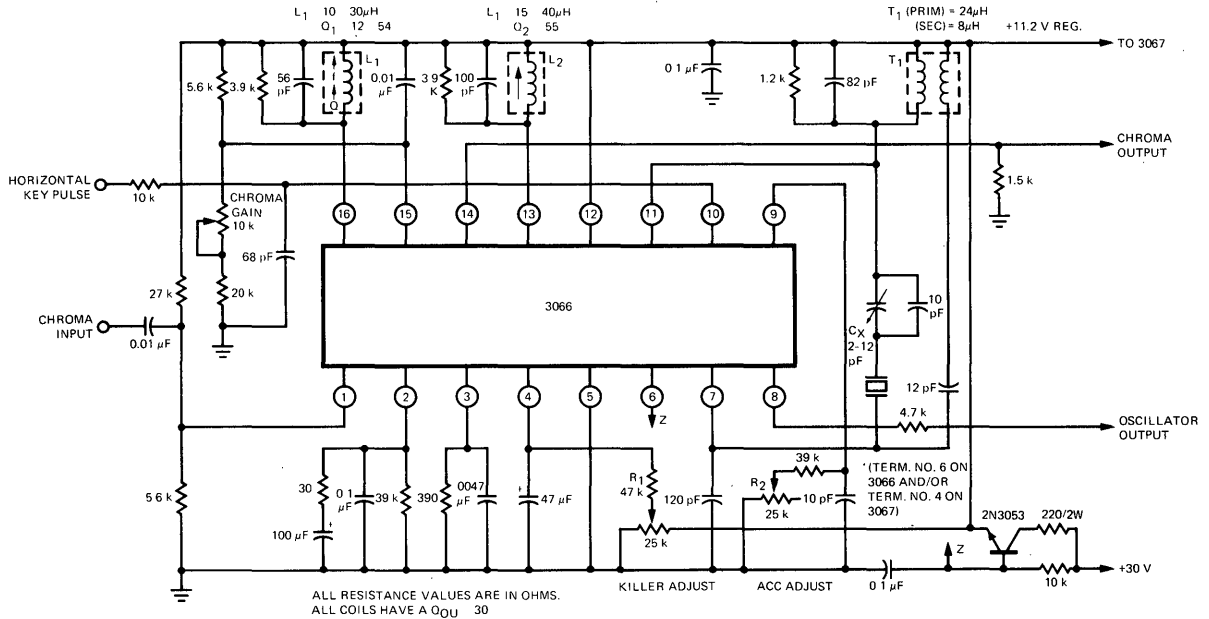
1. Adjust ACC potentiometer for $V_2 = +0.65$ V.
2. Adjust Killer Potentiometer for $V_4 = +1.2$ V.
3. Adjust capacitor C_X (crystal trimmer) so that frequency of oscillator is 3.579545 MHz.
4. Unless otherwise noted, the chroma gain control is at maximum gain (fully clockwise).
5. The chroma input test signal is a 52.5 μ s "line" at subcarrier frequency, and 10 cycles of burst at 46.5% of the "line" amplitude. The chroma input (V_1) is in peak-to-peak volts of "line" amplitude.
6. The chroma output (V_{14}) is the same as the chroma input (V_1) except that the burst is removed and keying overshoot occurs in the retrace period. The chroma output is in peak-to-peak volts of "line" amplitude.
7. The oscillator output (V_8) is the CW output at terminal No. 8 and is in peak-to-peak volts.

Fig. 2

COMPLETE CHROMA PROCESSING SYSTEM
3066/3067



TYPICAL APPLICATION



*NOTE: If the 3066 or 3067 are to be separately removed from the circuit, the Zeners should be paralleled to avoid excessive voltage on the remaining unit.

3067

CHROMA DEMODULATOR

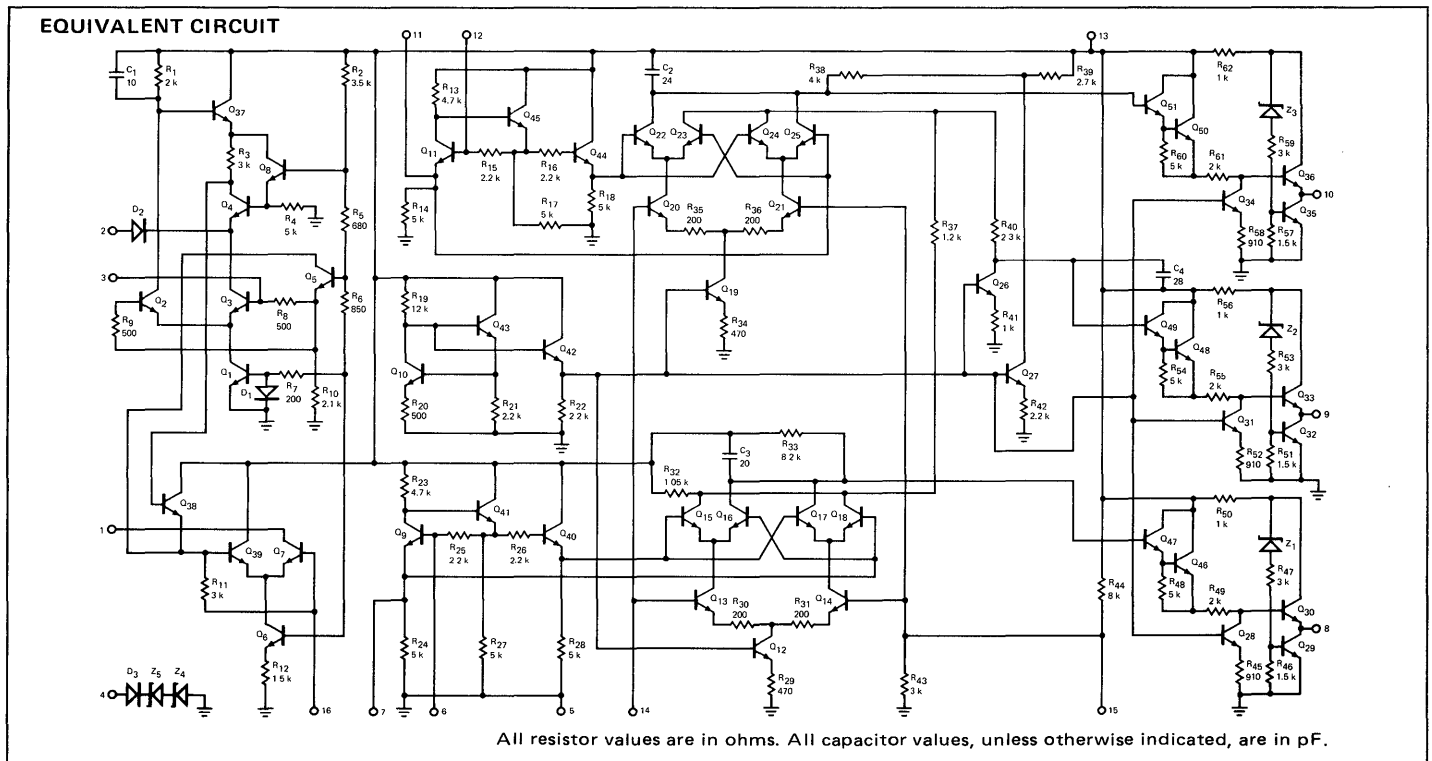
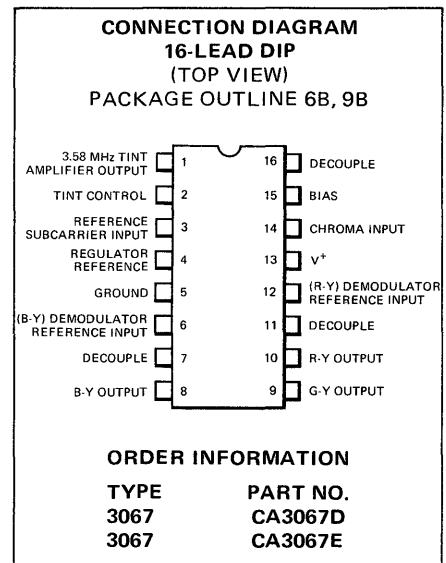
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3067 is a monolithic integrated circuit for TV chroma demodulation. This device demodulates the chroma information contained in the color video signal and provides the color difference output signals. The device also incorporates a dc tint control and an internal R-C filter for eliminating high frequency components in the output signals.

- BALANCED CHROMA DEMODULATORS
- DC TINT CONTROL
- COLOR DIFFERENCE MATRIX
- INTERNAL RF FILTERING
- REFERENCE SUBCARRIER LIMITER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	12 V
Tint Amplifier Output Voltage	15 V
Internal Power Dissipation (Note 1)	730 mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds) CA3067D	300°C
Molded DIP (Soldering, 10 seconds) CA3067E	260°C
Current into Regulator Reference Terminal	20 mA



Notes on following pages.

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 3067

ELECTRICAL CHARACTERISTICS – $T_A = 25^\circ\text{C}$ and $V^+ = 11.2\text{ V}$

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
DC CHARACTERISTICS						
Voltages						
Tint Control Input	V_2	$I_2 = 0.25\text{ mA}$		3.5		V
Reference Subcarrier	V_3			2.1		
Regulator Reference	V_4		10.6	11.9	12.6	
B-Y, R-Y Oscillator Reference Inputs	V_6, V_{12}			5.7		
Balance (B-Y, R-Y)	V_7, V_{11}			5.0		
B-Y, G-Y, R-Y Outputs	V_8, V_9, V_{10}		4.2	5.0	5.8	
Difference Outputs (Note 2)	$\Delta V_8, \Delta V_9, \Delta V_{10}$		-0.3		0.3	
Chroma Inputs	V_{14}, V_{15}			3.0		
Tint Amplifier Balance	V_{16}			4.7		
Currents						
Tint Amplifier Output (min)	$I_{1(\text{min})}$	$V_{16} = 8\text{ V}$	0.16	0.37		mA
Total Supply	$I_1 + I_{13}$		15	24	33	
AC CHARACTERISTICS						
Tint Amplifier Output						
Sensitivity	V_1	$V_3 = 7\text{ mVRMS}$	160	250		mVRMS
Limiting Knee		$V_3 = 35\text{ mVRMS}$		300		
Limiting		$V_3 = 350\text{ mVRMS}$			380	
Tint Amplifier Phase Reference (Note 3)	ϕ_6	$V_3 = 70\text{ mVRMS}$	185	220	235	Degree
Tint Amplifier Phase Shift (Note 4)	$\Delta\phi_6$	$V_3 = 70\text{ mVRMS}$	90	105		Degree
Demodulated Chroma Output						
R-Y	V_{10}	$V_3 = 70\text{ mVRMS}$ $V_{14} = 35\text{ mVRMS}$	150	250		VRMS
Ratio of G-Y to R-Y	V_9/V_{10}		0.28	0.36	0.44	
Ratio of B-y to R-Y	V_8/V_{10}		1.0	1.2	1.4	
Color Difference Output (3 dB Bandwidth)	BW		450	550		kHz
Color Difference Outputs (maximum input signals)						
R-Y	V_{10}	$V_3 = 70\text{ mVRMS}$ $V_{14} = 212\text{ mVRMS}$		3.0		V_{p-p}
G-Y	V_9			1.1		
B-Y	V_8			3.6		
Small Signal Input Resistance						
Terminal No. 3	r_i			550		Ω
Terminal Nos. 6 and 12				2,200		
Small Signal Output Resistance						
Terminal Nos. 8, 9 and 10	r_o			5		

NOTES

1. Rating applies to ambient temperature of 70°C . From 70°C to 85°C derate linearly at $8.3\text{ mW}/^\circ\text{C}$.

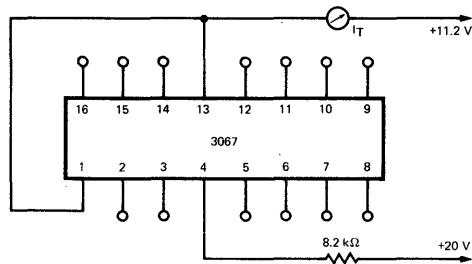
$$2. \Delta V_8 = V_8 - \frac{V_8 + V_9 + V_{10}}{3} \quad \Delta V_9 = V_9 - \frac{V_8 + V_9 + V_{10}}{3} \quad \Delta V_{10} = V_{10} - \frac{V_8 + V_9 + V_{10}}{3}$$

3. Terminal No. 3 is phase reference.

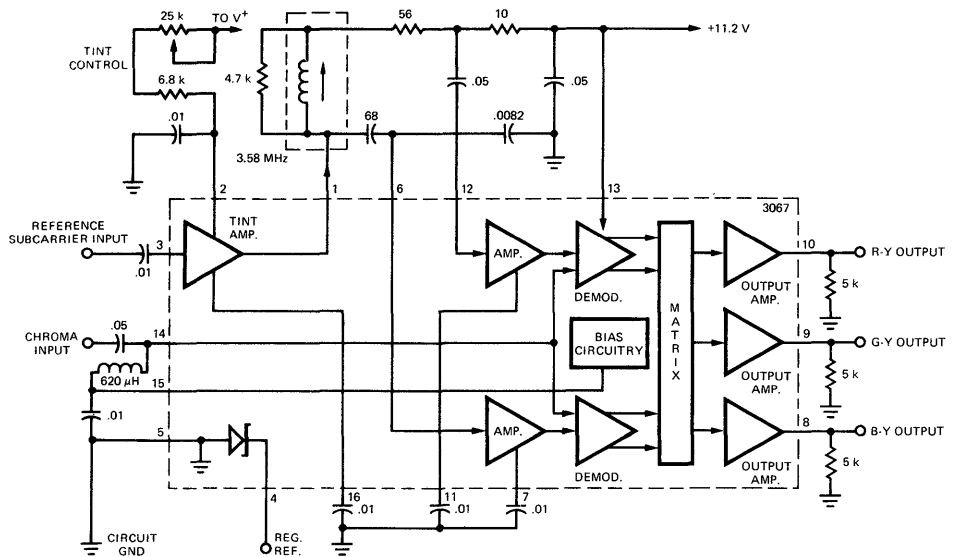
4. Read phase shift as tint control is varied.

FAIRCHILD LINEAR INTEGRATED CIRCUIT • 3067

DC TEST CIRCUIT



AC TEST CIRCUIT

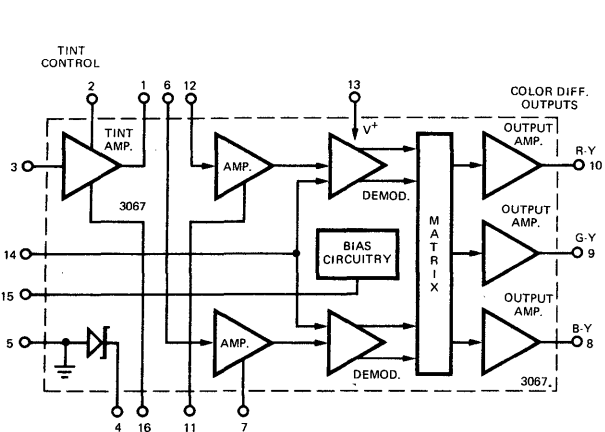


All resistance values are in ohms.
Unless otherwise indicated, all capacitance values less than 1.0 are in microfarads; 1.0 or greater are in picofarads.

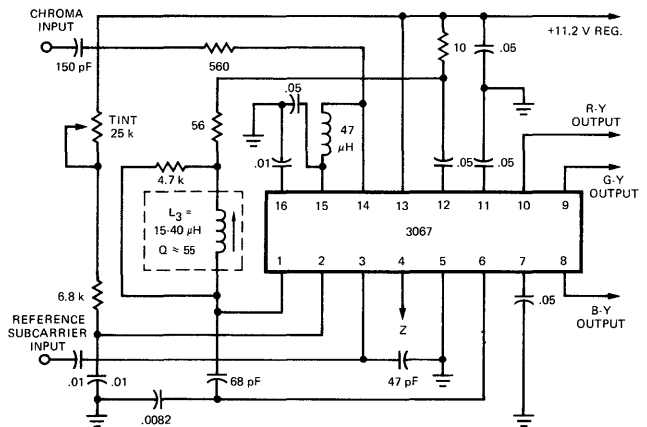
AC TEST PROCEDURE

1. The reference subcarrier input (3) is a 3.58 MHz CW signal from a 50 Ω source.
2. The chroma input (14) is a 3.53 MHz CW signal from a 50 Ω source.
3. Phase and amplitude at terminal Nos. 1, 3, 6, and 12 are measured with vector voltmeter (HP8405A or equivalent).
4. Signals at terminal Nos. 8, 9 and 10 are measured with an ac voltmeter (HP400E or equivalent) or an oscilloscope.
5. Unless otherwise noted the Tint control is at maximum resistance.

BLOCK DIAGRAM



TYPICAL APPLICATION



All resistance values are in ohms.
All capacitance values above 1.0 are in pF, below 1.0 are in μF.

3075

FM IF AMPLIFIER-LIMITER, DETECTOR, AUDIO PREAMPLIFIER FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3075 is a monolithic FM IF sub-system constructed using the Fairchild Planar* epitaxial process. The system consists of a three stage limiting amplifier with a zener diode regulated power supply, a differential peak detector stage and an internally biased audio preamplifier stage.

The IF amplifier stage provides typically 60 dB gain at 10.7 MHz and is followed by a differential limiting stage with constant current source to provide excellent limiting characteristics. The differential peak detector circuit requires only one coil and thus provides easy tuning and minimum external components.

Applications include automotive and home FM receivers, mobile communications equipment, and television sound channels.

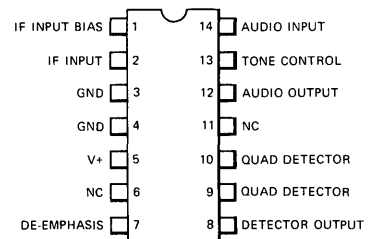
- 250 μ V TYPICAL LIMITING SENSITIVITY AT 10.7MHz
- 125 μ V TYPICAL LIMITING SENSITIVITY AT 4.5MHz
- 55dB TYPICAL AM REJECTION AT 4.5MHz
- SINGLE COIL TUNING
- DIFFERENTIAL PEAK DETECTION
- INTERNAL ZENER DIODE REGULATION FOR IF SECTION

ABSOLUTE MAXIMUM RATINGS (Voltage at any terminal must not exceed V+)

Supply Voltage (Pin 5)	+18V
Input Voltage (between pins 1 and 2)	± 3 V
Power Dissipation (Note 1)	670mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering 60 Seconds) CA3075D	300°C
Molded DIP (Soldering 10 Seconds) CA3075E	260°C

NOTE 1: Rating applies to $T_A = 70^\circ\text{C}$. Above 70°C derate at 8.3 mW/ $^\circ\text{C}$.

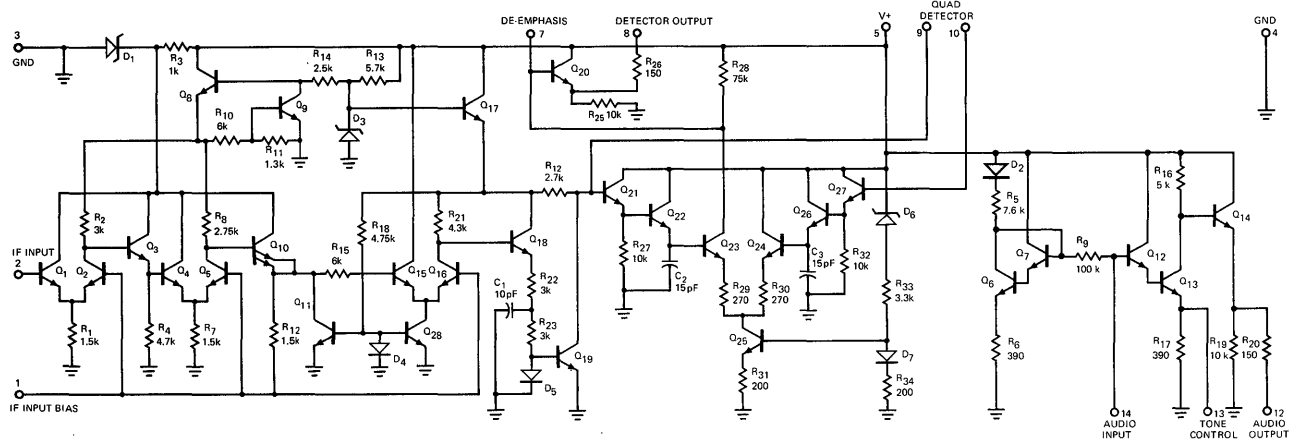
**CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A**



ORDER INFORMATION

TYPE	PART NO.
3075	CA3075D
3075	CA3075E

EQUIVALENT CIRCUIT

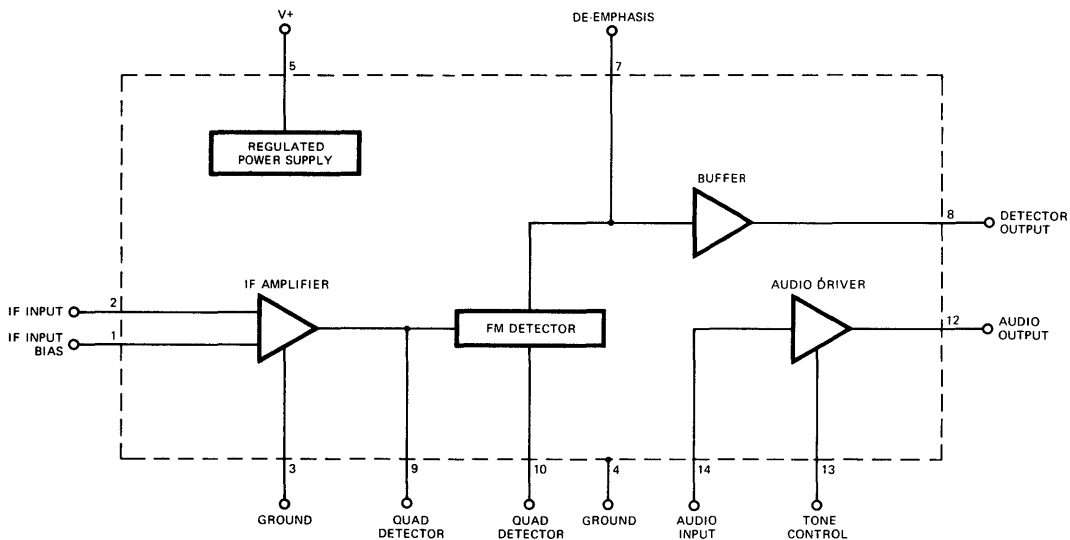


3075

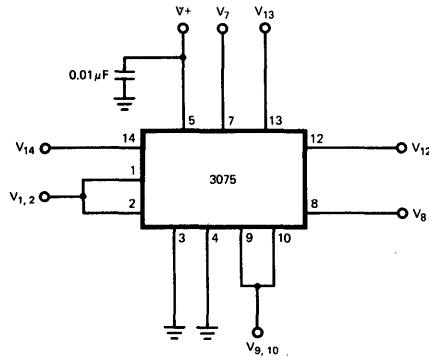
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_+ = +12\text{V}$, unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC CHARACTERISTICS (Test Circuit 1)					
Supply Current I_5	$V_+ = 8.5\text{V}$	8.0	11		mA
	$V_+ = 12\text{V}$	12	17	28	mA
	$V_+ = 16\text{V}$		25	35	mA
Power Dissipation				340	mW
Terminal Voltages	Pin 7		6.0		V
	Pin 8		5.5		V
	Pin 12	R_L at Pin 12 = 3.9Ω		5.0	V
DC Shift Pin 8	Change V_+ from 10V to 16V	-600		+600	mV
AC CHARACTERISTICS (IF Stage $f = 10.7\text{ MHz}$, Test Circuit 2)					
-3dB Limiting Sensitivity			250	600	μV
Recovered Audio at Detector Output		0.5	0.7		V_{RMS}
THD at Detector Output			1.0	2.0	%
AM Rejection		40	50		dB
AC CHARACTERISTICS (IF Stage $f = 4.5\text{ MHz}$, Test Circuit 2)					
-3dB Limiting Sensitivity			125	400	μV
Recovered Audio at Detector Output		1.0	1.4		V_{RMS}
THD at Detector Output			1.5	2.0	%
AM Rejection		40	56		dB
AC CHARACTERISTICS (Audio Amplifier $f = 1\text{ kHz}$, Test Circuit 3)					
Input Resistance		40			$\text{k}\Omega$
Voltage Gain		10	12	17	V/V
THD at Detector Output	$V_{\text{OUT}} = 2 V_{\text{RMS}}$		2.0	4.0	%
Maximum Available Output Swing		8.4			V _{p-p}

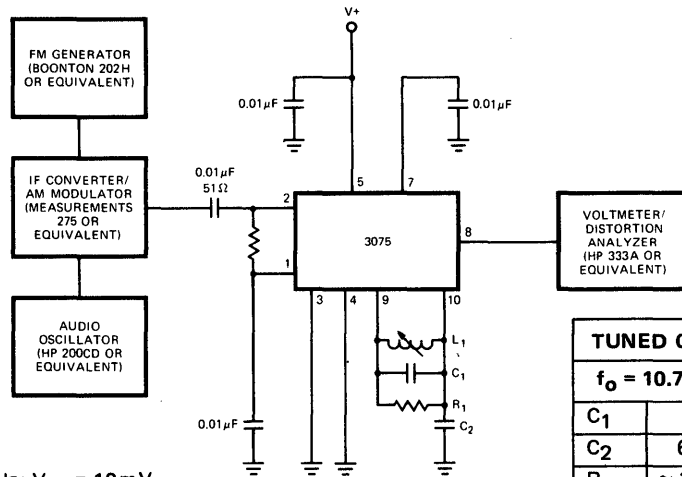
BLOCK DIAGRAM



TEST CIRCUITS



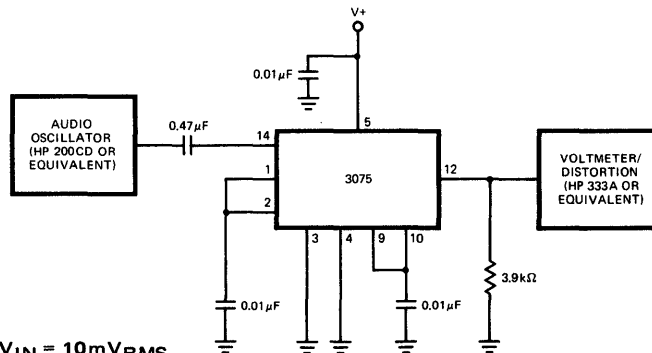
TEST CIRCUIT 1



TUNED CIRCUIT COMPONENTS		
	$f_o = 10.7\text{MHz}$	$f_o = 4.5\text{MHz}$
C_1	33pF	68pF
C_2	6.8pF	12pF
R_1	$\approx 33k\Omega$	
L_1	7 μH	16 μH
Q_L	55	55

FM = 4.5 MHz \pm 25kHz @ 400Hz; $V_{IN} = 10\text{mV}_{RMS}$
 NO CONNECTION TO PINS 6, 11, 12, 13, 14
 AM modulation = 30% @ 400 Hz
 Select R_1 for desired loaded Q (Q_L).

TEST CIRCUIT 2



FM = 10.7MHz @ 400Hz, $V_{IN} = 10\text{mV}_{RMS}$
 NO CONNECTION TO PINS 6, 7, 8, 11, 13

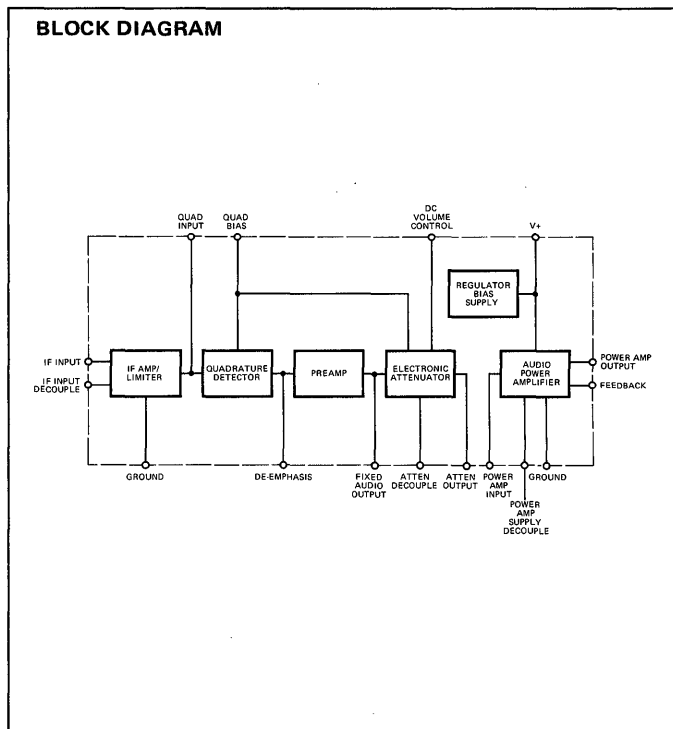
TEST CIRCUIT 3

μA704

TELEVISION SOUND SYSTEM

GENERAL DESCRIPTION — The μA704 is designed to perform the entire sound function in a television receiver. It can also perform the functions of the IF amplifier/limiter, detector, dc volume control, audio amplifier and power output stages in a monophonic FM radio. The circuit provides an undistorted power output of 2.0W into a 16Ω or 8.0Ω load and 1.0W into a 4.0Ω load. It operates over a supply voltage range of 10V to 30V while maintaining V+/2 output tracking and 40dB ripple rejection. An electronic attenuator makes possible a dc volume control with greater than 80dB range. The desired volume control characteristic is achieved using an inexpensive linear potentiometer. A fixed audio output is provided for use with an ac volume control or a video tape recorder. Other features are thermal overload protection, ac short circuit protection at the power amplifier output, and a low external component count.

- GOOD LIMITING SENSITIVITY . . . 100μV
- DC VOLUME CONTROL
- HIGH OUTPUT POWER . . . 2.0W WITH ±7.5kHz DEVIATION
- GOOD AM REJECTION . . . 45dB TYPICAL
- LOW DISTORTION
- OPERATES FROM 10 TO 30V
- THERMAL SHUTDOWN
- SHORT CIRCUIT PROTECTION
- LOW EXTERNAL COMPONENT COUNT
- FIXED OUTPUT AVAILABLE FOR VTR APPLICATIONS

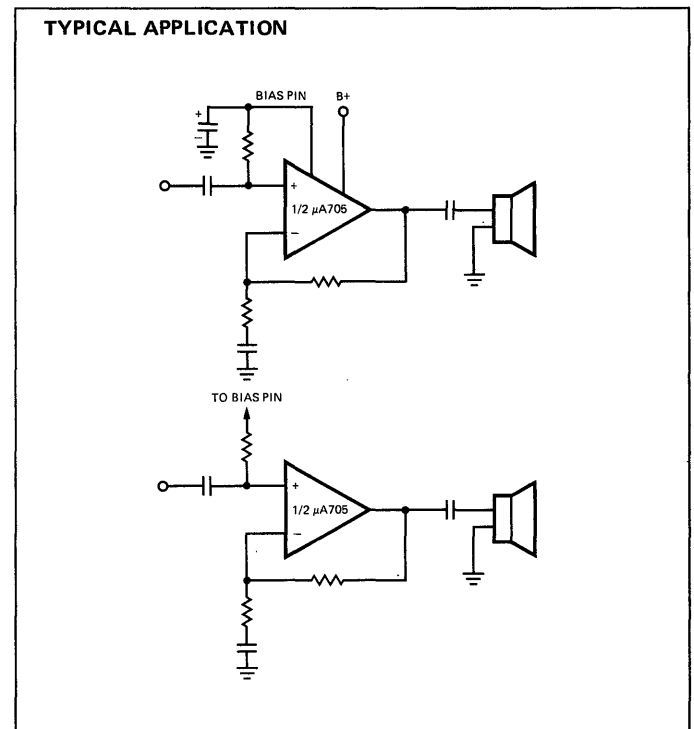


μA705

DUAL CHANNEL AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION — The μA705 is a Dual Audio Power Amplifier capable of delivering 2.5W per channel into an 8Ω load from a supply voltage of 18 Vdc. The device can be operated over a supply range of 6.0V to 30V. The μA705 requires a minimum of external components; short circuit current limiting and thermal limiting are incorporated on-chip for device protection. In addition, the device incorporates an internal ripple filter for unregulated or minimally filtered power supplies without use of large electrolytic capacitors. A fast charge circuit is included to eliminate undesirable pops in the speakers caused by turn on transients.

- 2.5W CONTINUOUS POWER/CHANNEL
- TYPICALLY 80dB GAIN
- LOW DISTORTION (TYPICALLY 0.3%)
- FAST CHARGE CIRCUIT ELIMINATES TURN ON SPEAKER POPS
- SELF CENTERING BIASING WITH RIPPLE FILTER
- SHORT CIRCUIT AND THERMAL PROTECTION



μA7350

TACHOMETER SUBSYSTEM

GENERAL DESCRIPTION — The μA7350 includes a tachometer circuit, as well as an operational amplifier and two comparators constructed using the Fairchild Planar* epitaxial process. The tachometer produces fixed width pulses at the zero crossing of a ground referenced ac input signal. Each pulse width is individually determined by the choice of an external resistor and capacitor. The output stage of the tachometer section is a common emitter NPN transistor with an uncommitted collector. The operational amplifier and comparators are of identical design except that the comparators have no provision for external compensation. Their output stages consist of Class A PNP amplifiers with uncommitted collectors which allow variety of loads for general purpose applications. In addition, the outputs of the comparators may be wired-OR for use as a dual level sensor.

The entire device will function on a single as well as a dual supply system.

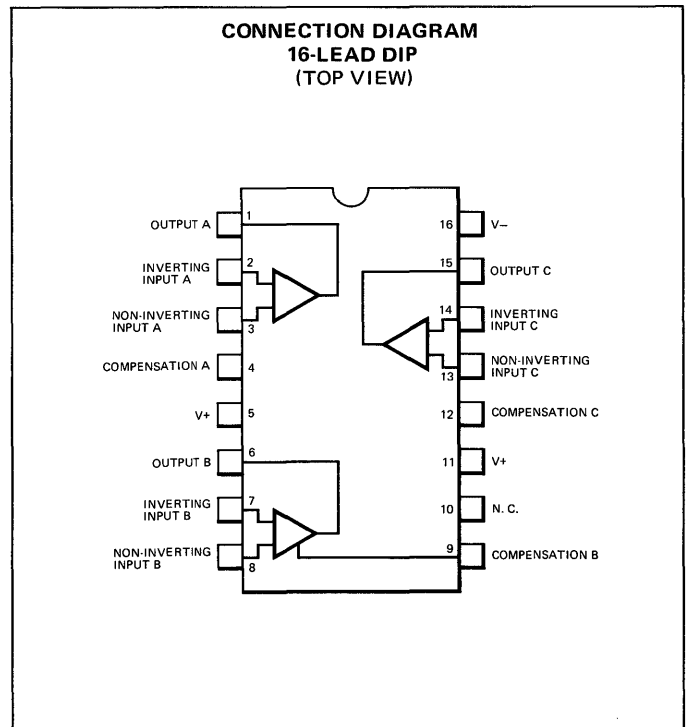
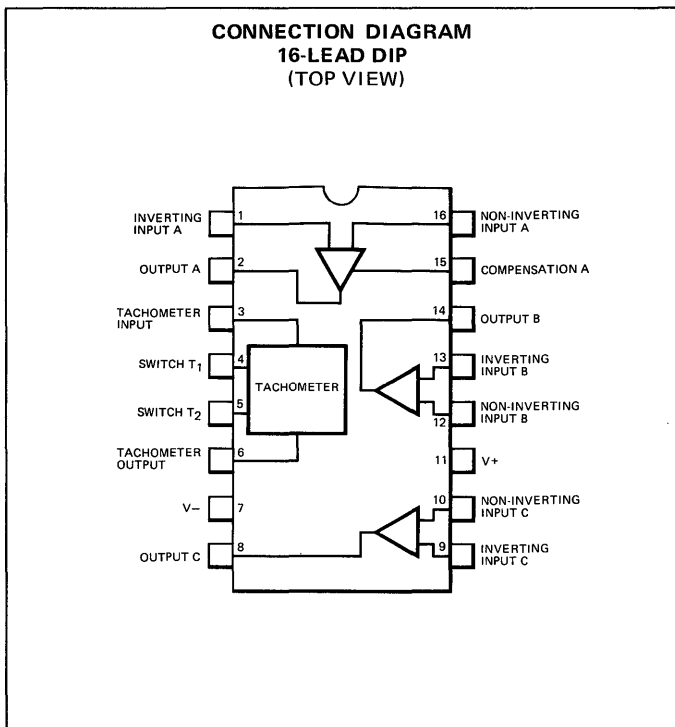
- SINGLE OR DUAL SUPPLY OPERATION
- TACHOMETER, OPERATIONAL AMPLIFIER AND TWO COMPARATORS ON ONE CHIP
- SEPARATELY CONTROLLED PULSE WIDTHS AT POSITIVE AND NEGATIVE ZERO CROSSINGS
- UNCOMMITTED COLLECTOR OUTPUTS
- SHORT-CIRCUIT PROTECTED

μA7351

TRIPLE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION — The μA7351 consists of three identical operational amplifiers constructed using the Fairchild Planar* epitaxial process. Each two stage amplifier uses a Class A PNP common emitter output stage with an uncommitted collector, which allows a variety of loads for general purpose applications. In addition, the outputs of two or more of the op amps may be wired-OR for use as logic blocks, such as dual level comparators. The absence of latch-up makes them ideal for use as voltage followers. Designed specifically to operate on a single supply, the μA7351 is an excellent choice for automotive systems and other battery operated equipment requiring general purpose operational amplifiers.

- OPERATION ON SINGLE SUPPLIES +4.0 TO +16V OR DUAL SUPPLIES ±2.0 TO ±8.0V
- LOW POWER CONSUMPTION
- NO LATCH UP
- SHORT CIRCUIT PROTECTED
- VERSATILE OUTPUT STAGE GIVES WIRED-OR CAPABILITY AND WIDE OUTPUT SWING



*Planar is a patented Fairchild process

TBA920

HORIZONTAL OSCILLATOR, PHASE COMPARATOR AND SYNC SEPARATOR

TBA970

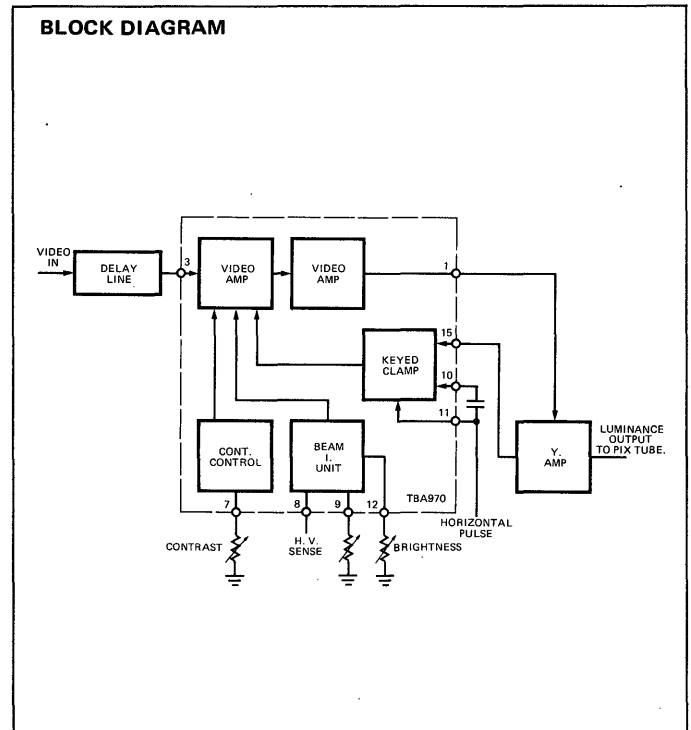
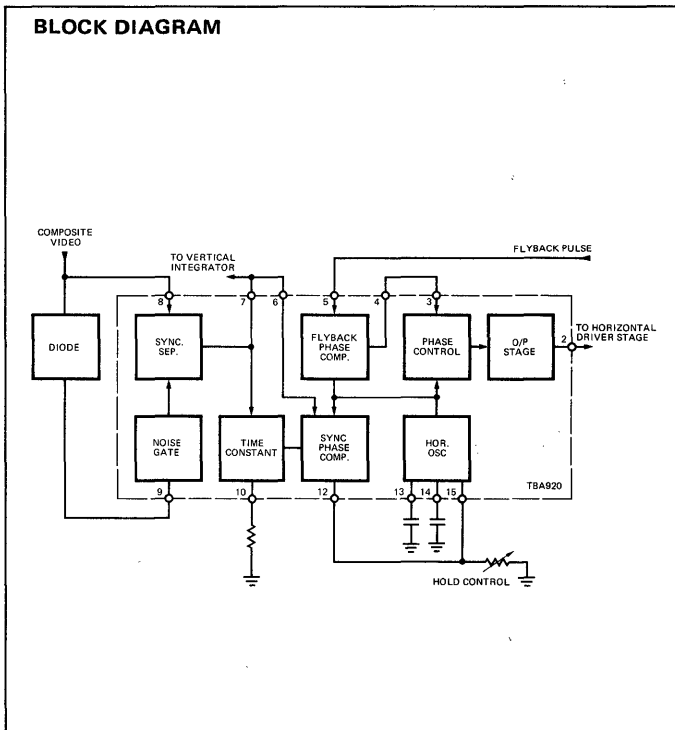
TELEVISION VIDEO AMPLIFIER

GENERAL DESCRIPTION — The TBA920 is a monolithic integrated circuit designed for TV receiver applications. It accepts the composite video signal, separates sync pulses with the added safeguard of noise gating and provides a sync output for the vertical integrator. Also incorporated is the horizontal oscillator along with two phase comparators, one to compare flyback pulses to the oscillator and the other for sync phase comparison. The device will interface with both SCR and transistor deflection systems.

GENERAL DESCRIPTION — The TBA970 is a monolithic integrated video amplifier for television receivers. In addition to video amplification, it provides a dc contrast control which can be ganged to the chroma gain control, beam current limiting and black level control by a clamped feedback circuit combined with the brightness control.

- SYNC SEPARATOR
- NOISE GATE
- HORIZONTAL OSCILLATOR
- DUAL PHASE COMPARATOR

- DC CONTRAST CONTROL
- DC BRIGHTNESS CONTROL
- BLACK LEVEL CLAMPING
- BEAM CURRENT LIMITING

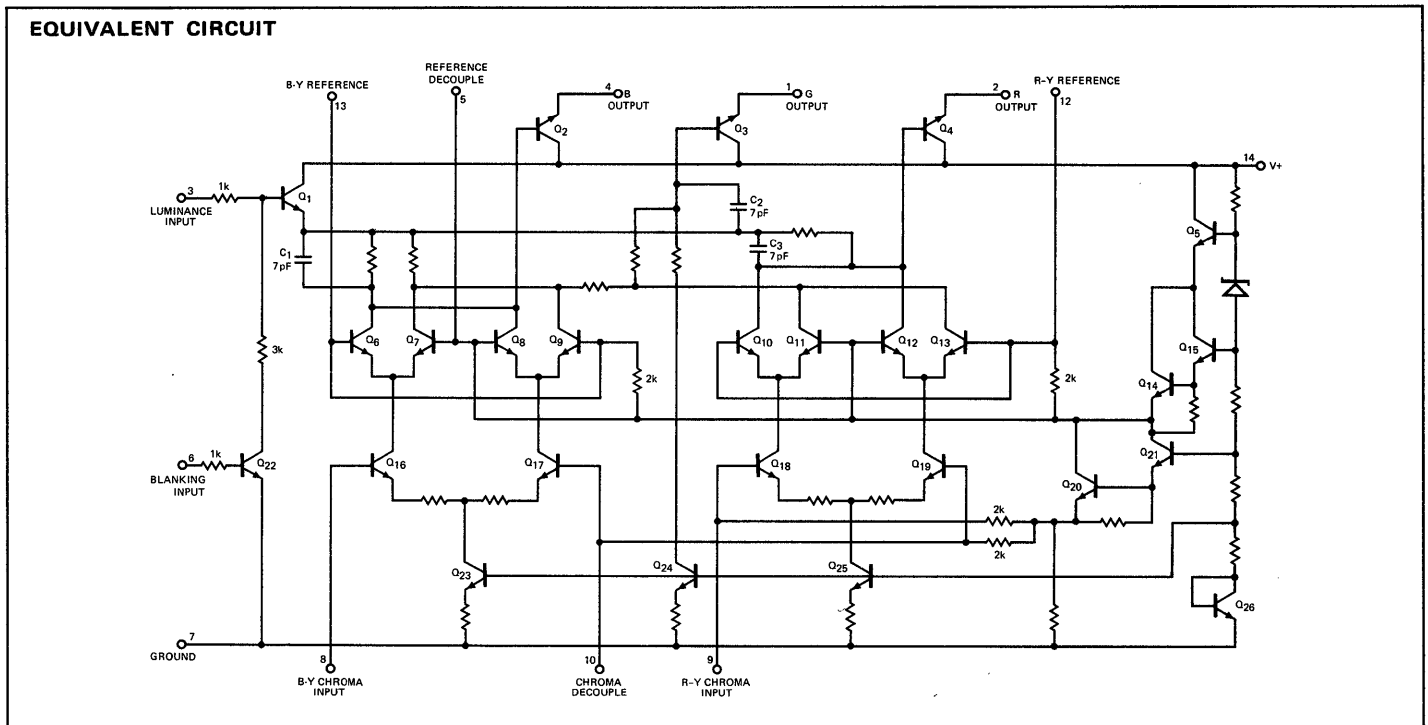


1326

CHROMA DEMODULATOR

GENERAL DESCRIPTION — The 1326 is a color television Chroma Demodulator constructed on a monolithic chip using the Fairchild Planar* process. The device demodulates the chroma subcarrier information contained in an NTSC color television video signal and can provide either color difference or RGB signals at the outputs. The low voltage drift of the dc output ensures excellent performance in direct coupled output circuitry.

- LUMINANCE AND BLANKING INPUTS
- COLOR DIFFERENCE OR RGB OUTPUTS
- HIGH OUTPUT VOLTAGE SWING
- LOW OUTPUT VOLTAGE DRIFT WITH TEMPERATURE
- ON-CHIP FILTERING OF OUTPUT RF COMPONENTS



*Planar is a patented Fairchild process

2136

FM IF AMPLIFIER AND DETECTOR

GENERAL DESCRIPTION — The 2136 FM sound system consists of a limiting IF amplifier and doubly balanced quadrature detector. Excellent sensitivity, good AM rejection and an internally regulated power supply coupled with low external component count make the 2136 suitable for many FM applications.

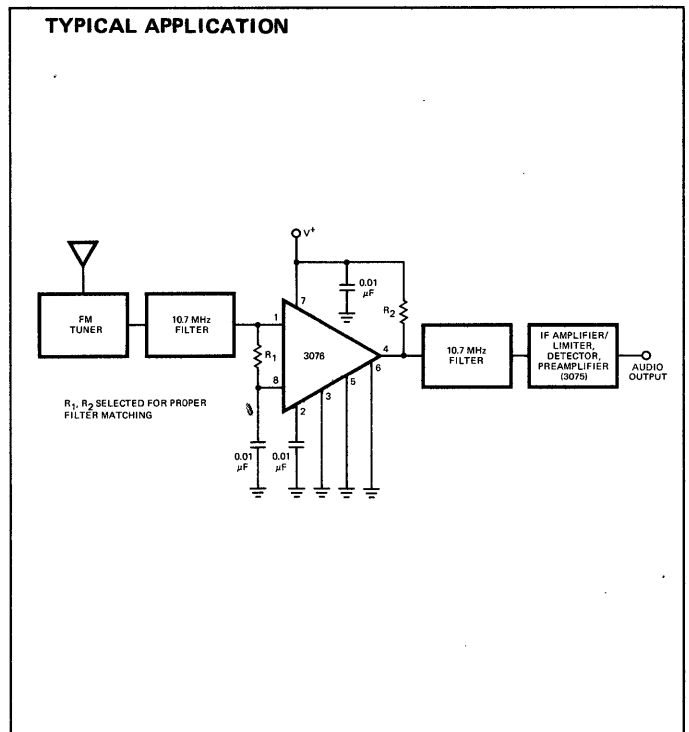
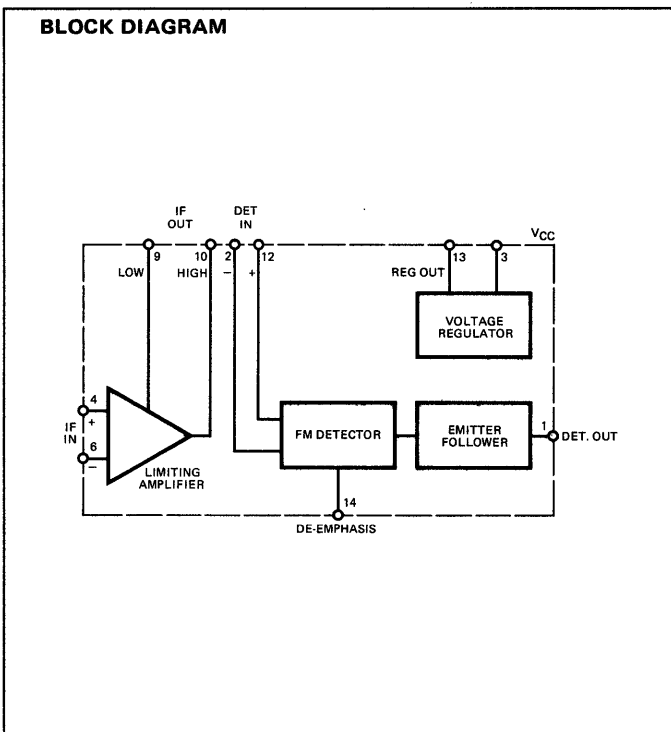
- 300 μ V LIMITING SENSITIVITY
- 40dB AM REJECTION
- SINGLE TUNING COIL
- EXCELLENT REGULATION
- LOW DISTORTION

3076

FM GAIN BLOCK

GENERAL DESCRIPTION — The 3076 is a monolithic high gain wideband IF amplifier-limiter constructed using the Fairchild Planar* epitaxial process. The device provides a four stage IF amplifier-limiter with its own voltage regulator section. The four stage amplifier is emitter coupled between stages and typically provides 80 dB of voltage gain, with a 2 k Ω load at 10.7 MHz. Excellent limiting in the differential output stage is provided by the use of a constant current sink. The regulator section uses a zener diode to provide regulated and decoupled voltages to the amplifier.

- 50 μ V TYPICAL LIMITING SENSITIVITY AT 10.7MHz
- 80dB GAIN WITH 2k Ω LOAD
- INTERNAL ZENER DIODE SUPPLY REGULATION
- BANDWIDTH 20MHz



GLOSSARY

CONSUMER

AM Rejection — The ratio of the recovered audio output produced by a desired FM signal with specified modulation, amplitude and frequency to that produced by an AM signal, on the same carrier, with specified modulation index.

Burst Separator Output — The amplitude of the chroma reference burst at the output of the gated burst amplifier.

Channel Balance, Monaural Input — The ratio of the outputs from the right and left channels with a monaural signal applied to the input.

Common Mode Gain — The ratio of the output voltage change to the input common mode voltage producing that change.

Converter Transconductance — The ratio of the converter output ac current to the input voltage causing it.

Differential Output Resistance — The resistance measured between the two output terminals.

Differential Output Voltage Swing — The peak differential output voltage that can be obtained without clipping the output voltage waveform.

Equivalent Input Noise Voltage — The equivalent input noise voltage which would reproduce the noise seen at the output if all other noise sources were turned off and the source resistance set to zero.

Feedback Capacitance — The effective value of the capacitive coupling from output to input.

Forward Transadmittance — The ratio of the small signal ac short-circuit output current to the input voltage causing it.

Forward Transfer Admittance, (Y_{21}) — See Forward Transadmittance.

Frequency Response — The frequency at which the output drops to 0.707 of its low frequency value.

IF Transconductance — The ratio of the output ac IF current to the input signal voltage.

Input Admittance (Y_{11}) — The ratio of the small signal ac input current to the input voltage causing it, with the output short circuited.

Input Limiting Voltage at -3.0 dB Point — See Limiting Sensitivity.

Input Offset Current — The difference in current into the two input terminals with the output voltage at zero.

Input Voltage for -3.0 dB Limiting at Output — See Limiting Sensitivity.

Input Voltage Range — The range of input voltage over which the device will operate within specifications.

Intermodulation Products — Undesired output signals created by interaction of undesired input signals.

Internal Power Dissipation — The power dissipated by the device under specified conditions.

Killer Off Threshold — The voltage required at the color killer terminal to restore the chroma output.

Killer On Threshold — The voltage required at the color killer terminal to kill the chroma output.

Limiting Sensitivity — The value of input voltage above which the output is 3.0 dB below its limited value.

Maximum Available Output Swing — The maximum available output voltage without clipping of the output voltage waveform.

Noise Figure – The common logarithm of the ratio of the input signal to noise ratio to the output signal to noise ratio.

Oscillator Control Sensitivity – The ratio of the change in oscillator frequency to the change in control voltage causing it.

Oscillator Pull-In Range – The range of free-running frequency over which the oscillator will lock to the incoming signal.

Oscillator Static Phase Error – The phase difference between the oscillator output and the incoming frequency to which it is locked.

Output Admittance (Y_{22}) – The ratio of the small signal ac output current to the ac output voltage with the input short-circuited.

Output Common Mode Voltage – The average of the voltages at the output terminals.

Output Conductance – The resistive value of the output admittance.

Output Saturation Voltage – The dc voltage between output and ground in the saturated condition.

Play-Through Voltage – The signal voltage measured at the output with the volume control set for minimum output.

Power Supply Sensitivity – The ratio of the change in a specified parameter to the change in power supply voltage causing it.

Quiescent Output Current – The output current with no signal applied at the input.

Recovered Audio – The value of the audio voltage measured at the detector output under the specified circuit conditions.

Reverse Transfer Admittance (Y_{12}) – The ratio of the small

signal ac input current to the ac output voltage, with the input short-circuited.

RF Noise Voltage – The equivalent input noise voltage of the RF Stage.

RF Transconductance – The ratio of the RF output current to the RF input voltage.

Short-Circuit Load Current – The maximum output current which the device will provide into a short-circuit.

Stereo Separation – The ratio of the right and left channel outputs for a standard input signal with specified audio frequency.

Supply Regulation – The change in internal device supply voltage for a specified change in external power supply voltage.

Supply Rejection – The ratio of the change in a specified circuit voltage to the change in supply voltage causing it.

Temperature Coefficient of dc Voltage – The change in dc voltage over the operating temperature range divided by the operating temperature range.

THD – See Total Harmonic Distortion.

Total Harmonic Distortion – The rms value of the harmonic content of a signal expressed as a percentage of the rms value of its fundamental.

Voltage Gain – The ratio of the output signal voltage to the input signal voltage under linear conditions.

67 kHz Storecast Rejection – The ratio of the 67 kHz SCA signal at the output to the desired output with the standard FCC signal input.

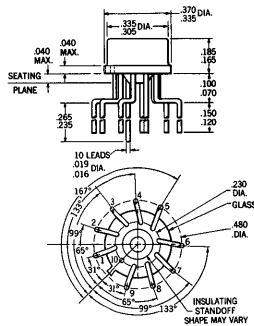
CONSUMER LINEAR INTEGRATED CIRCUITS OPTIONAL PACKAGE OUTLINES

(H) 5A

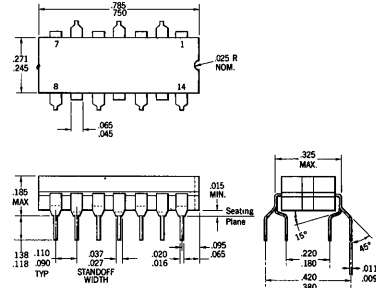
(D) 7F

JEDEC (TO-100) With Formed Leads

14-Lead Hermetic Quad In-Line



NOTES
 All dimensions in inches
 Leads are gold plated kovar
 Package weight is 1.22 gram
 This is a 5E package with the leads formed



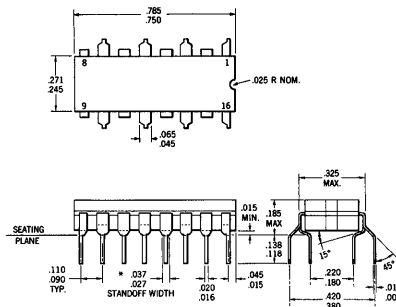
NOTES
 Package weight is 2.0 grams
 This is a 6A package with the leads formed

16-Lead Hermetic Quad In-Line

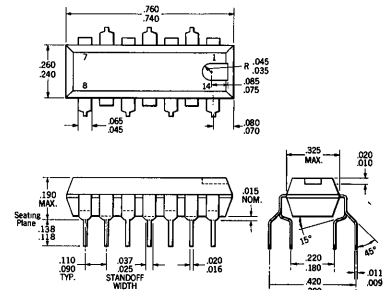
(D) 7H

14-Lead Molded Quad In-Line

(P) 9C



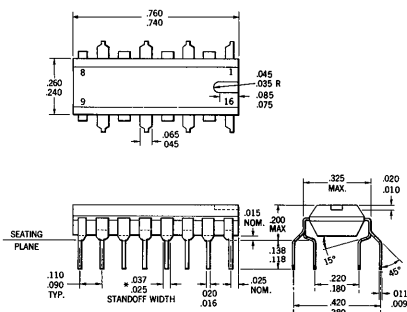
NOTES
 Package weight is 2.0 grams
 *The .037/.027 dimension does not apply to the corner leads
 This is a 6B package with the leads formed



NOTES
 Package weight is 0.9 grams
 This is a 9A package with the leads formed

16-Lead Molded Quad In-Line

(P) 9D



NOTES
 Package weight is 0.9 grams
 *The .037/.027 dimension does not apply to the corner leads
 This is a 9B package with the leads formed

GENERAL NOTES FOR (D)7F, (D)7H, (P)9C, AND (P)9D

All dimensions in inches
 Leads are intended for insertion in hole rows on .300" centers
 They are purposely shipped with "positive" misalignment to facilitate insertion
 Board-drilling dimensions should equal your practice for .020 inch diameter lead
 Leads are tin-plated kovar

LINEAR LINEAR LINEAR LINEAR LINEAR LINEAR LINEAR

CONTENTS AND SECTION SELECTOR

TRANSISTOR/DIODE ARRAYS/ANALOG SWITCHES	8
PACKAGE OUTLINES	9
ORDER INFORMATION	10
MIL-M-38510/MIL-STD-883	11
DICE	12
INDUSTRY CROSS REFERENCE GUIDE	13
APPLICATION INFORMATION	14

INDEX

Transistor/diode array and analog switches data sheets are presented in alphanumeric sequence.

DATA SHEETS

μ A726	Temperature - Controlled Differential Pair	8-3
3018	Transistor Array	8-6
3018A	Transistor Array	8-6
3019	Diode Array	8-6
3026	Transistor Array	8-6
3036	Transistor Array	8-6
3039	Diode Array	8-6
3045	Transistor Array	8-6
3046	Transistor Array	8-6
3054	Transistor Array	8-6
3086	Transistor Array	8-6
SH3002	SPDT Analog Switch	8-22
Glossary		8-25

μA726

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA726 is a Monolithic Transistor Pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers. It is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

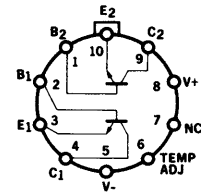
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
Military (726)	-55°C to +125°C
Commercial (726C)	0°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18V
Internal Power Dissipation	500mW

MAXIMUM RATINGS FOR EACH TRANSISTOR

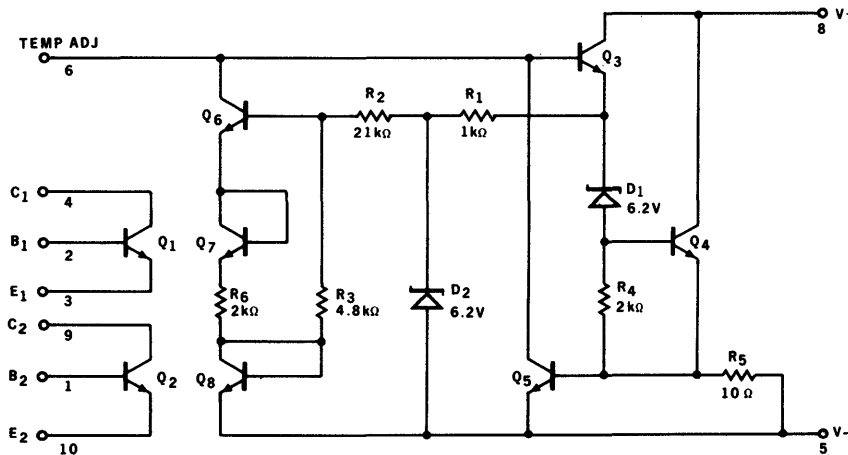
Collector-to-Emitter Voltage, V_{CE0}	30V
Collector-to-Base Voltage, V_{CB0}	40V
Collector-to-Substrate Voltage, V_{C10}	40V
Emitter-to-Base Voltage, V_{EBO}	5V
Collector Current, I_C	5mA

CONNECTION DIAGRAM
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5U



ORDER INFORMATION	
TYPE	PART NO.
726	726HM
726C	726HC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A726

726

ELECTRICAL CHARACTERISTICS ($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, $R_{\text{adj}} = 62\text{k}\Omega$ unless otherwise specified)

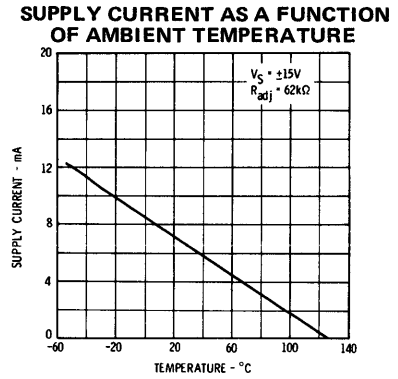
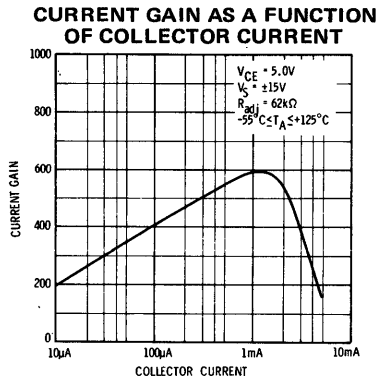
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\mu\text{A} \leq I_C \leq 100\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$		10	50	nA
	$I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$		50	200	nA
Average Input Bias Current	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$		50	150	nA
	$I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$		250	500	nA
Offset Voltage Change	$I_C = 10\mu\text{A}$, $5\text{V} \leq V_{CE} \leq 25\text{V}$, $R_S \leq 100\text{k}\Omega$		0.3	6.0	mV
	$I_C = 100\mu\text{A}$, $5\text{V} \leq V_{CE} \leq 25\text{V}$, $R_S \leq 10\text{k}\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$10\mu\text{A} \leq I_C \leq 100\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$, $+25^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		0.2	1.0	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Voltage Drift	$10\mu\text{A} \leq I_C \leq 100\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$, $-55^{\circ}\text{C} \leq T_A \leq +25^{\circ}\text{C}$		0.2	1.0	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current Drift	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$		10		$\text{pA}/^{\circ}\text{C}$
	$I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$		30		$\text{pA}/^{\circ}\text{C}$
Supply Voltage Rejection Ratio	$10\mu\text{A} \leq I_C \leq 100\mu\text{A}$, $R_S \leq 50\Omega$		25		$\mu\text{V}/\text{V}$
Low Frequency Noise	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$ BW = .001 Hz to 0.1 Hz		4.0		$\mu\text{V p-p}$
Broadband Noise	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$ BW = 0.1 Hz to 10kHz		10		$\mu\text{V p-p}$
Long-term Drift	$10\mu\text{A} \leq I_C \leq 100\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$, $T_A = 25^{\circ}\text{C}$		5.0		$\mu\text{V}/\text{week}$
High Frequency Current Gain	$f = 20\text{MHz}$, $I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5\text{V}$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\mu\text{A}$		1.0		pF
Collector Saturation Voltage	$I_B = 100\mu\text{A}$, $I_C = 1\text{mA}$		0.5	1.0	V

726C

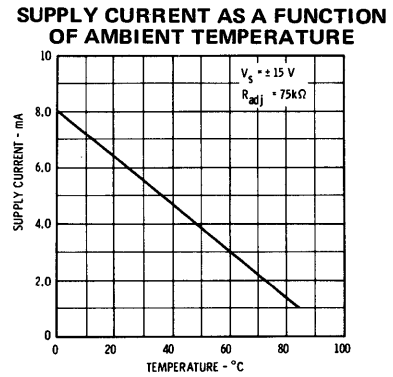
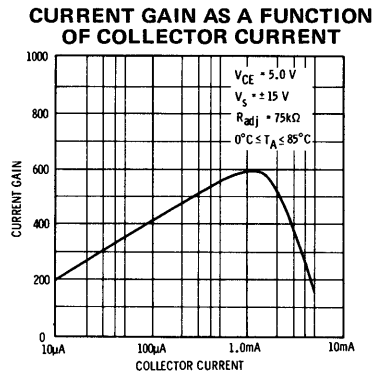
ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, $R_{\text{adj}} = 75\text{k}\Omega$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\mu\text{A} \leq I_C \leq 100\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$		10	100	nA
	$I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$		50	400	nA
Average Input Bias Current	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$		50	300	nA
	$I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$		250	1000	nA
Offset Voltage Change	$I_C = 10\mu\text{A}$, $5\text{V} \leq V_{CE} \leq 25\text{V}$, $R_S \leq 100\text{k}\Omega$		0.3	6.0	mV
	$I_C = 100\mu\text{A}$, $5\text{V} \leq V_{CE} \leq 25\text{V}$, $R_S \leq 10\text{k}\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$		0.2	2.0	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current Drift	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$		10		$\text{pA}/^{\circ}\text{C}$
	$I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$		30		$\text{pA}/^{\circ}\text{C}$
Supply Voltage Rejection Ratio	$I_C = 100\mu\text{A}$, $R_S \leq 50\Omega$		25		$\mu\text{V}/\text{V}$
Low Frequency Noise	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz		4.0		$\mu\text{V p-p}$
Broadband Noise	$I_C = 10\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10kHz		10		$\mu\text{V p-p}$
Long-Term Drift	$I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$, $R_S \leq 50\Omega$, $T_A = 25^{\circ}\text{C}$		5.0		$\mu\text{V}/\text{week}$
High Frequency Current Gain	$f = 20\text{MHz}$, $I_C = 100\mu\text{A}$, $V_{CE} = 5\text{V}$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5\text{V}$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\mu\text{A}$		1.0		pF
Collector Saturation Voltage	$I_B = 100\mu\text{A}$, $I_C = 1\text{mA}$		0.5	1.0	V

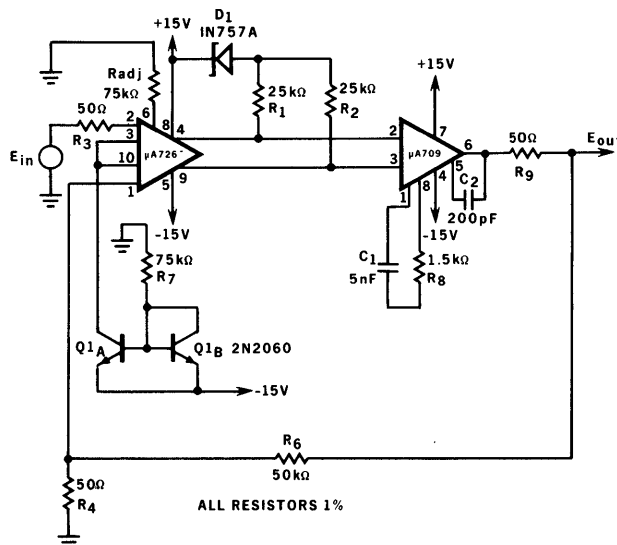
TYPICAL PERFORMANCE CURVES FOR 726



TYPICAL PERFORMANCE CURVES FOR 726C



TYPICAL X100 AMPLIFIER CIRCUIT



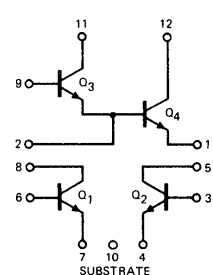
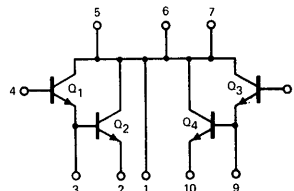
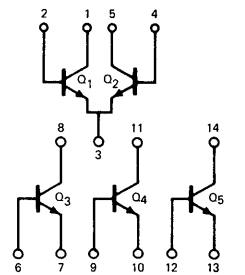
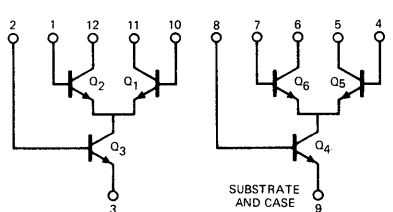
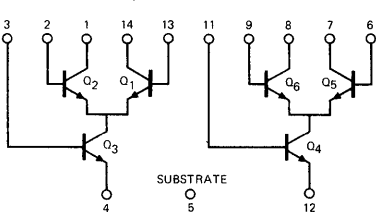
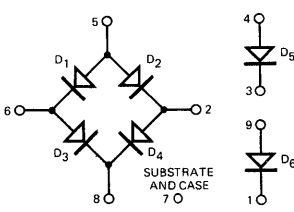
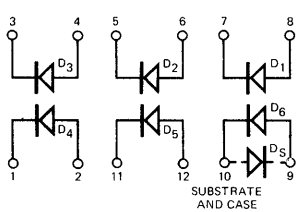
3018•3018A•3019•3026•3036 3039•3045•3046•3054•3086

TRANSISTOR AND DIODE ARRAYS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — Fairchild Transistor and Diode Arrays consist of general purpose integrated circuit devices constructed on a single substrate, using the Fairchild Planar* epitaxial process. These arrays are arranged to offer maximum flexibility in circuit design for applications from dc to 120 MHz. Excellent transistor and diode matching and temperature tracking allow circuit techniques unavailable when using discrete devices. Multiple devices in one package permit a greater packing density and cost saving than with individually packaged transistors.

- PRECISION MONOLITHIC MATCHING
- DESIGN FLEXIBILITY
- CUSTOM APPLICATIONS

<p>PACKAGE OUTLINE 5G</p>  <p>ORDER INFORMATION</p> <table border="0"> <tr> <td>TYPE</td> <td>PART NO.</td> </tr> <tr> <td>3018/3018A</td> <td>CA3018/CA3018A</td> </tr> </table>	TYPE	PART NO.	3018/3018A	CA3018/CA3018A	<p>PACKAGE OUTLINE 5E</p>  <p>ORDER INFORMATION</p> <table border="0"> <tr> <td>TYPE</td> <td>PART NO.</td> </tr> <tr> <td>3036</td> <td>CA3036</td> </tr> </table>	TYPE	PART NO.	3036	CA3036	<p>PACKAGE OUTLINE 6A</p>  <p>ORDER INFORMATION</p> <table border="0"> <tr> <td>TYPE</td> <td>PART NO.</td> </tr> <tr> <td>3045/3046/3086</td> <td>CA3045/3046/3086</td> </tr> </table>	TYPE	PART NO.	3045/3046/3086	CA3045/3046/3086
TYPE	PART NO.													
3018/3018A	CA3018/CA3018A													
TYPE	PART NO.													
3036	CA3036													
TYPE	PART NO.													
3045/3046/3086	CA3045/3046/3086													
<p>PACKAGE OUTLINE 5G</p>  <p>ORDER INFORMATION</p> <table border="0"> <tr> <td>TYPE</td> <td>PART NO.</td> </tr> <tr> <td>3026</td> <td>CA3026</td> </tr> </table>	TYPE	PART NO.	3026	CA3026	<p>PACKAGE OUTLINE 6A</p>  <p>ORDER INFORMATION</p> <table border="0"> <tr> <td>TYPE</td> <td>PART NO.</td> </tr> <tr> <td>3054</td> <td>CA3054</td> </tr> </table>	TYPE	PART NO.	3054	CA3054					
TYPE	PART NO.													
3026	CA3026													
TYPE	PART NO.													
3054	CA3054													
<p>PACKAGE OUTLINE 5E</p>  <p>ORDER INFORMATION</p> <table border="0"> <tr> <td>TYPE</td> <td>PART NO.</td> </tr> <tr> <td>3019</td> <td>CA3019</td> </tr> </table>	TYPE	PART NO.	3019	CA3019	<p>PACKAGE OUTLINE 5G</p>  <p>ORDER INFORMATION</p> <table border="0"> <tr> <td>TYPE</td> <td>PART NO.</td> </tr> <tr> <td>3039</td> <td>CA3039</td> </tr> </table>	TYPE	PART NO.	3039	CA3039					
TYPE	PART NO.													
3019	CA3019													
TYPE	PART NO.													
3039	CA3039													

*Planar is a patented Fairchild process.

FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

3018/3018A

- **MATCHED MONOLITHIC GENERAL PURPOSE TRANSISTORS**
- **h_{FE} MATCHED $\pm 10\%$**
- **V_{BE} MATCHED ± 2 mV 3018A (± 5 mV 3018)**
- **OPERATION FROM DC TO 120 MHz**
- **WIDE OPERATING CURRENT RANGE**
- **3018A PERFORMANCE CHARACTERISTICS CONTROLLED FROM $10\mu A$ TO 10 mA**
- **LOW NOISE FIGURE – 3.2 dB TYPICAL AT 1 kHz**
- **FULL MILITARY TEMPERATURE RANGE CAPABILITY (-55 TO $+125^\circ C$)**

APPLICATIONS

- General Use in Signal Processing Systems in dc Through VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	3018	3018A
Any One Transistor	300 mW	300 mW
Total Package	450 mW	450 mW
Temperature Range		
Operating Temperature	$-55^\circ C$ to $+125^\circ C$	$-55^\circ C$ to $+125^\circ C$
Storage Temperature	$-65^\circ C$ to $+200^\circ C$	$-65^\circ C$ to $+200^\circ C$
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage, V_{CEO}	15 V	15 V
Collector-to-Base Voltage, V_{CBO}	20 V	30 V
Collector-to-Substrate Voltage, V_{C1O} (Note 2)	20 V	40 V
Emitter-to-Base Voltage, V_{EBO}	5 V	5 V
Collector Current, I_C	50 mA	50 mA

ELECTRICAL CHARACTERISTICS FOR 3018/3018A ($T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	CONDITIONS	3018			3018A			UNITS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10 V, I_E = 0$	–	0.002	100	–	0.002	40	nA
Collector Cutoff Current	I_{CEO}	$V_{CE} = 10 V, I_B = 0$	–	See Curve	5	–	See Curve	0.5	μA
Collector Cutoff Current Darlington Pair	I_{CEOD}	$V_{CE} = 10 V, I_B = 0$	–	–	–	–	–	5	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1 mA, I_B = 0$	15	24	–	15	24	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10 \mu A, I_E = 0$	20	60	–	30	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10 \mu A, I_C = 0$	5	7	–	5	7	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)C1O}$	$I_C = 10 \mu A, I_{C1} = 0$	20	60	–	40	60	–	V
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1 mA, I_C = 10 mA$	–	0.23	–	–	0.23	0.5	V
Static Forward Current Transfer Ratio	h_{FE}	$V_{CE} = 3 V, \begin{cases} I_C = 10 mA \\ I_C = 1 mA \\ I_C = 10 \mu A \end{cases}$	–	100	–	50	100	–	–
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		$V_{CE} = 3 V, I_{C1} = I_{C2} = 1 mA$	0.9	0.97	–	0.9	0.97	–	–
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	$V_{CE} = 3 V, \begin{cases} I_C = 1 mA \\ I_C = 100 \mu A \end{cases}$	1500	5400	–	2000	5400	–	–
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3 V, \begin{cases} I_E = 1 mA \\ I_E = 10 mA \end{cases}$	–	0.715	–	0.600	0.715	0.800	V
Input Offset Voltage	$\begin{cases} V_{BE1} \\ V_{BE2} \end{cases}$	$V_{CE} = 3 V, I_E = 1 mA$	–	0.48	5	–	0.48	2	mV
Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	$\frac{ \Delta V_{BE} }{\Delta T}$	$V_{CE} = 3 V, I_E = 1 mA$	–	–1.9	–	–	–1.9	–	mV/ $^\circ C$
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} ($V_{9.1}$)	$V_{CE} = 3 V, \begin{cases} I_E = 10 mA \\ I_E = 1 mA \end{cases}$	–	1.46	–	–	1.46	1.60	V
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair- Q_3, Q_4	$\frac{ \Delta V_{BED} }{\Delta T}$	$V_{CE} = 3 V, I_E = 1 mA$	–	4.4	–	–	4.4	–	mV/ $^\circ C$
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{ V_{BE1} - V_{BE2} }{\Delta T}$	$V_{CC} = +6 V, V_{EE} = -6 V,$	–	10	–	–	10	–	$\mu V/^\circ C$

NOTES

1. Derate at 5 mW/ $^\circ C$ for $T_A > 85^\circ C$.
2. Substrate must be connected to the most negative voltage to maintain normal operation.

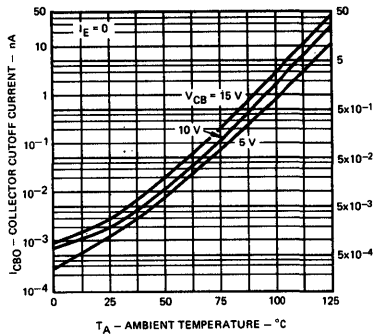
FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

ELECTRICAL CHARACTERISTICS FOR 3018/3018A ($T_A = 25^\circ\text{C}$ unless otherwise specified)

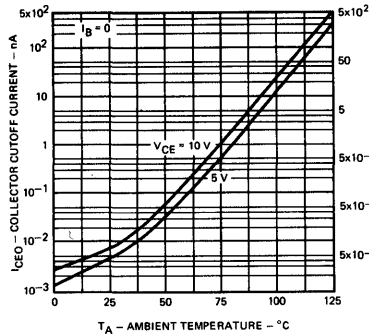
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Low Frequency Noise Figure	NF $f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}, I_C = 100 \mu\text{A}$ Source resistance = $1 \text{ k}\Omega$	—	3.25	—	dB
Low Frequency, Small-Signal Equivalent Circuit Characteristics:					
Forward Current-Transfer Ratio	h_{fe}	—	110	—	—
Short Circuit Input Resistance	h_{ie}	—	3.5	—	$\text{k}\Omega$
Open Circuit Output Conductance	h_{oe}	—	15.6	—	μmho
Open Circuit Reverse Voltage-Transfer Ratio	h_{re}	—	1.8×10^{-4}	—	—
Admittance Characteristics:					
Forward Transfer Admittance	Y_{fe}	—	$31 - j 1.5$	—	mmho
Input Admittance	Y_{ie}	—	$0.3 + j 0.04$	—	mmho
Output Admittance	Y_{oe}	—	$0.001 + j 0.03$	—	mmho
Reverse Transfer Admittance	Y_{re}	—	See Curve	—	mmho
Gain-Bandwidth Product	f_T	300	500	—	MHz
Emitter-to-Base Capacitance	C_{eb}	—	0.6	—	pF
Collector-to-Base Capacitance	C_{cb}	—	0.58	—	pF
Collector-to-Substrate Capacitance	C_{Cl}	—	2.8	—	pF

TYPICAL PERFORMANCE CURVES FOR 3018/3018A

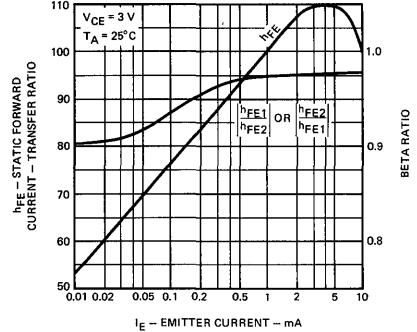
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



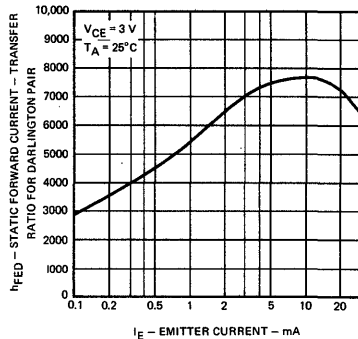
COLLECTOR-TO-EMITTER CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



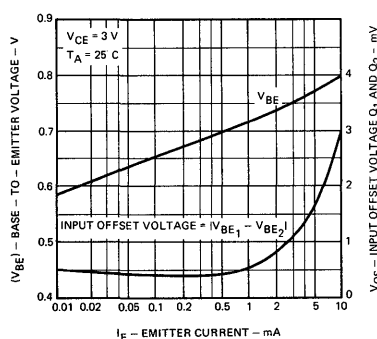
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q1, Q2 AS A FUNCTION OF EMITTER CURRENT



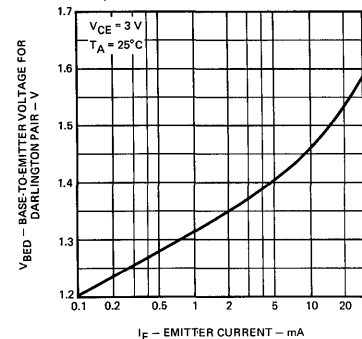
STATIC FORWARD CURRENT-TRANSFER RATIO FOR DARLINGTON CONNECTED TRANSISTORS Q3, Q4 AS A FUNCTION OF EMITTER CURRENT



STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR Q1, Q2 AS A FUNCTION OF EMITTER CURRENT

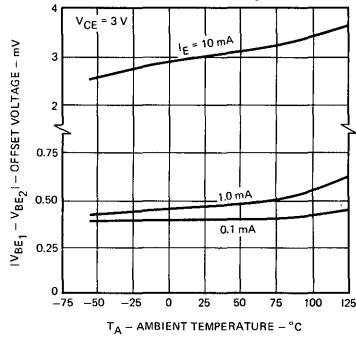


STATIC INPUT VOLTAGE FOR DARLINGTON PAIR Q3, Q4 AS A FUNCTION OF EMITTER CURRENT

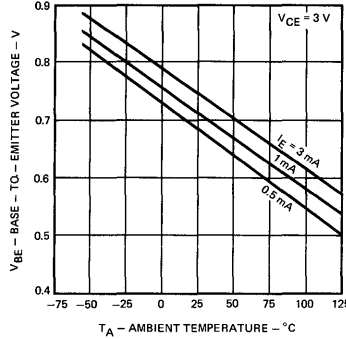


TYPICAL PERFORMANCE CURVES FOR 3018/3018A (Cont'd)

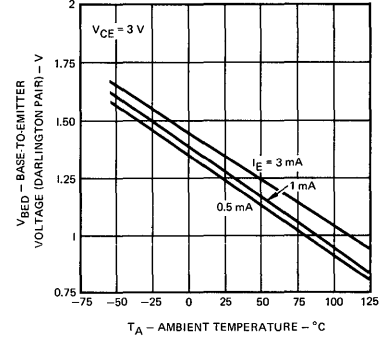
OFFSET VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE



BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE

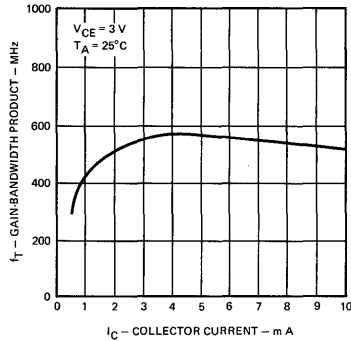


STATIC INPUT VOLTAGE FOR DARLINGTON PAIR (Q3, Q4) AS A FUNCTION OF AMBIENT TEMPERATURE

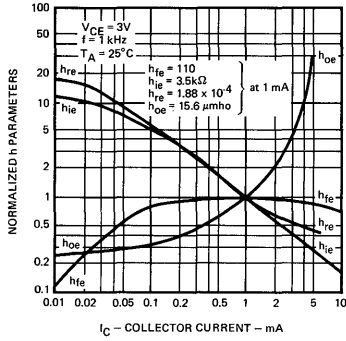


TYPICAL AC CHARACTERISTICS FOR EACH TRANSISTOR

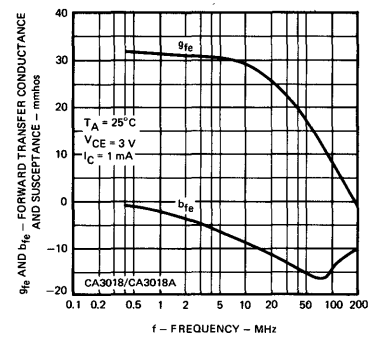
GAIN-BANDWIDTH PRODUCT (f_T) AS A FUNCTION OF COLLECTOR CURRENT



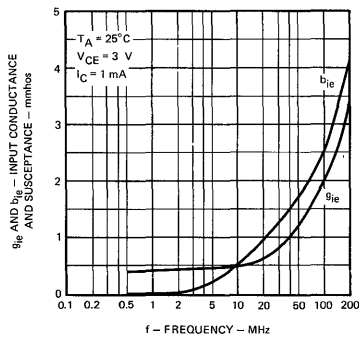
NORMALIZED h PARAMETERS AS A FUNCTION OF COLLECTOR CURRENT



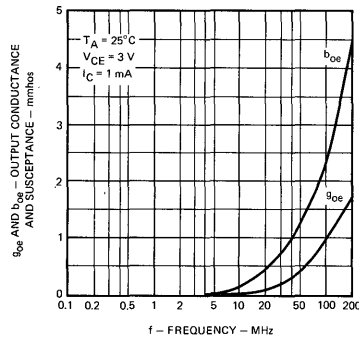
FORWARD TRANSFER ADMITTANCE (Y_{fe}) AS A FUNCTION OF FREQUENCY



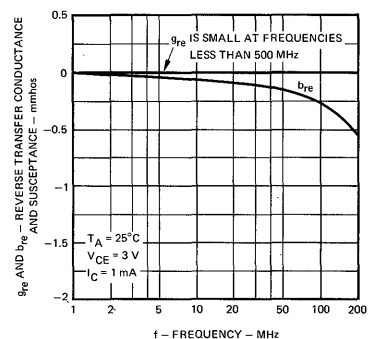
INPUT ADMITTANCE (Y_{ie}) AS A FUNCTION OF FREQUENCY



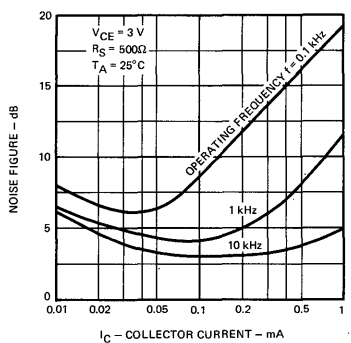
OUTPUT ADMITTANCE (Y_{oe}) AS A FUNCTION OF FREQUENCY



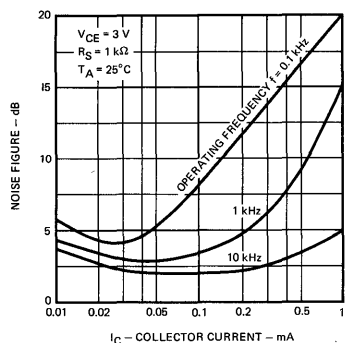
REVERSE TRANSFER ADMITTANCE (Y_{re}) AS A FUNCTION OF FREQUENCY



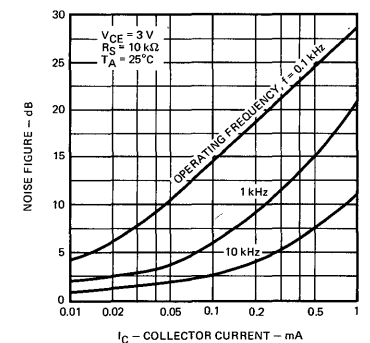
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

3019

- EXCELLENT DIODE MATCHING – 1 mV TYP.
- LOW REVERSE LEAKAGE CURRENT – 5 mA TYP.

APPLICATIONS

- Modulator
- Mixer
- Balanced Modulator
- Analog Switch
- Diode Gate for Chopper-Modulator Applications

ABSOLUTE MAXIMUM RATINGS

Power Dissipation		
For each Diode		20 mW
Total For Device		120 mW
Temperature Range		
Storage Temperature		–65°C to +200°C
Operating Temperature		–55°C to +125°C
Voltage Between Any Pin and Pin 7 (Note 1)		18 V

ELECTRICAL CHARACTERISTICS FOR 3019 (For each diode, $T_A = 25^\circ\text{C}$ unless otherwise specified)

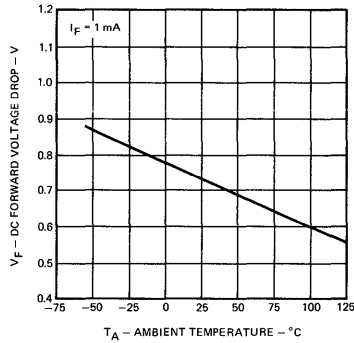
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC Forward Voltage Drop	V_F	DC Forward Current, $I_F = 1\text{ mA}$	–	0.73	0.78	V
DC Reverse Breakdown Voltage (Any Diode)	BV	DC Reverse Current, $I_R = -10\ \mu\text{A}$	4.0	6.0	–	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	BV_S	DC Reverse Current, $I_R = -10\ \mu\text{A}$	25	80	–	V
DC Reverse (Leakage) Current	I_R	DC Reverse Voltage, $V_R = -4\text{ V}$	–	0.0055	10	μA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	DC Reverse Voltage, $V_R = -4\text{ V}$	–	0.010	10	μA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$ V_{F1} - V_{F2} $	DC Forward Current, $I_F = 1\text{ mA}$	–	1.0	5.0	mV
Single Diode Capacitance	C_D	Frequency, $f = 1\text{ MHz}$ DC Reverse Voltage, $V_R = -2\text{ V}$ Frequency, $f = 1\text{ MHz}$	–	1.8	–	pF
Diode Quad-to-Substrate Capacitance	C_{DQ-I}	DC Reverse Voltage, V_R between Pins 2,5,6, or 8 of Diode Quad and Pin 7 (Substrate) = -2 V Pin 2 or 6 to Pin 7 Pin 5 or 8 to Pin 7	–	4.4 2.7	–	pF pF
Series Gate Switching Pedestal Voltage	V_S	See Figure 1	–	10	–	mV

NOTE

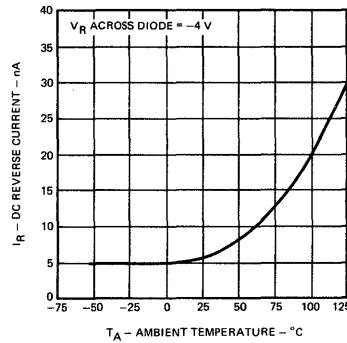
1. Substrate (Pin 7) must be connected to the most negative potential.

TYPICAL PERFORMANCE CURVES FOR 3019

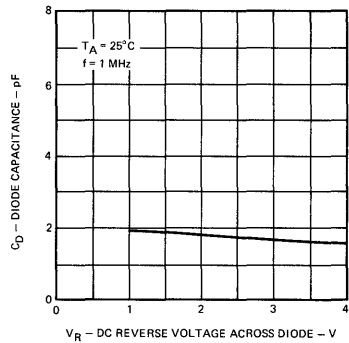
DC FORWARD VOLTAGE DROP (ANY DIODE) AS A FUNCTION OF TEMPERATURE



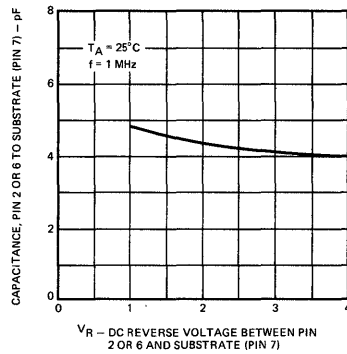
REVERSE (LEAKAGE) CURRENT (ANY DIODE) AS A FUNCTION OF TEMPERATURE



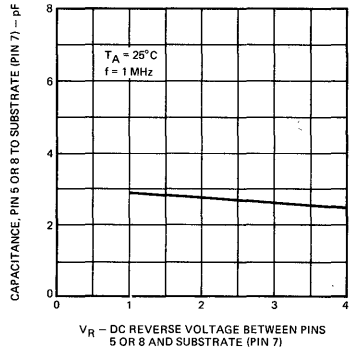
DIODE CAPACITANCE (ANY DIODE) AS A FUNCTION OF REVERSE VOLTAGE



DIODE QUAD-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



DIODE QUAD-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



SERIES GATE SWITCHING TEST SETUP

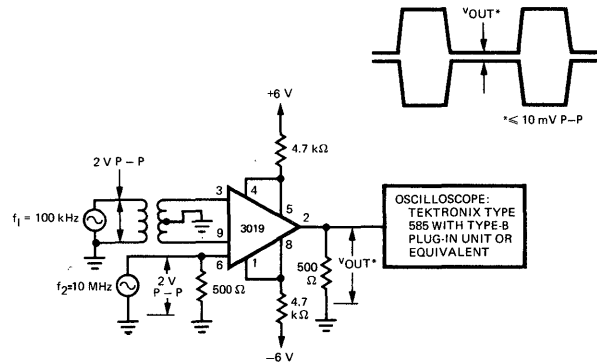


Fig. 1

FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

3026/3054

- **LOW INPUT OFFSET VOLTAGE** — ±5 mV
- **WIDEBAND OPERATION**
- **INDEPENDENTLY ACCESSIBLE INPUTS AND OUTPUTS**
- **TWO MATCHED DIFFERENTIAL AMPLIFIERS**

APPLICATIONS

- | | |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> • Dual Sense Amplifiers • Dual Schmitt Triggers • Multifunction Combinations — RF/Mixer/Oscillator; Converter/IF • IF Amplifiers (Differential and/or Cascode) • Product Detectors • Doubly Balanced Modulators and Demodulators | <ul style="list-style-type: none"> • Balanced Quadrature Detectors • Cascade Limiters • Synchronous Detectors • Pairs of Balanced Mixers • Synthesizer Mixers • Balanced (Push-Pull) Cascode Amplifiers |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

Power Dissipation (Note 1)	3054	3026
Any One Transistor	300 mW	300 mW
Total Package	600 mW	750 mW
Temperature Range		
Operating Temperature	-55°C to +125°C	0°C to +85°C
Storage Temperature	-65°C to +200°C	-25°C to +85°C
The following ratings apply for each transistor in the device		
Collector-to-Emitter Voltage, V _{CEO}		15 V
Collector-to-Base Voltage, V _{CBO}		20 V
Collector-to-Substrate Voltage, V _{CIO} (Note 2)		20 V
Emitter-to-Base Voltage, V _{EBO}		5 V
Collector Current, I _C		50 mA

ELECTRICAL CHARACTERISTICS FOR 3026/3054 (T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
For Each Differential Amplifier					
Input Offset Voltage	V _{IO}	—	0.45	5	mV
Input Offset Current	I _{IO}	—	0.3	2	μA
Input Bias Current	I _I	—	10	24	μA
Quiescent Operating Current Ratio	I _{C(Q1)} or I _{C(Q5)} I _{C(Q2)} or I _{C(Q6)}	—	0.98 to 1.02	—	—
Temperature Coefficient Magnitude of Input-Offset Voltage	Δ V _{IO} ΔT	—	1.1	—	μV/°C
For Each Transistor					
DC Forward Base-to-Emitter Voltage	V _{BE}	—	0.630	0.700	V
		—	0.715	0.800	
		—	0.750	0.850	
		—	0.800	0.900	
Temperature Coefficient of Base-to-Emitter Voltage	ΔV _{BE} ΔT	—	-1.9	—	mV/°C
Collector-Cutoff Current	I _{CBO}	—	0.002	100	nA
Collector-to-Emitter Breakdown Voltage	V _{(BR)CEO}	15	24	—	V
Collector-to-Base Breakdown Voltage	V _{(BR)CBO}	20	60	—	V
Collector-to-Substrate Breakdown Voltage	V _{(BR)CIO}	20	60	—	V
Emitter-to-Base Breakdown Voltage	V _{(BR)EBO}	5	7	—	V

NOTES

1. For T_A > 55°C; 3026 derates at 5 mW/°C and 3054 at 6.67 mW/°C
2. The collector of each transistor of the 3026 and 3054 is isolated from the substrate by an integral diode. Substrate must be connected to the most negative voltage to maintain normal operation.

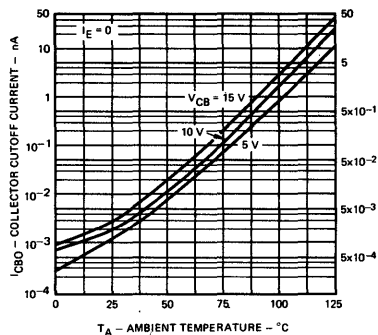
FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

ELECTRICAL CHARACTERISTICS FOR 3026/3054 (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

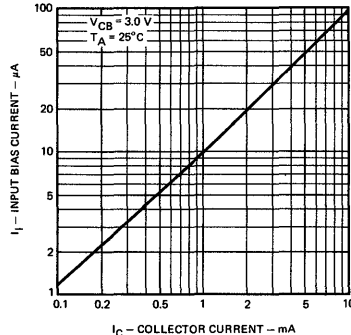
PARAMETER (See Test Circuits)		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Common-Mode Rejection Ratio for Each Amplifier	CMRR	$V_{CC} = 12\text{ V}$	—	100	—	dB
AGC Range, One Stage	AGC	$V_{EE} = -6\text{ V}$	—	75	—	dB
Voltage Gain, Single Stage Double-Ended Output	A_V	$V_X = -3.3\text{ V}$	—	32	—	dB
AGC Range, Two Stage	AGC	$f = 1\text{ kHz}$	—	105	—	dB
Voltage Gain, Two Stage Double-Ended Output	A_V		—	60	—	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (for Single Transistor)						
Forward Current-Transfer Ratio	h_{fe}		—	110	—	—
Short Circuit Input Resistance	h_{ie}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	3.5	—	$k\Omega$
Open Circuit Output Conductance	h_{oe}		—	15.6	—	μmho
Open Circuit Reverse Voltage-Transfer Ratio	h_{re}		—	1.8×10^{-4}	—	—
1 Noise Figure (for Single Transistor)	NF	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}$	—	3.25	—	dB
Gain-Bandwidth Product (for Single Transistor)	f_T	$V_{CE} = 3\text{ V}, I_C = 3\text{ mA}$	—	550	—	MHz
Admittance Characteristics; Differential Circuit Configuration: (for Each Amplifier)						
Forward Transfer Admittance	Y_{21}	$V_{CB} = 3\text{ V}$	—	$-20 + j0$	—	mmho
Input Admittance	Y_{11}	Each Collector	—	$0.22 + j0.1$	—	mmho
Output Admittance	Y_{22}	$I_C \approx 1.25\text{ mA}$	—	$0.01 + j0$	—	mmho
Reverse Transfer Admittance	Y_{12}	$f = 1\text{ MHz}$	—	$-0.003 + j0$	—	mmho
Admittance Characteristics; Cascode Circuit Configuration: (for Each Amplifier)						
Forward Transfer Admittance	Y_{21}	$V_{CB} = 3\text{ V}$	—	$68 - j0$	—	mmho
Input Admittance	Y_{11}	Total Stage	—	$0.55 + j0$	—	mmho
Output Admittance	Y_{22}	$I_C \approx 2.5\text{ mA}$	—	$0 + j0.02$	—	mmho
Reverse Transfer Admittance	Y_{12}	$f = 1\text{ MHz}$	—	$0.004 - j0.005$	—	μmho
Noise Figure	NF	$f = 100\text{ MHz}$	—	8	—	dB

TYPICAL PERFORMANCE CURVES FOR 3026/3054

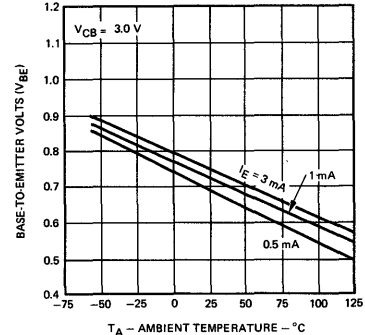
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



INPUT BIAS CURRENT CHARACTERISTIC AS A FUNCTION OF COLLECTOR CURRENT FOR EACH TRANSISTOR

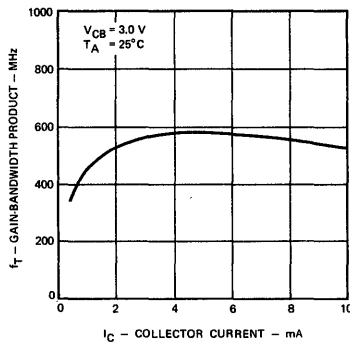


BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE

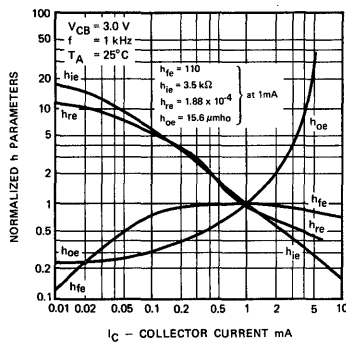


TYPICAL AC CHARACTERISTICS FOR EACH TRANSISTOR FOR 3026/3054

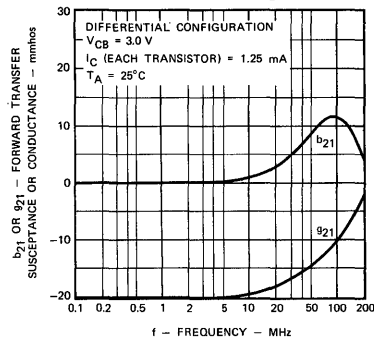
GAIN BANDWIDTH PRODUCT (f_T) AS A FUNCTION OF COLLECTOR CURRENT



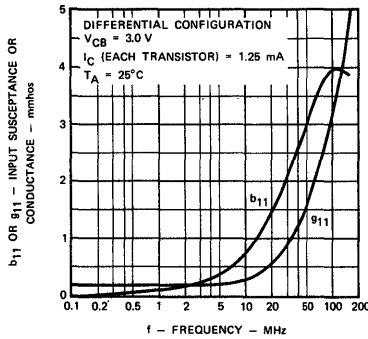
NORMALIZED h PARAMETER AS A FUNCTION OF COLLECTOR CURRENT FOR EACH TRANSISTOR



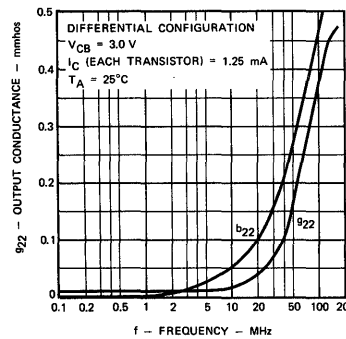
FORWARD TRANSFER ADMITTANCE (Y_{21}) AS A FUNCTION OF FREQUENCY



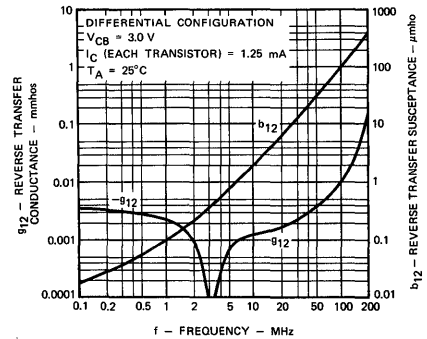
INPUT ADMITTANCE (Y_{11}) AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) AS A FUNCTION OF FREQUENCY

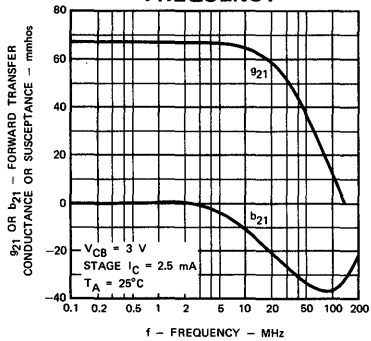


REVERSE TRANSFER ADMITTANCE (Y_{12}) AS A FUNCTION OF FREQUENCY

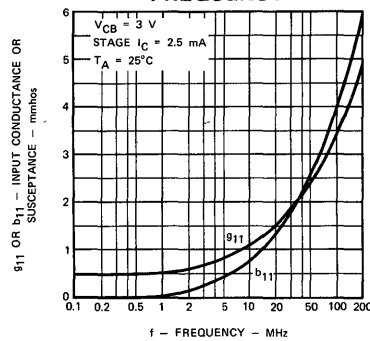


TYPICAL AC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER FOR 3026/3054

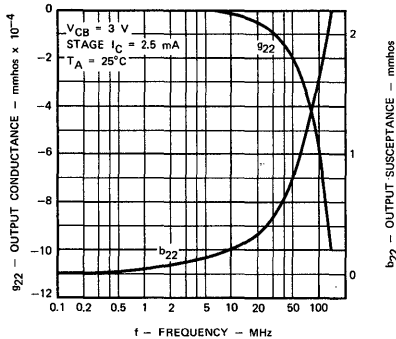
FORWARD TRANSFER ADMITTANCE (Y_{21}) AS A FUNCTION OF FREQUENCY



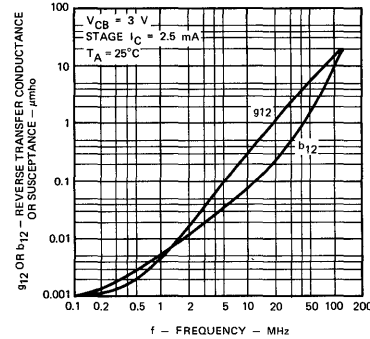
INPUT ADMITTANCE (Y_{11}) AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) AS A FUNCTION OF FREQUENCY

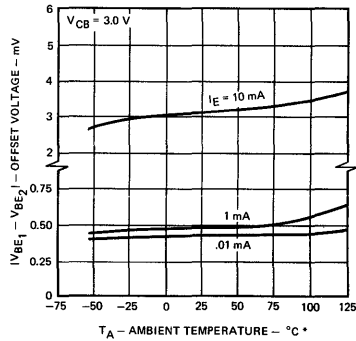


REVERSE TRANSFER ADMITTANCE (Y_{12}) AS A FUNCTION OF FREQUENCY

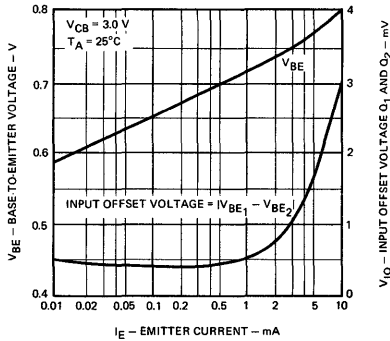


TYPICAL PERFORMANCE CURVES FOR 3026/3054 (Cont'd)

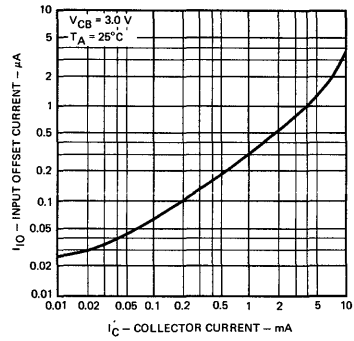
OFFSET VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE FOR DIFFERENTIAL PAIRS



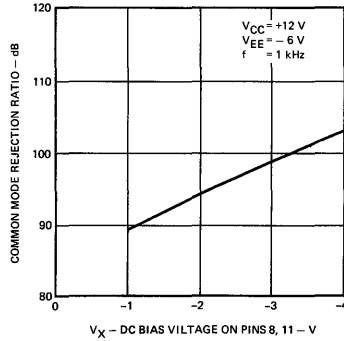
STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS AS A FUNCTION OF EMITTER CURRENT



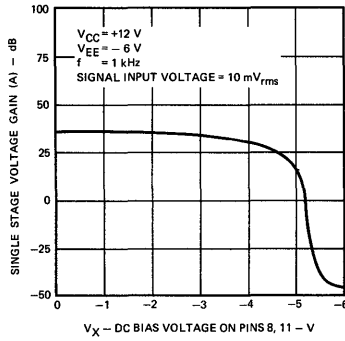
INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS AS A FUNCTION OF COLLECTOR CURRENT



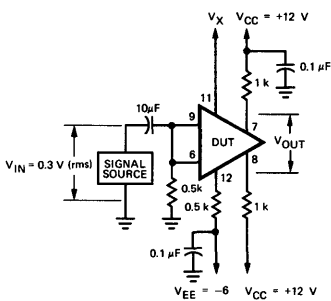
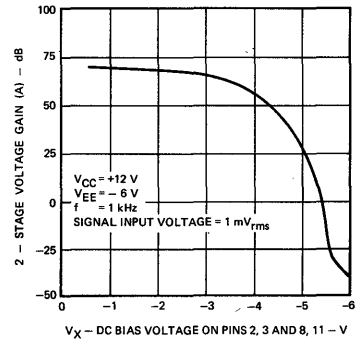
COMMON MODE REJECTION RATIO



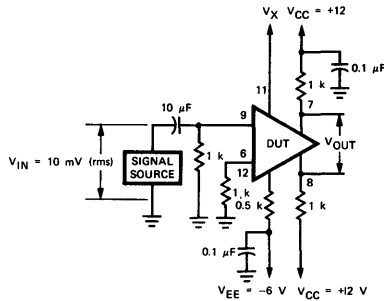
SINGLE STAGE VOLTAGE GAIN



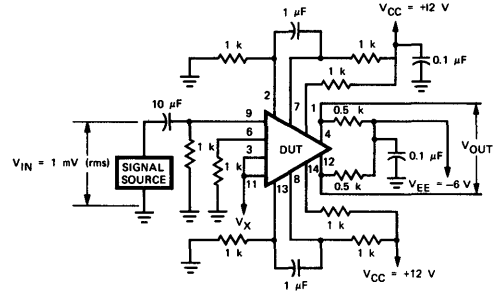
TWO-STAGE VOLTAGE GAIN



Test setup



Test setup



Test setup

Pin numbers are shown for 3054 (DIP) only.

FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

3036

- **MATCHED TRANSISTOR PERFORMANCE**
- **LOW NOISE PERFORMANCE**
- **200 MHz GAIN BANDWIDTH PRODUCT**

APPLICATIONS

- Stereo Phonograph Preamplifiers
- Low level Stereo and Single Channel Amplifier Stages
- Low noise, Emitter-follower Differential Amplifiers
- Operational Amplifier Drivers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

Power Dissipation		
Any One Transistor		300 mW
Total For Array		300 mW
Temperature Range		
Operating Temperature		-55°C to +125°C
Storage Temperature		-65°C to +200°C
The following ratings apply for each transistor in the array		
Collector-to-Emitter Voltage, V_{CE0}		15 V
Collector-to-Base Voltage, V_{CBO}		30 V
Emitter-to-Base Voltage, V_{EBO}		5 V
Collector Current, I_C		50 mA

ELECTRICAL CHARACTERISTICS FOR 3036 ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
For Each Transistor (Q_1, Q_2, Q_3, Q_4)						
Collector Cutoff Current	I_{CBO}	$V_{CB} = 5\text{ V}, I_E = 0$	-	-	0.5	μA
Collector Cutoff Current	I_{CEO}	$V_{CE} = 15\text{ V}, I_B = 0$	-	-	5.0	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{ mA}, I_B = 0$	15	20	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu\text{A}, I_E = 0$	30	44	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu\text{A}, I_C = 0$	5.0	6.0	-	V
For Either Input Transistor (Q_1 or Q_3)						
Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or $I_{C3} = 1\text{ mA}$	30	82	-	-
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)						
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or $I_{E4} = 10\ \mu\text{A}$	10	12.6	-	V
Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ } = 1 mA	1000	4540	-	-
For Each Input Transistor (Q_1 or Q_3)						
Short Circuit Forward Current-Transfer Ratio	h_{fe}		-	82	-	-
Short Circuit Input Resistance	h_{ie}	$f = 1\text{ kHz}$	-	2.6	-	$k\Omega$
Open Circuit Output Conductance	h_{oe}	I_{C1} or $I_{C3} = 1\text{ mA}$	-	7.0	-	μmho
Open Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	9.8×10^{-5}	-	-
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)						
Short Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	$f = 1\text{ kHz}$	-	1300	-	-
Short Circuit Input Resistance	$h_{ie(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ } = 1 mA	-	82	-	$k\Omega$
Open Circuit Output Conductance	$h_{oe(D)}$		-	108	-	μmho
Open Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$		-	2.7×10^{-3}	-	-
Noise Voltage	E_N	$f = 100\text{ Hz}$ $f = 1\text{ kHz}$ $f = 10\text{ kHz}$	-	0.2 0.05 0.012	3.0 0.3 0.1	$\frac{\mu\text{V (rms)}}{\sqrt{f(\text{Hz})}}$
For Either Input Transistor (Q_1 or Q_3)						
Forward Transfer Admittance	Y_{fe}		-	$0.68 + j 7.9$	-	mmho
Input Admittance (Output Short Circuited)	Y_{ie}	$f = 50\text{ MHz}$	-	$4.4 + j 5.95$	-	mmho
Output Admittance (Input Short Circuited)	Y_{oe}	I_{C1} or $I_{C3} = 2\text{ mA}$	-	$1.94 + j 2.64$	-	mmho
Reverse Transfer Admittance (Input Short-Circuited)	Y_{re}		-	Negligible	-	mmho
For Either Darlington Pair (Q_1, Q_2 , or Q_3, Q_4)						
Input Admittance (Output Short Circuited)	$Y_{ie(D)}$	$f = 50\text{ MHz}$	-	$1.71 + j 2.8$	-	mmho
Output Admittance (Input Short Circuited)	$Y_{oe(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ } = 2 mA	-	$3.96 + j 2.6$	-	mmho
Gain-Bandwidth Product	$f_T(D)$		150	200	-	MHz

FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

3039

- EXCELLENT DIODE MATCHING – 1 mV TYP.
- REVERSE RECOVERY TIME – 1 ns TYP.
- LOW DIODE CAPACITANCE – 0.65 pF @ $V_R = -2$ V

APPLICATIONS

- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (See note)		
Any One Diode Unit		100 mW
Total for Device		600 mW
Temperature Range		
Operating Temperature		–55° C to +125° C
Storage Temperature		–65° C to +200° C
Voltages and Currents		
Peak Inverse Voltage, PIV for: D ₁ - D ₅		5 V
	D ₆	0.5 V
Peak Diode-to-Substrate Voltage, V_{DI} for D ₁ - D ₅		+20, -1 V
(term. 1,4,5,8 or 12 to term. 10)		
DC Forward Current, I_F		25 mA
Peak Recurrent Forward Current, I_{fR}		100 mA
Peak Forward Surge Current, I_{fS} (surge)		100 mA

ELECTRICAL CHARACTERISTICS FOR 3039 (For each diode unit, $T_A = 25^\circ\text{C}$ unless otherwise specified)

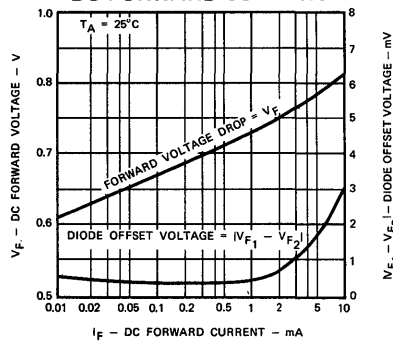
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
DC Forward Voltage Drop	V_F	$I_F = 50 \mu\text{A}$ 1 mA 3 mA 10 mA	–	0.65	0.69	V
			–	0.73	0.78	V
			–	0.76	0.80	V
			–	0.81	0.90	V
DC Reverse Breakdown Voltage	BV	$I_R = -10 \mu\text{A}$	5.0	7.0	–	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	BV_S	$I_R = -10 \mu\text{A}$	20	–	–	V
DC Reverse (Leakage) Current	I_R	$V_R = -4$ V	–	0.016	100	nA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	$V_R = -10$ V	–	0.022	100	nA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$ V_{F1} - V_{F2} $	$I_F = 1$ mA	–	0.5	5.0	mV
Temperature Coefficient of $ V_{F1} - V_{F2} $	$\frac{\Delta V_{F1} - V_{F2} }{\Delta T}$	$I_F = 1$ mA	–	1.0	–	$\mu\text{V}/^\circ\text{C}$
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	$I_F = 1$ mA	–	–1.9	–	$\text{mV}/^\circ\text{C}$
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	$I_F = 1$ mA	–	0.65	–	V
Reverse Recovery Time	t_{rr}	$I_F = 10$ mA, $I_R = 10$ mA	–	1.0	–	ns
Diode Resistance	R_D	$f = 1$ kHz, $I_F = 1$ mA	25	30	45	Ω
Diode Capacitance	C_D	$V_R = -2$ V, $I_F = 0$	–	0.65	–	pF
Diode-to-Substrate Capacitance	C_{DI}	$V_{DI} = +4$ V, $I_F = 0$	–	3.2	–	pF

NOTE: Derate at 5.7 mW/°C for $T_A > 55^\circ\text{C}$.

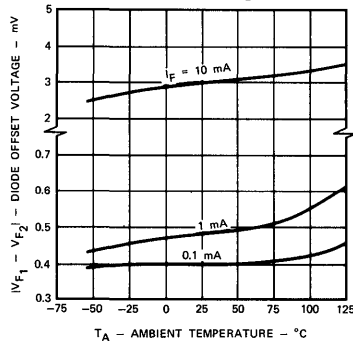
FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

TYPICAL PERFORMANCE CURVES FOR 3039

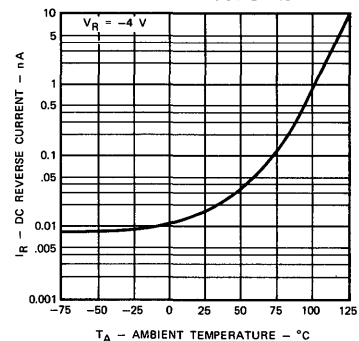
DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE AS A FUNCTION OF DC FORWARD CURRENT



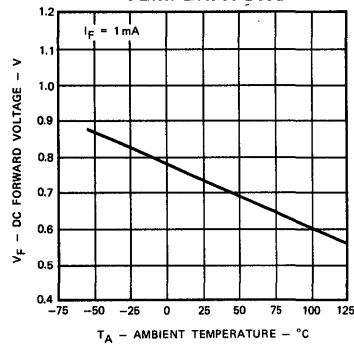
DIODE OFFSET VOLTAGE (ANY DIODE) AS A FUNCTION OF TEMPERATURE



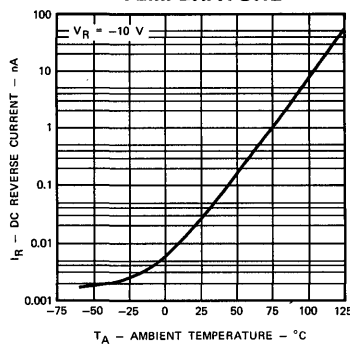
DC REVERSE (LEAKAGE) CURRENT (DIODES 1, 2, 3, 4, 5) AS A FUNCTION OF TEMPERATURE



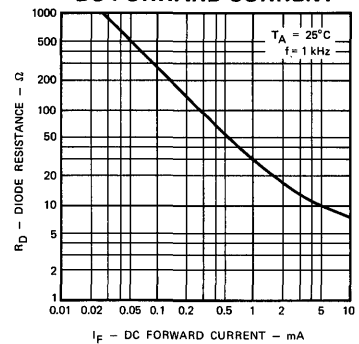
DC FORWARD VOLTAGE DROP (ANY DIODE) AS A FUNCTION OF TEMPERATURE



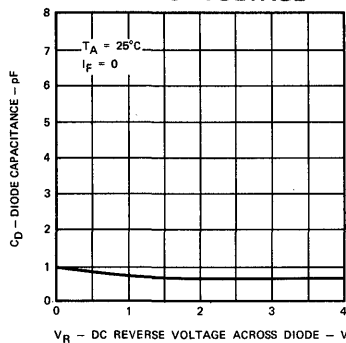
DC REVERSE (LEAKAGE) CURRENT BETWEEN DIODES (1, 2, 3, 4, 5) AND SUBSTRATE AS A FUNCTION OF TEMPERATURE



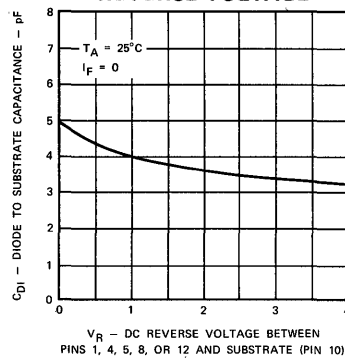
DIODE RESISTANCE (ANY DIODE) AS A FUNCTION OF DC FORWARD CURRENT



DIODE CAPACITANCE (DIODES 1, 2, 3, 4, 5) AS A FUNCTION OF REVERSE VOLTAGE



DIODE-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



FAIRCHILD LIC TRANSISTOR AND DIODE ARRAYS • 30XX SERIES

3045/3046/3086

- **LOW INPUT OFFSET VOLTAGE**
- **WIDEBAND OPERATION**
- **LOW NOISE**

APPLICATIONS

- General Use in all Types of Signal Processing Systems Operating Anywhere in the Frequency Range From DC to VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

Power Dissipation (Note 1)	3045		3046/3086	
	Each Transistor	Total Package	Each Transistor	Total Package
At $T_A = 25^\circ\text{C}$	300 mW	750 mW	300 mW	750 mW
At $T_A = 25^\circ\text{C}$ to 55°C			300 mW	750 mW
At $T_A = 25^\circ\text{C}$ to 75°C	300 mW	750 mW		
Voltages and Currents				
Collector-to-Emitter Voltage, V_{CEO}	15 V	—	15 V	—
Collector-to-Base Voltage, V_{CBO}	20 V	—	20 V	—
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V	—	20 V	—
Emitter-to-Base Voltage, V_{EBO}	5 V	—	5 V	—
Collector Current, I_C	50 mA	—	50 mA	—
Temperature Range				
Operating Temperature	-55°C to +125°C		(3046) 0°C to +85°C (3086) -40°C to +85°C	
Storage Temperature	-65°C to +200°C		-55°C to +125°C	

ELECTRICAL CHARACTERISTICS FOR 3045/3046/3086 ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	CONDITIONS	3045, 3046			3086			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$ $I_C = 10 \mu\text{A}, I_E = 0$	20	60	—	20	60	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$ $I_C = 1 \text{ mA}, I_B = 0$	15	24	—	15	24	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$ $I_C = 10 \mu\text{A}, I_{CI} = 0$	20	60	—	20	60	—	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$ $I_E = 10 \mu\text{A}, I_C = 0$	5.0	7.0	—	5.0	7.0	—	V
Collector Cutoff Current	I_{CBO} $V_{CB} = 10 \text{ V}, I_E = 0$	—	0.002	40	—	0.002	100	nA
Collector Cutoff Current	I_{CEO} $V_{CE} = 10 \text{ V}, I_B = 0$	—	See curve	0.5	—	See curve	5.0	μA
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE} $V_{CE} = 3 \text{ V}$ $I_C = 10 \text{ mA}$ $I_C = 1 \text{ mA}$ $I_C = 10 \mu\text{A}$	— 40 —	100 100 54	— — —	— 40 —	100 100 54	— — —	— — —
Input Offset Current for Matched Pair Q_1 and Q_2 $ I_{IO1} - I_{IO2} $	$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	—	0.3	2.0	—	—	—	μA
Base-to-Emitter Voltage	V_{BE} $V_{CE} = 3 \text{ V}$ $I_E = 1 \text{ mA}$ $I_E = 10 \text{ mA}$	— —	0.715 0.800	— —	— —	0.715 0.800	— —	V
Magnitude of Input Offset Voltage for Differential Pair $ V_{BE1} - V_{BE2} $	$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	—	0.45	5.0	—	—	—	mV
Magnitude of Input Offset Voltage for Isolated Transistors $ V_{BE3} - V_{BE4} $, $ V_{BE4} - V_{BE5} $, $ V_{BE5} - V_{BE3} $	$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	—	0.45	5.0	—	—	—	mV
Temperature Coefficient of Base-to-Emitter Voltage	ΔV_{BE} ΔT $V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	—	-1.9	—	—	-1.9	—	mV/°C
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$ $I_B = 1 \text{ mA}, I_C = 10 \text{ mA}$	—	0.23	—	—	0.23	—	V
Temperature Coefficient: Magnitude of Input-Offset Voltage	$ \Delta V_{10} $ ΔT $V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	—	1.1	—	—	—	—	$\mu\text{V}/^\circ\text{C}$

NOTES

1. 3046 and 3086 derate at 6.67 mW/°C for $T_A > 55^\circ\text{C}$, 3045 at 8 mW/°C for $T_A > 75^\circ\text{C}$.
2. Substrate (Pin 13) must be connected to the most negative voltage to maintain normal operation.

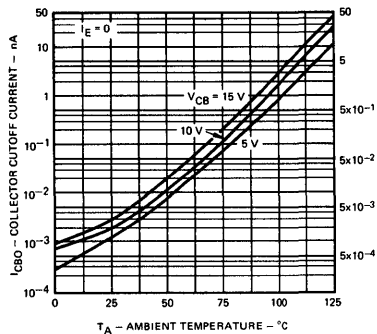
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ELECTRICAL CHARACTERISTICS FOR 3045/3046/3086 ($T_A = 25^\circ\text{C}$ unless otherwise specified) (Continued)

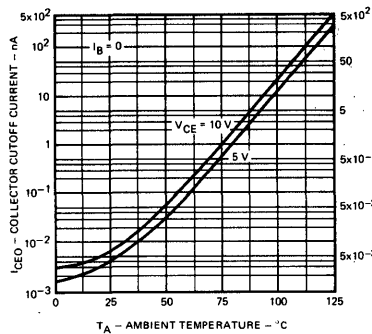
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Low Frequency Noise Figure	NF	$f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 100\mu\text{A}$ $R_S = 1\text{k}\Omega$	—	3.25	—	dB	
Low Frequency, Small-Signal Equivalent-Circuit Characteristics:							
Forward Current-Transfer Ratio	h_{fe}	$f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	—	110	—	k Ω	
Short-Circuit Input Resistance	h_{ie}		3.5	—	—		
Open-Circuit Output Conductance	h_{oe}		15.6	—	—		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		1.8×10^{-4}	—	—		—
Admittance Characteristics:							
Forward Transfer Admittance	Y_{fe}	$f = 1\text{MHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	—	$31 - j1.5$	—	—	
Input Admittance	Y_{ie}		$0.3 + j0.04$	—	—	—	
Output Admittance	Y_{oe}		$0.001 + j0.03$	—	—	—	
Reverse Transfer Admittance	Y_{re}		See curve	—	—	—	
Gain-Bandwidth Product	f_T	$V_{CE} = 3\text{V}, I_C = 3\text{mA}$	300	550	—	—	
Emitter-to-Base Capacitance	C_{EB}	$V_{EB} = 3\text{V}, I_E = 0$	—	0.6	—	pF	
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 3\text{V}, I_C = 0$	—	0.58	—	pF	
Collector-to-Substrate Capacitance	C_{CI}	$V_{CS} = 3\text{V}, I_C = 0$	—	2.8	—	pF	

TYPICAL PERFORMANCE CURVES FOR 3045/3046/3086

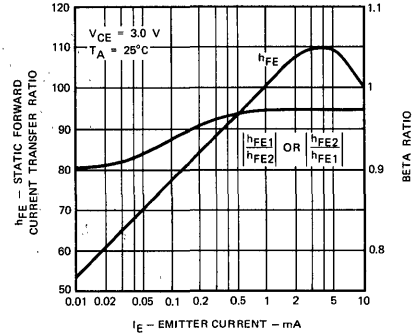
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



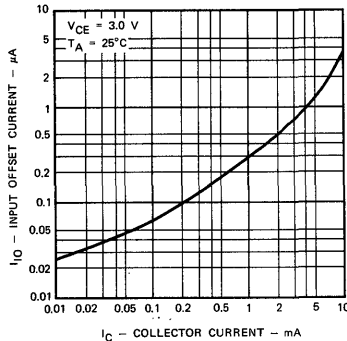
COLLECTOR-TO-EMITTER CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



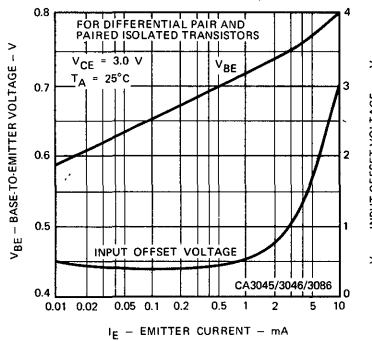
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q1, Q2 AS A FUNCTION OF EMITTER CURRENT



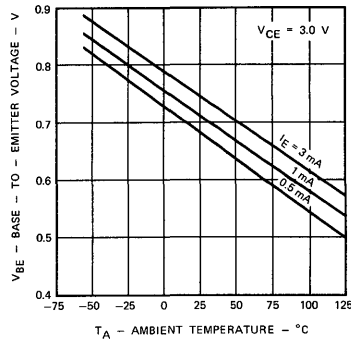
INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q1, Q2 AS A FUNCTION OF COLLECTOR CURRENT



STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE AS A FUNCTION OF EMITTER CURRENT



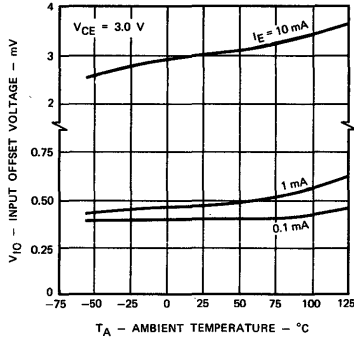
BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



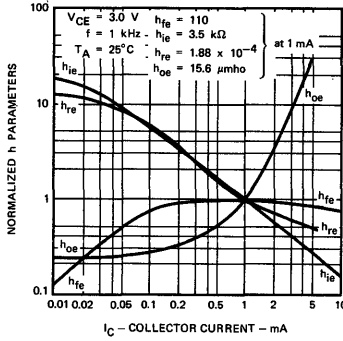
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TYPICAL PERFORMANCE CURVES FOR 3045/3046/3086 (Cont'd)

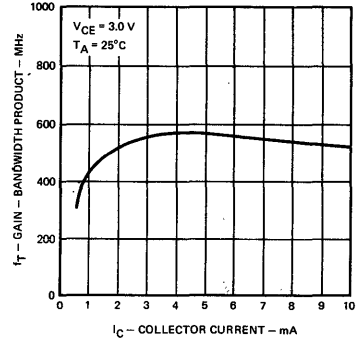
INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS AS A FUNCTION OF AMBIENT TEMPERATURE



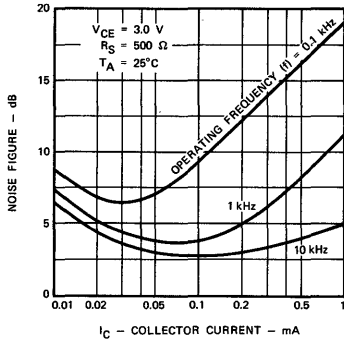
NORMALIZED h PARAMETERS AS A FUNCTION OF COLLECTOR CURRENT



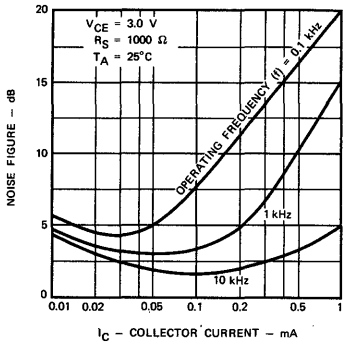
GAIN-BANDWIDTH PRODUCT AS A FUNCTION OF COLLECTOR CURRENT



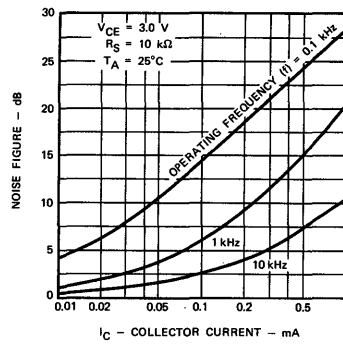
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



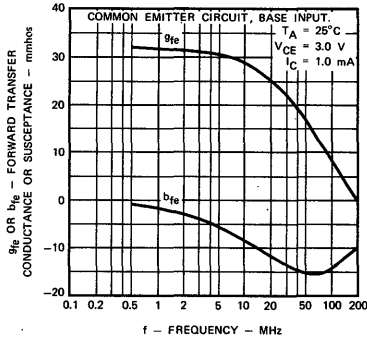
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



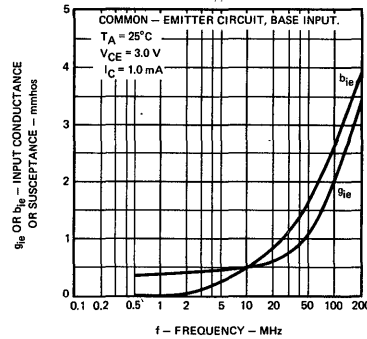
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



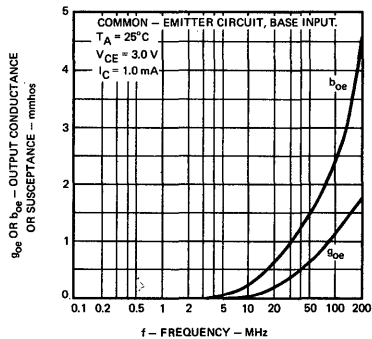
FORWARD TRANSFER ADMITTANCE AS A FUNCTION OF FREQUENCY



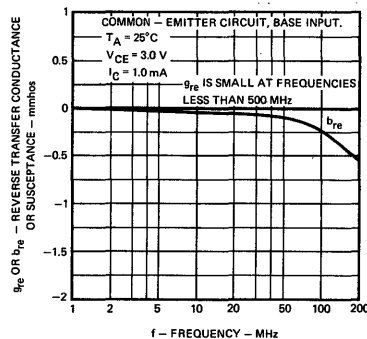
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



REVERSE TRANSFER ADMITTANCE AS A FUNCTION OF FREQUENCY



SH3002

SPDT ANALOG SWITCH

FAIRCHILD INTEGRATED MICROSYSTEMS

GENERAL DESCRIPTION — The SH3002 is a SPDT analog switch which consists of a monolithic TTL type gate driving a pair of MOS switches.

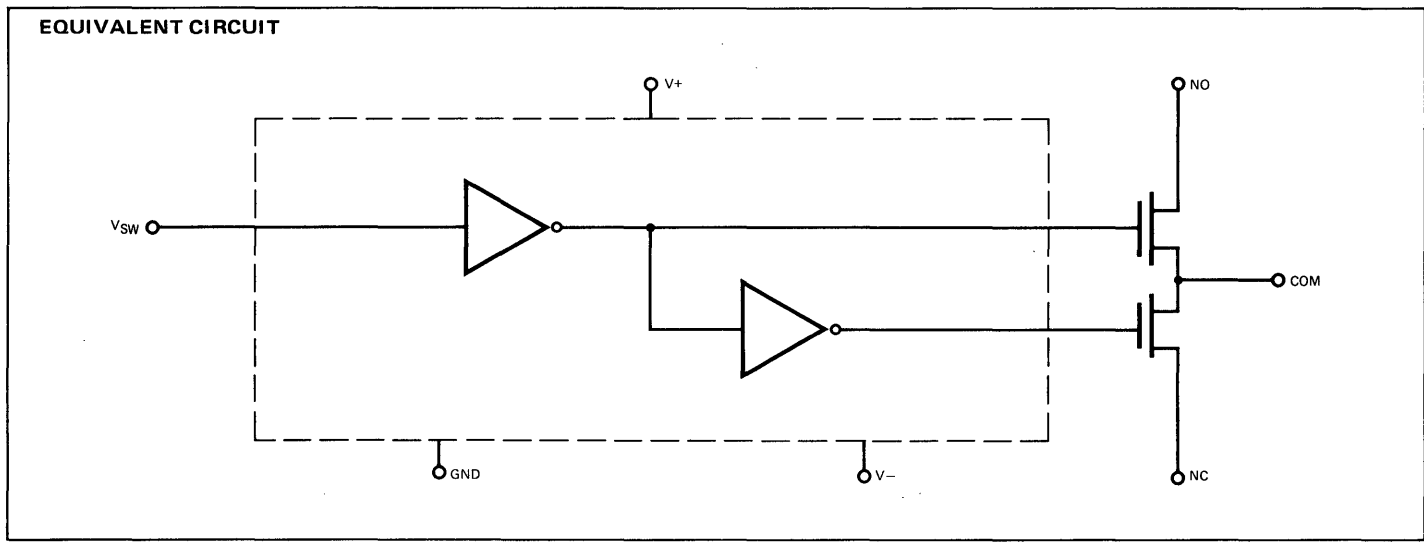
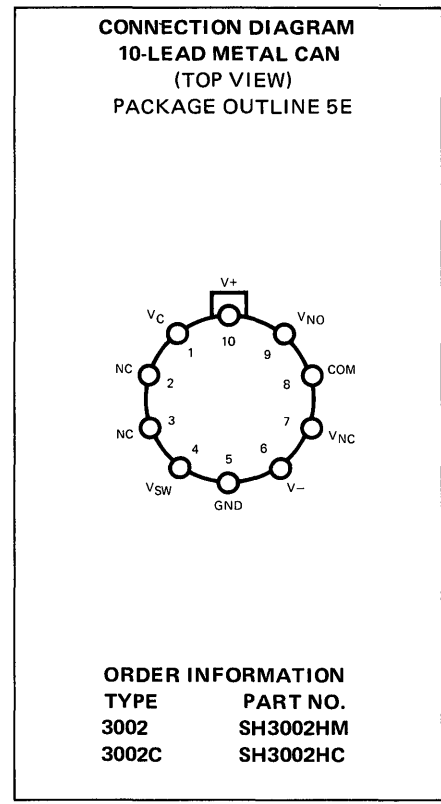
- **INPUTS TTL COMPATIBLE**
- **LOW FEED THROUGH SPIKES ON THE OUTPUT**
- **TYPICAL t_{ON} 75 ns**

APPLICATIONS

- Series Shunt Choppers
- A/D Conversion Single Pole Double Throw Relays
- Multiplexing
- Scanning

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Temperature	Military (3002) -55°C to +125°C Commercial (3002C) 0°C to + 70°C
Maximum Power Dissipation	
at 25°C Case	500 mW
at 25°C Ambient	350 mW
Maximum Voltages and Current	
V _{COM} (Pin 8)	±12 V
V _{NO} , V _{NC} (Pins 7 & 9)	±12 V
V ⁺ (Pin 10)	+11 V
V ⁻ (Pin 6)	-22 V
I _{NO} , I _{NC}	10 mA
V _{switch} (Pin 4)	±6 V



3002

ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
High Switch Drive Voltage	V _{SWH}	T _A = 25°C	1.9			V
High Switch Drive Voltage	V _{SWH}	T _A = -55°C	2.2			V
High Switch Drive Voltage	V _{SWH}	T _A = 125°C	1.6			V
Low Switch Drive Voltage	V _{SWL}	T _A = 25°C			1.1	V
Low Switch Drive Voltage	V _{SWL}	T _A = -55°C			1.5	V
Low Switch Drive Voltage	V _{SWL}	T _A = 125°C			0.5	V
High Switch Input Current	I _{SWH}	V _{SW} = 5.0 V, V ₁₀ = 10 V, V ₆ = -22 V			2.5	μA
Low Switch Input Current	I _{SWL}	V _{SW} = 0 V, V ₁₀ = 11 V, V ₆ = -20 V			-1.5	mA
Channel "On" Resistance	R _{ON/CHANNEL}	V _g = GND, I ₇ or I ₉ = 100 μA		140	200	Ω
Channel "Off" Leakage	I _{OFF}	V _g = ±10 V, V ₇ = ±10 V, V ₉ = ±10 V, T _A = 25°C			25	nA
		V _g = ±10 V, V ₇ = ±10 V, V ₉ = ±10 V, T _A = 125°C			1.0	μA
Analog Peak Signal Input	V _{IN}				±10	V
Positive Supply Current	I ₁₀	V _{SW} = 4.0 V, V ₁₀ = 11 V, V ₆ = -22 V			8.0	mA
Positive Supply Current	I ₁₀	V _{SW} = 0 V, V ₁₀ = 11 V, V ₆ = -22 V			8.0	mA
Negative Supply Current	I ₆	V _{SW} = 4.0 V, V ₁₀ = 11 V, V ₆ = -22 V			6.5	mA
Turn-on Time (Pin 9)	t _{on+}	See Fig. 1 and 2		75	150	ns
Turn-off Time (Pin 7)	t _{off+}	See Fig. 1 and 2		575	650	ns
Turn-on Time (Pin 9)	t _{on-}	See Fig. 1 and 3		75	160	ns
Turn-off Time (Pin 7)	t _{off-}	See Fig. 1 and 3		260	340	ns
Turn-off Time (Pin 9)	t _{off+}	See Fig. 1 and 2		1.6	1.9	μs
Turn-on Time (Pin 7)	t _{on+}	See Fig. 1 and 2		1.35	2.0	μs
Turn-off Time (Pin 9)	t _{off-}	See Fig. 1 and 3		1.5	1.7	μs
Turn-on Time (Pin 7)	t _{on-}	See Fig. 1 and 3		1.6	2.5	μs

SWITCHING TEST CIRCUIT

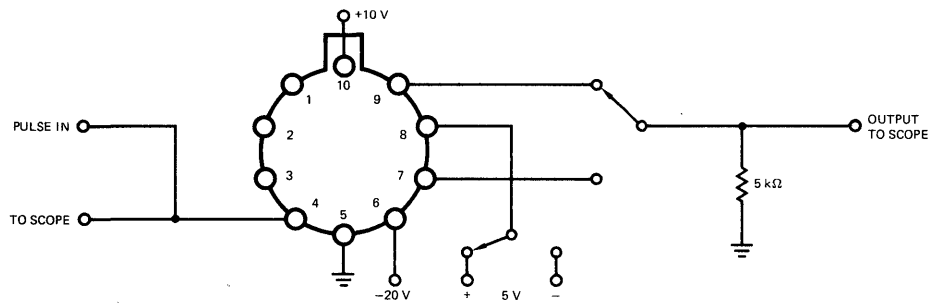


Fig. 1

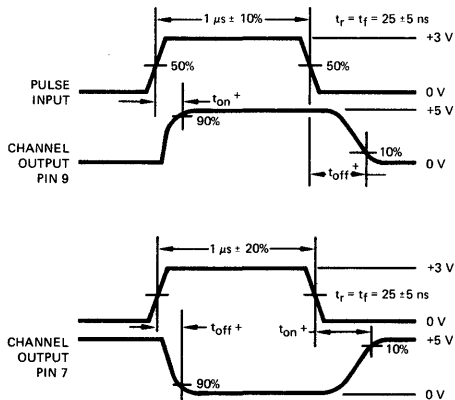


Fig. 2 (with +5 V on Pin 8)

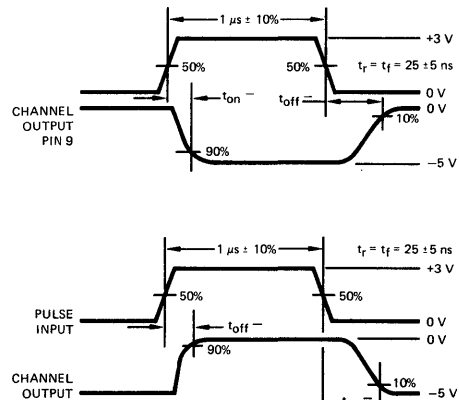


Fig. 3 (with -5 V on Pin 8)

3002C

ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
High Switch Drive Voltage	V _{SWH}	T _A = 25°C	1.9			V
High Switch Drive Voltage	V _{SWH}	T _A = 0°C	2.0			V
High Switch Drive Voltage	V _{SWH}	T _A = 70°C	1.7			V
Low Switch Drive Voltage	V _{SWL}	T _A = 25°C			1.1	V
Low Switch Drive Voltage	V _{SWL}	T _A = 0°C			1.3	V
Low Switch Drive Voltage	V _{SWL}	T _A = 70°C			0.8	V
High Switch Input Current	I _{SWH}	V _{SW} = 5.0 V, V ₁₀ = 10 V, V ₆ = -22 V			2.5	μA
Low Switch Input Current	I _{SWL}	V _{SW} = 0 V, V ₁₀ = 11 V, V ₆ = -20 V			-1.5	mA
Channel "On" Resistance	R _{ON/CHANNEL}	V ₈ = GND, I ₇ or I ₉ = 100 μA		140	200	Ω
Channel "Off" Leakage	I _{OFF}	V ₈ = ±10 V, V ₇ = ±10 V, V ₉ = ±10 V, T _A = 25°C			25	nA
		V ₈ = ±10 V, V ₇ = ±10 V, V ₉ = ±10 V, T _A = 100°C			1.0	μA
Analog Peak Signal Input	V _{IN}				±10	V
Positive Supply Current	I ₁₀	V _{SW} = 4.0 V, V ₁₀ = 11 V, V ₆ = -22 V			8.0	mA
Positive Supply Current	I ₁₀	V _{SW} = 0 V, V ₁₀ = 11 V, V ₆ = -22 V			8.0	mA
Negative Supply Current	I ₆	V _{SW} = 4.0 V, V ₁₀ = 11 V, V ₆ = -22 V			6.5	mA
Turn-on Time (Pin 9)	t _{on+}	See Fig. 1 and 2		75	150	ns
Turn-off Time (Pin 7)	t _{off+}	See Fig. 1 and 2		675	760	ns
Turn-on Time (Pin 9)	t _{on-}	See Fig. 1 and 3		75	160	ns
Turn-off Time (Pin 7)	t _{off-}	See Fig. 1 and 3		320	400	ns
Turn-off Time (Pin 9)	t _{off+}	See Fig. 1 and 2		1.6	1.9	μs
Turn-on Time (Pin 7)	t _{on+}	See Fig. 1 and 2		1.35	2.0	μs
Turn-off Time (Pin 9)	t _{off-}	See Fig. 1 and 3		1.5	1.7	μs
Turn-on Time (Pin 7)	t _{on-}	See Fig. 1 and 3		1.6	2.5	μs

GLOSSARY

TRANSISTOR/DIODE ARRAYS/ANALOG SWITCHES

Admittance Characteristics, Forward Transfer Admittance — The ratio of the output current to the input voltage with the output short-circuited.

Admittance Characteristics, Input Admittance — The ratio of the input current to the input voltage with the output short-circuited.

Admittance Characteristics, Output Admittance — The ratio of the output current to the output voltage with the input short-circuited.

Admittance Characteristics, Reverse Transfer Admittance — The ratio of the input current to the output voltage with the input short-circuited.

AGC Range — The amount by which the maximum gain can be reduced.

Average Input Bias Current — The average value of the input bias currents.

Broadband Noise — The equivalent value of the device noise over its flat-band frequency range.

Common-Mode Rejection Ratio — The ratio of the change of input offset voltage to the change in input common mode voltage causing it.

DC Forward Voltage Drop — The dc voltage measured between anode and cathode at a specified forward current.

DC Reverse (Leakage) Current — The leakage current flowing from cathode to anode at some specified reverse bias voltage.

Diode Capacitance — The equivalent anode to cathode capacitance for a specified bias condition.

Diode Resistance — The anode to cathode resistance measured at some specified bias current.

Gain Bandwidth Product — The frequency at which the small signal ac gain of the device reduces to unity.

High Frequency Current Gain — The small signal ac current gain at a specified frequency.

IF Noise Figure — The noise figure measured at a specified low frequency below the frequency range where the device noise figure is essentially flat.

Input Offset Current — The difference in input currents required to give equal output currents from a matched pair of devices.

Input Offset Current Drift — The change in input offset current produced by variations in time, voltage or temperature.

Input Offset Voltage — The input voltage differential required to give equal output currents from a matched pair of devices.

Input Offset Voltage Drift — The change in input offset voltage produced by variations in time, voltage or temperature.

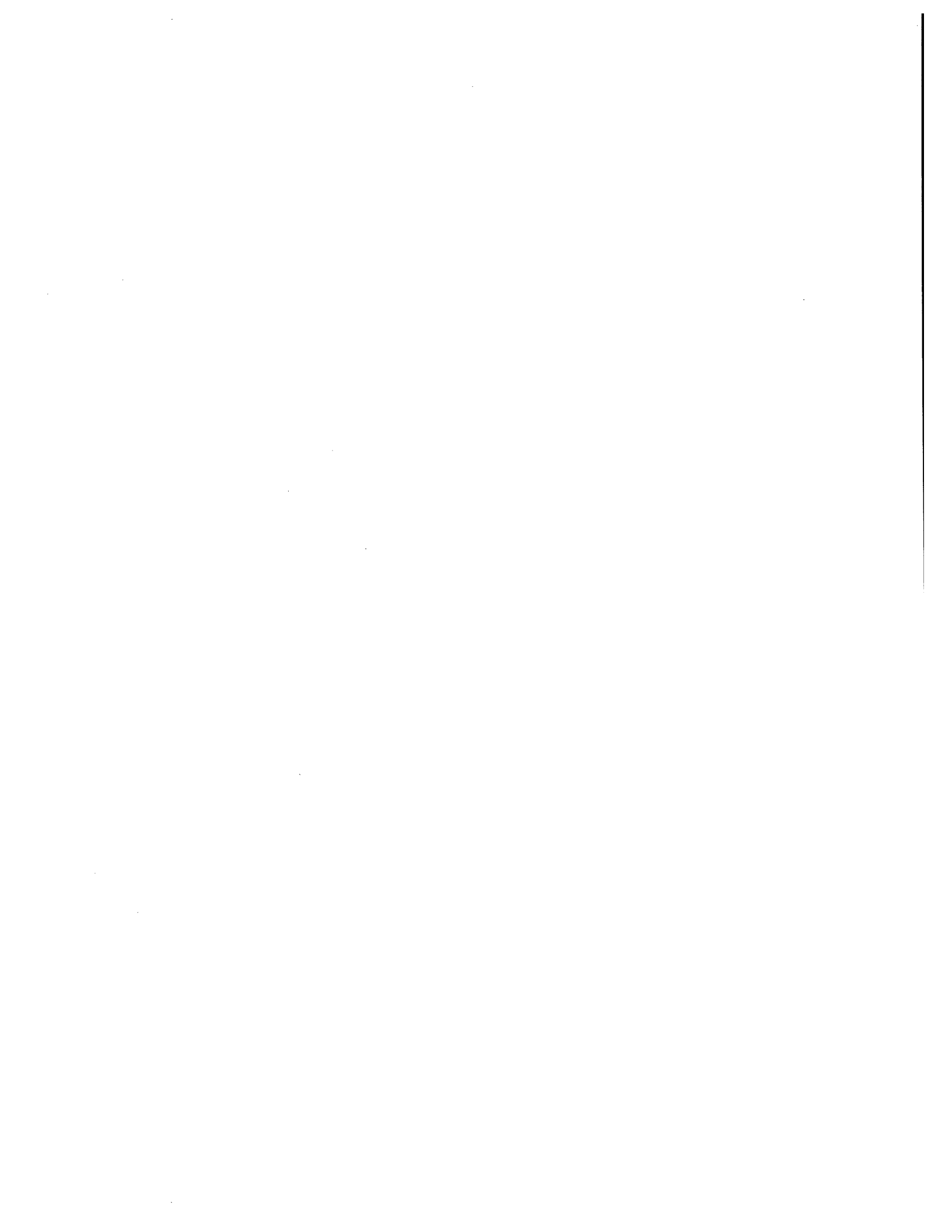
Long Term Drift — The change in a specified parameter with respect to time.

Noise Figure — The common logarithm of the ratio of the input signal to noise ratio to the output signal to noise ratio.

Reverse Recovery Time — The time taken for the reverse recovery current to fall to a specified value after removal of the reverse bias under specified conditions.

Static Forward Current Transfer Ratio — The ratio of the dc collector current to the corresponding dc base current.

Supply Voltage Rejection Ratio — The ratio of the change in input offset voltage to the change in supply voltage causing it.



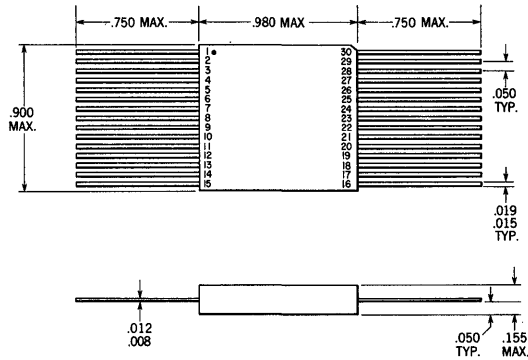
LINEAR LINEAR LINEAR LINEAR LINEAR LINEAR LINEAR LINEAR

CONTENTS AND SECTION SELECTOR

PACKAGE OUTLINES	9
ORDER INFORMATION	10
MIL-M-38510/MIL-STD-883	11
DICE	12
INDUSTRY CROSS-REFERENCE GUIDE	13
APPLICATION INFORMATION	14

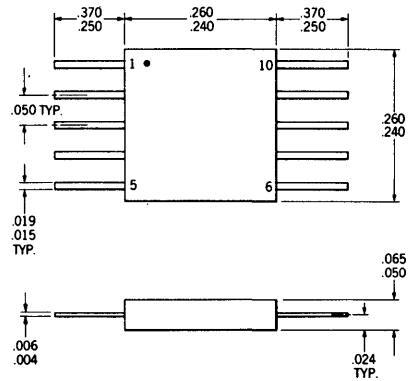
PACKAGE OUTLINES

30-Lead Flatpak (F) 2B



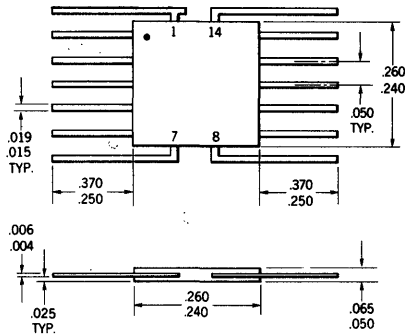
NOTES:
 All dimensions in inches
 Leads are gold-plated kovar
 Package weight is 5.0 grams
 Package material is alumina

JEDEC (TO-91) 10-Lead Cerpak (F) 3F



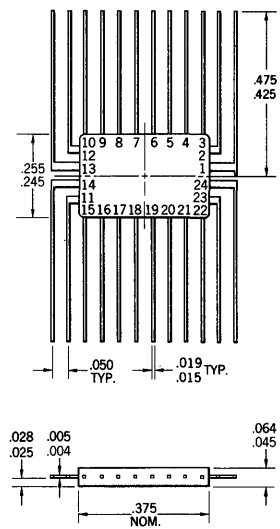
NOTES
 All dimensions in inches
 Leads are gold-plated kovar
 Package weight is 0.26 gram

JEDEC (TO-86) 14-Lead Cerpak (F) 3I



NOTES
 All dimensions in inches
 Leads are gold-plated kovar
 Package weight is 0.26 gram
 Lead 1 orientation may be either tab or dot

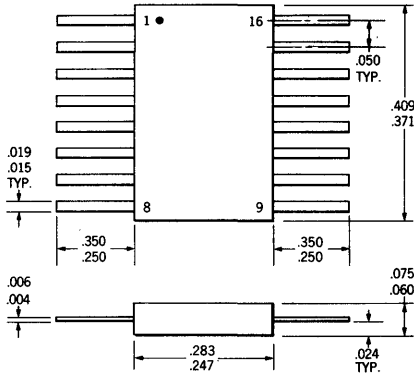
24-Lead Flatpak (F) 3M



NOTES
 All dimensions in inches
 Leads are gold-plated kovar
 Package weight is 0.8 gram

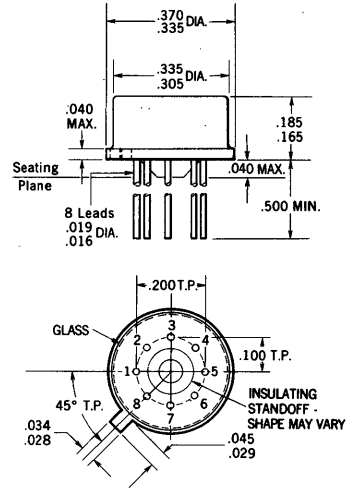
PACKAGE OUTLINES

(F)4L
16-Lead Cerpak



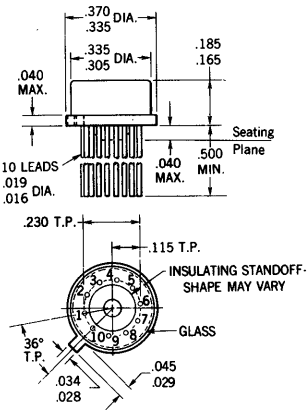
NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

(H)5B
JEDEC (TO-99)



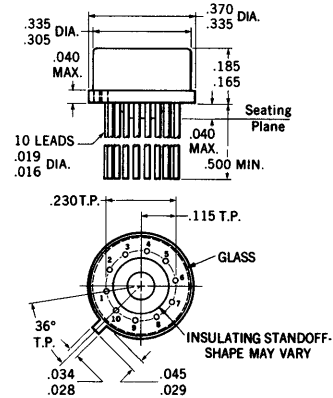
NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 gram
Seven leads through, lead No. 4 connected to case
15 mil kovar header

(H)5E
JEDEC (TO-100)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Ten leads through
15 mil kovar header

(H)5F
JEDEC (TO-100)

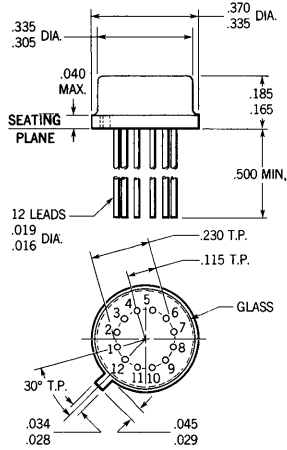


NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Nine leads through, lead No. 5 is connected to case
15 mil kovar header

PACKAGE OUTLINES

(H)5G

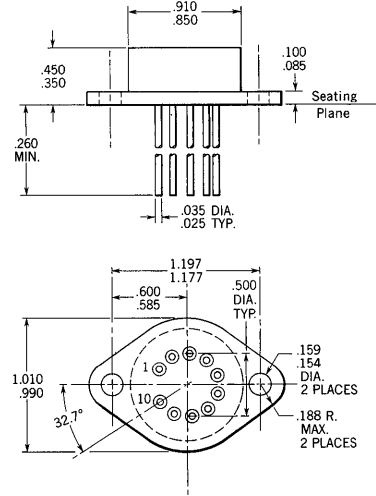
JEDEC (TO-101)
without standoff



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.03 gram
15 mil kovar header

(K)5H

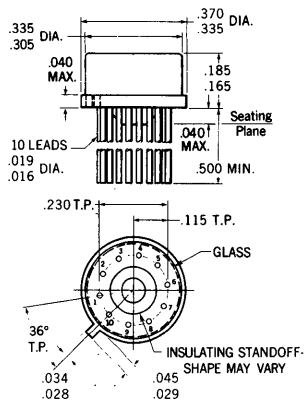
JEDEC (TO-3)
except 10 pins on 11 pin circle



NOTES
All dimensions in inches

(H)5U

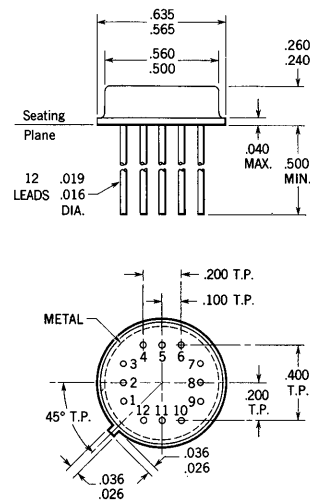
JEDEC (TO-100)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
High thermal resistance package
Ten leads through
15 mil kovar header

(H)5V

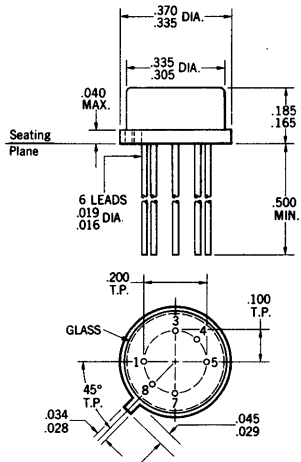
JEDEC (TO-8)



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 2.2 grams

PACKAGE OUTLINES

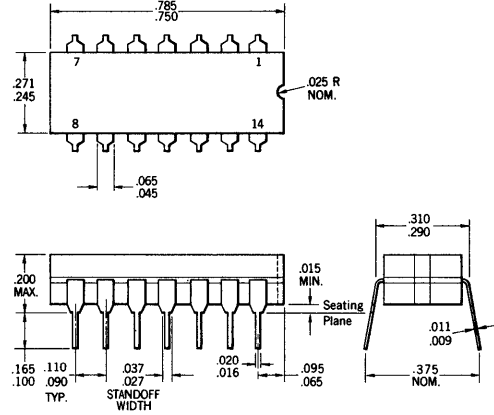
(H)5Z
JEDEC (TO-78)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.95 gram
50 mil kovar header

(D)6A

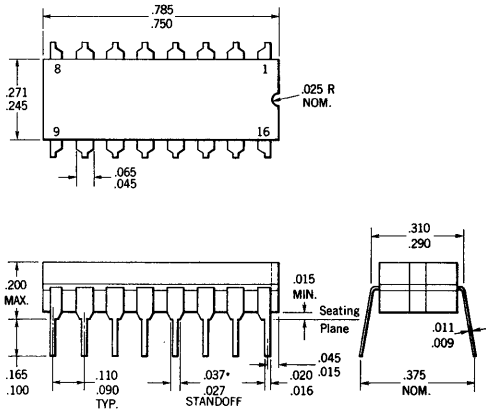
JEDEC (TO-116)
14-Lead Hermetic Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

(D)6B

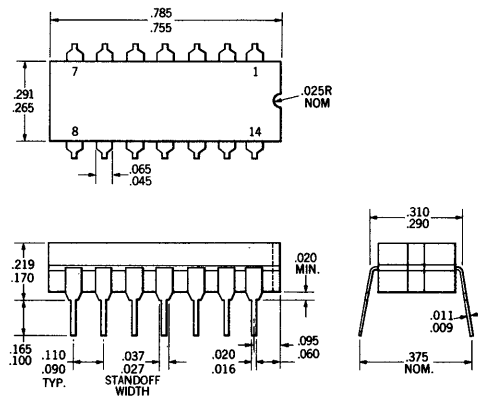
16-Lead Hermetic Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .027/.037 dimension does not apply to the corner leads

(D)7A

14-Lead Hermetic Dual In-line

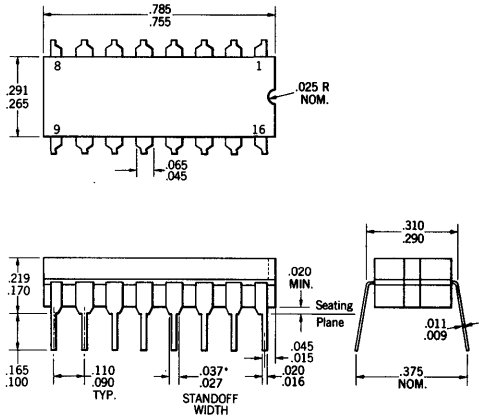


NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
JEDEC TO-116 except for package width

PACKAGE OUTLINES

(D)7B

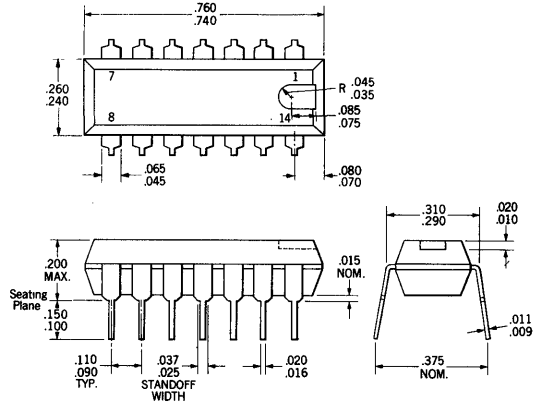
16-Lead Hermetic Dual In-line



NOTES
 All dimensions in inches
 Leads are intended for insertion in hole rows on .300" centers
 They are purposely shipped with "positive" misalignment to facilitate insertion
 Board-drilling dimensions should equal your practice for .020 inch diameter lead
 Leads are tin-plated kovar
 Package weight is 2.2 grams
 The .037/.027 dimension does not apply to the corner leads

(P)9A

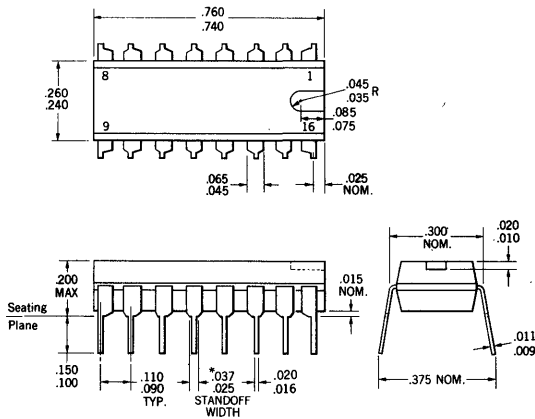
JEDEC (TO-116)
 14-Lead Molded Dual In-line



NOTES
 All dimensions in inches
 Leads are intended for insertion in hole rows on .300" centers
 They are purposely shipped with "positive" misalignment to facilitate insertion
 Board-drilling dimensions should equal your practice for .020 inch diameter lead
 Leads are tin-plated kovar
 Package weight is 0.9 gram

(P)9B

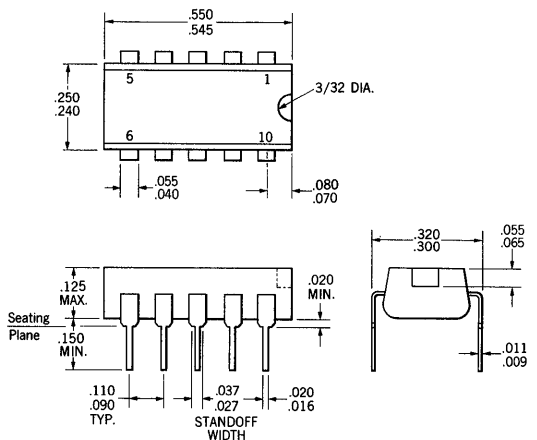
16-Lead Molded Dual In-line



NOTES
 All dimensions in inches
 Leads are intended for insertion in hole rows on .300" centers
 They are purposely shipped with "positive" misalignment to facilitate insertion
 Board-drilling dimensions should equal your practice for .020 inch diameter lead
 Leads are tin-plated kovar
 Package weight is 0.9 gram
 *The .037/.027 dimension does not apply to the corner leads

(P)9F

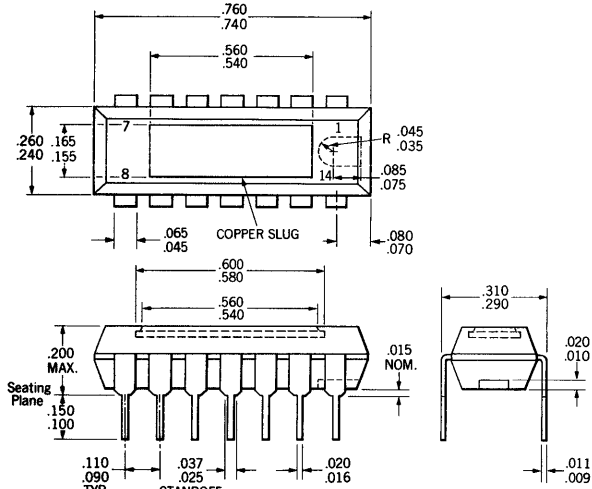
10-Lead Molded Dual In-line



NOTES:
 All dimensions in inches
 Board-drilling dimensions should equal your practice for .020 inch diameter lead
 Leads are gold-plated kovar
 Package weight is 0.65 gram

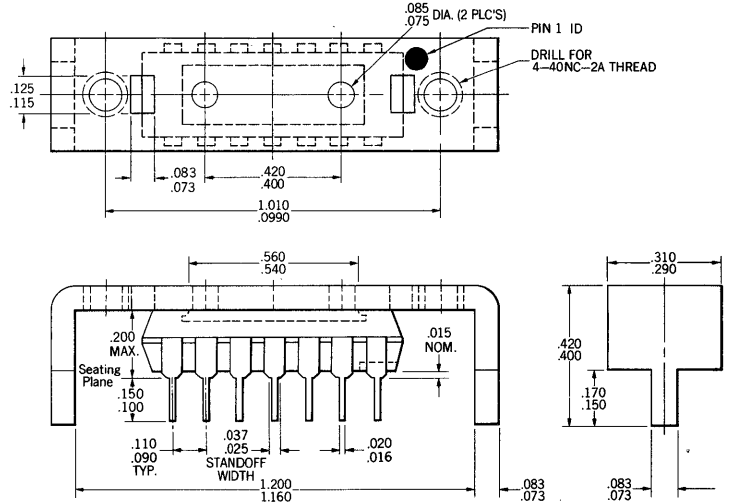
PACKAGE OUTLINES

(AP)9H
Dual In-line Power Package (DIPP)



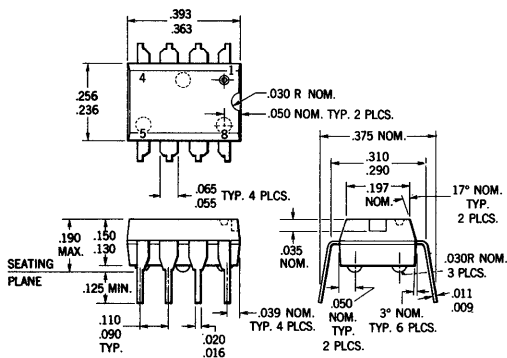
NOTES:
All dimensions in inches
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Copper slug

(BP)9J
Dual In-line Power Package (DIPP)
With Bracket Heat Sink



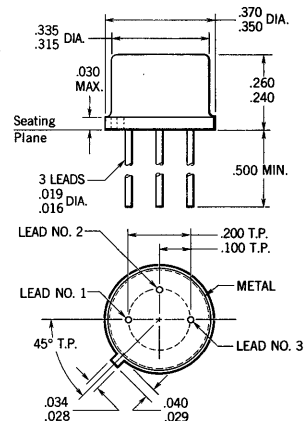
NOTES:
All dimensions in inches
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Copper slug and tin-plated copper bracket

(T)9T
8-Lead Molded Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Package weight is 0.6 gram
Leads are tin or gold-plate kovar

(H)CS
JEDEC (TO-39)

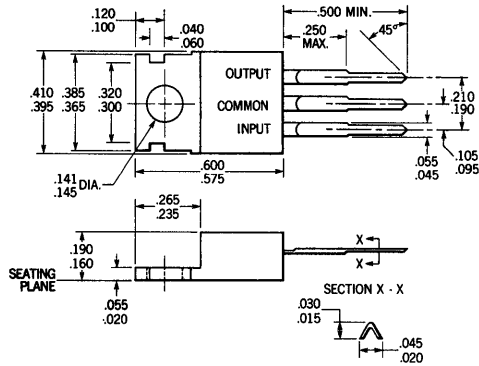


NOTES: All dimensions in inches
Leads are gold-plated over nickel-flash on steel
Lead No. 3 connected to case
Low thermal resistance
Package weight is 0.76 gram

PACKAGE OUTLINES

(U)GH

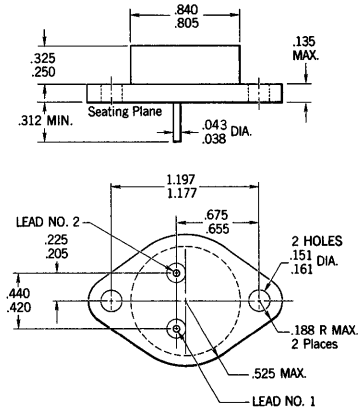
JEDEC (TO-220)
Molded Power Package



NOTES:
All dimensions in inches
Mounting tab is electrically connected to
COMMON
Package is molded with nickel plated copper
tab and leads
Package weight is 2.1 grams

(K)GJ

JEDEC (TO-3)



NOTES
All dimensions in inches
Leads 1 and 2 electrically isolated from case
Case is third electrical connection
(COMMON)
Leads are gold-plated copper cored kovar
Package weight is 7.4 grams

ORDER INFORMATION

A simplified ordering procedure for Fairchild linear integrated circuits is introduced with the publication of this catalog. Three basic units of information are contained in the new code.

<u>741</u>	<u>D</u>	<u>C</u>
Device Type	Package Type	Temperature Range

DEVICE TYPE

This group of alpha numeric characters defines the data sheet which specifies the device functional and electrical characteristics.

PACKAGE TYPE

One letter represents the basic package style.

D = Dual In-line Package (Hermetic)	K = Metal Power Package (TO-3 Outline)
F = Flatpak (Hermetic)	P = Dual In-line Package (Molded)
H = Metal Can Package	T = Mini DIP
J = Metal Power Package (TO-66 Outline)	U = Power Package (Molded, TO-220 Outline)

Different outlines exist within each package style to accommodate various die sizes and number of leads. Specific dimensions for each package can be found in the PACKAGE OUTLINES section of this catalog.

TEMPERATURE RANGE

Two basic temperature grades are in common use:

C = Commercial/Industrial/Consumer	M = Military
0°C to +70/75°C	-55°C to +125°C
-20°C to +85°C	-55°C to + 85°C
-40°C to +60°C	
-40°C to +85°C	

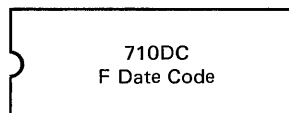
Exact values and conditions are indicated on the individual data sheets.

EXAMPLES

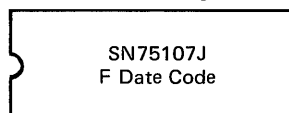
1. 710FM
This number code indicates a μ A710 Voltage Comparator in a flatpak with military temperature rating capability.
2. 725EHC
This number code indicates a μ A725 Instrumentation Operational Amplifier, electrical option E, in a metal can with a commercial temperature rating capability.

DEVICE IDENTIFICATION/MARKING

All Fairchild standard catalog linear circuits will be marked as the following example:



All second sourced items will be identified and marked with the original manufacturer's part number/order code:



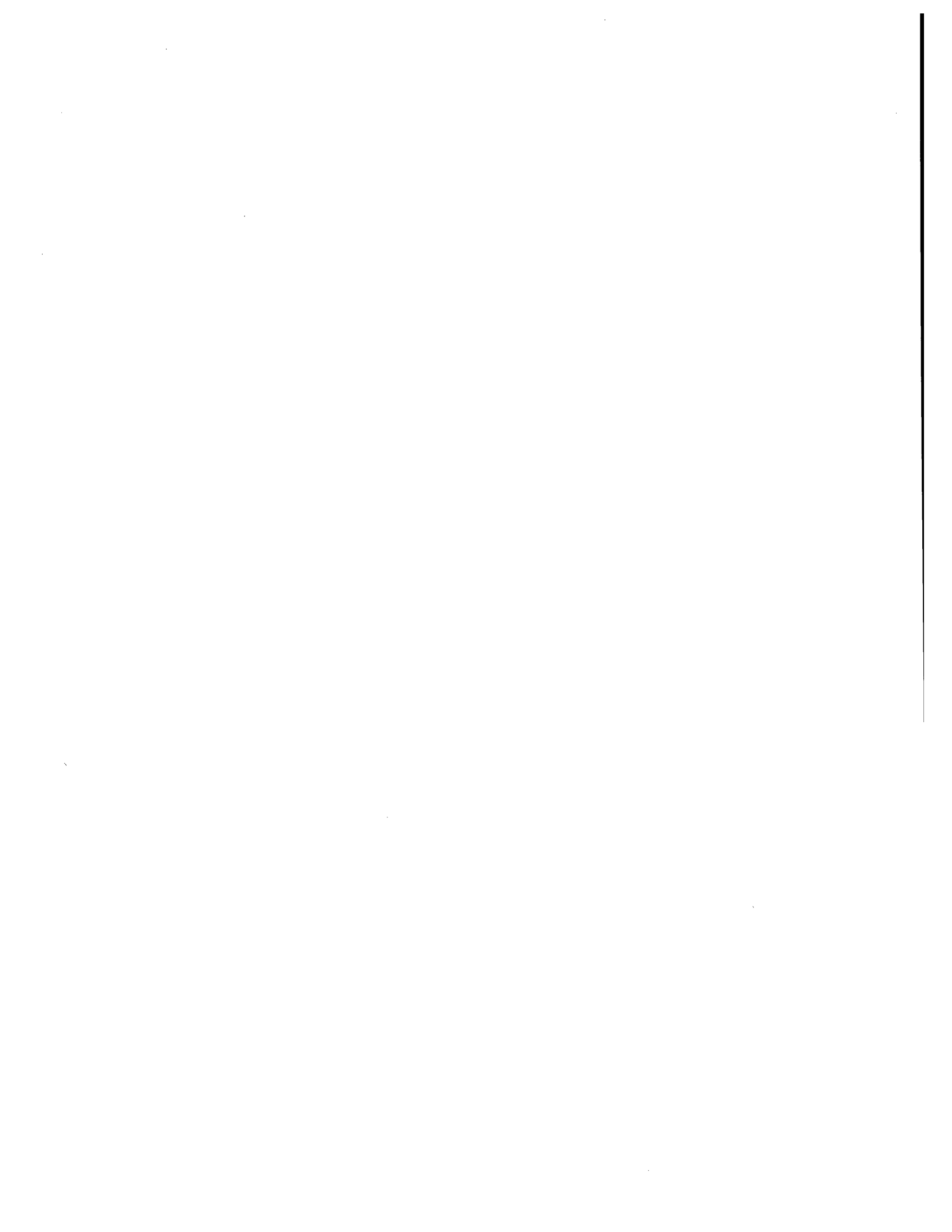
UNIQUE 38510 PROCESSING

Additional processing to Fairchild Unique 38510 specifications is indicated by noting the appropriate requirements (QB, QC) after the standard order code.

Detailed ordering procedures are provided in the OEM price list. (Also see page 11-1).

OLD ORDER CODES

Devices may continue to be purchased against old order codes (Example: U5R7723393; now 723HC). However, all products will be marked with new order codes unless otherwise specified.



MIL-M-38510/MIL-STD-883

Fairchild Analog Products has within it a unique "company" totally dedicated to the processing of Hi-Rel parts. This company is complete with marketing, production, engineering, production control and quality assurance functions designed specifically to serve the special needs of the Hi-Rel customer.

Our standard Hi-Rel process flow is MIL-M-38510. Fairchild maintains an inventory of MIL-M-38510 Class B processed parts.

Where an approved JAN slash specification exists (i.e. M38510/101) inventory is maintained for the JAN Class B part (i.e. JAN M38510/10101 BGC).

Where an approved slash specification does not exist product is processed per Fairchild's UNIQUE 38510 program Class B and inventoried. This UNIQUE 38510 inventory is available for processing to specific customer drawings or may be ordered directly from one of the standard processing options listed below.

UNIQUE 38510 CLASS CODES:

QB = MIL-M-38510 Class B Process Flow

QC = MIL-M-38510 Class C Process Flow

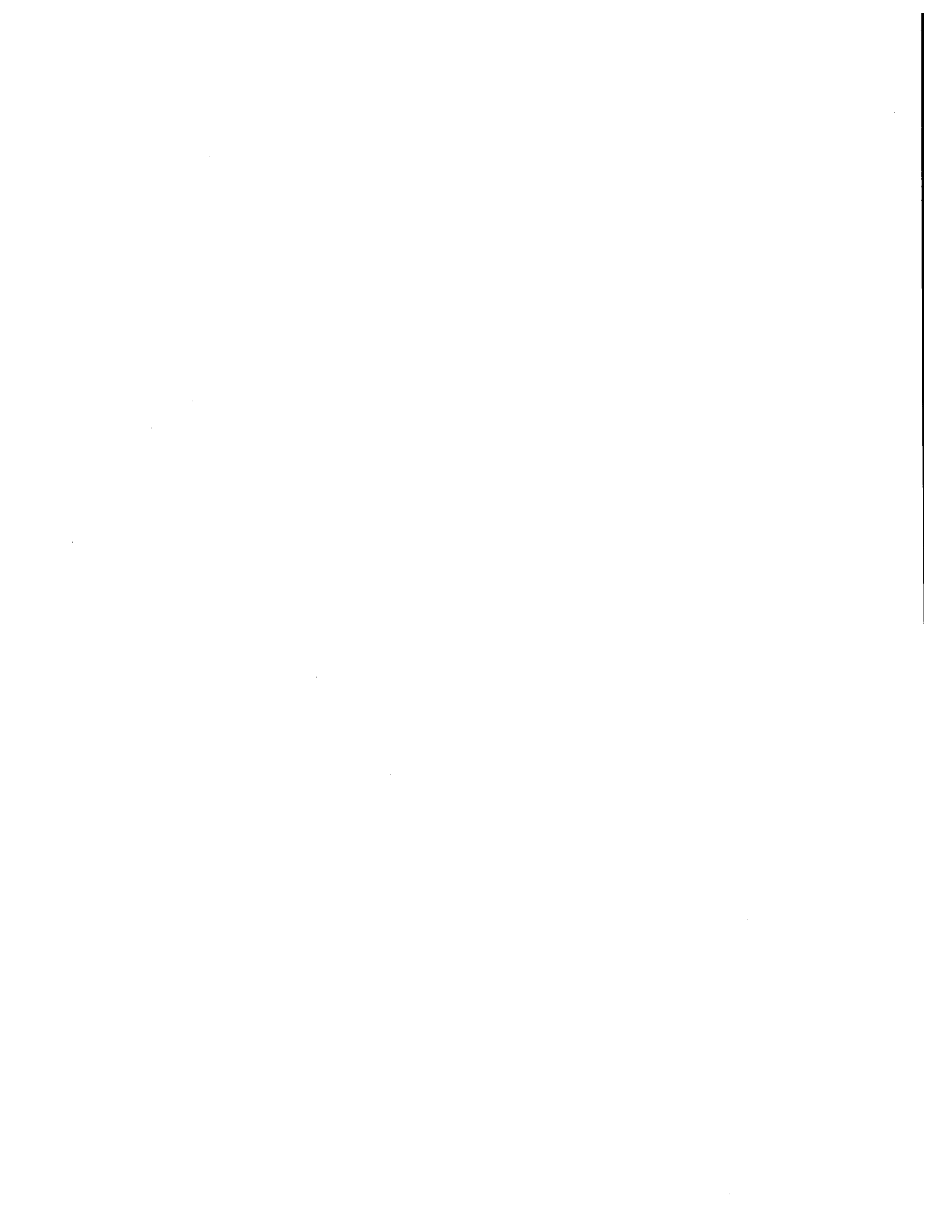
Number Options: These options apply to operations performed on each unit delivered:

- OPTION 1 Lead form to dimensions in detail specification, followed by hermetic seal tests.
- OPTION 2 Hot solder dip finish.
- OPTION 3 Read and record critical parameters before and after burn-in.
- OPTION 4 Initial qualification, Group B & C quality conformance not required.
- OPTION 5 Radiographic inspection shall be performed on all devices.
- OPTION 6 Special marking required.
- OPTION 7 Non-conforming variation - - refer to procurement documents for details (must be negotiated with factory.)

Letter Options: These options apply once per Purchase Order or line item and are considered Test Charges:

- OPTION A Group B testing shall be performed on customer's parts.
- OPTION B Group C testing shall be performed on customer's parts.
- OPTION C Generic data to be supplied from the latest completed lot.

The UNIQUE 38510 general specification and the detailed slash specifications are available upon request.



DICE POLICY

GENERAL INFORMATION

Fairchild linear integrated circuits, constructed using the Fairchild Planar* epitaxial process, are available in dice form incorporating these features:

- Commercial or Military Selection (Military Limits Probed at 25°C)
- MIL-STD-883, Method 2010.1, Condition B Visual
- Gold Backing
- Glass Passivation
- Protective Packaging

ELECTRICAL CHARACTERISTICS

Each die is electrically tested at 25°C to guaranteed commercial dc parameters.

Military grade die are similarly selected and defined as the 25°C dc military data sheet limits probed at 25°C.

QUALITY ASSURANCE

All Fairchild linear dice are 100% visually inspected and conform to MIL-STD-883, Method 2010.1, Condition B. In addition, quality control visually inspects the dice to a given sampling plan.

Each die is gold backed to aid die attach. For protection in handling and assembly, each die has a glass passivation coating with only the bonding pads exposed.

SHIPPING PACKAGES

Linear dice are packaged in containers with an anti-static sheet inserted between the lid and the dice. This sheet guards against electrostatic damage during shipment and storage.

The clear plastic carrier allows visual inspection of all the packaged dice. Each carrier is heat sealed within a transparent bag. A small piece of dehydrator paper with humidity indicating color is inserted in each bag prior to sealing.

ORDER INFORMATION

The minimum order quantity is in 25 piece multiples of value greater than \$250.00 per line item of commercial grade die. For ordering information and pricing on military grade die, contact your local Fairchild distributor or Fairchild sales office.

Each linear integrated circuit die has a unique order code which describes the device type, the dice designation and type of electrical tests performed. The dice designation is denoted by an "X" and is substituted for the package code. Examples follow:

Generic Type	Order Code
741C**	741XC
3045	CA3045X
75450	SN75450X
101A	LM101AX

**Some device types imply a military or commercial range by the generic type. Where this does not occur the suffix should be:

XM	Military Grade Die
or XC	Commercial Grade Die

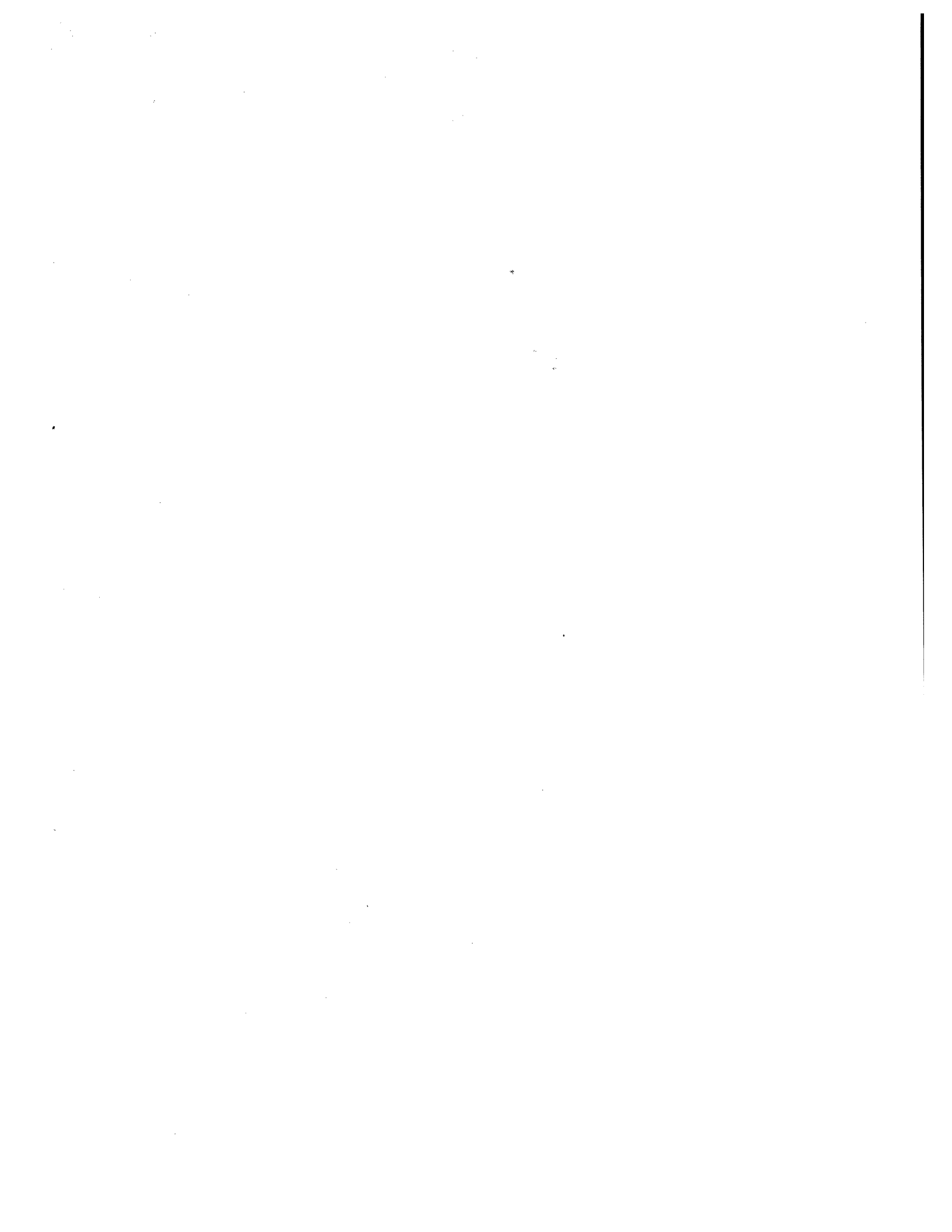
SPECIAL CHIP PROCESSING

If there is a need for additional testing or processing, Fairchild will negotiate with the customer to meet his requirements.

PRODUCT AVAILABLE IN DICE FORM

Please refer to FSC OEM Price List for product available in die form.

*Planar is a patented Fairchild process.



LINEAR
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LINEAR
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LINEAR
LINEAR
LINEAR

CONTENTS AND SECTION SELECTOR

INDUSTRY CROSS REFERENCE GUIDE 13

APPLICATION INFORMATION 14

LINEAR CROSS REFERENCE GUIDE

MOTOROLA

DEVICE ORDER NUMBER FORMAT



PACKAGE CROSS REFERENCE

PACKAGE	MOTOROLA	FAIRCHILD
Dual In-line HERMETIC	L	D
Dual In-line MOLDED	P	P
Flatpak	F	F
TO-5 Can	G,R	H

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE‡	MOTOROLA	FAIRCHILD
COMMERCIAL	13,14	C
MILITARY	15	M

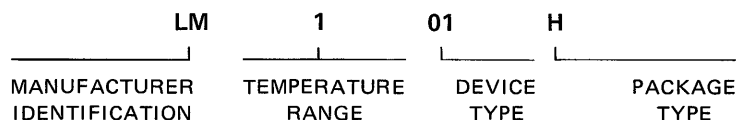
‡ See Order Information for values

MOTOROLA	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	MOTOROLA	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	MOTOROLA	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT
MC943	SH2001		MC1466		μA723C	MC1596	μA796	
MC1303		μA749C	MC1469		μA723C	MC1709	μA709	
MC1304	μA732C		MC1488		9616C	MC1710	μA710	
MC1305		μA732C	MC1489		9617C	MC1711	μA711	
MC1307	μA767C		MC1496	μA796C		MC1712	μA702	
MC1310		μA758C	MC1509		μA733	MC1723	μA723	
MC1326		μA746C	MC1510		μA733	MC1741	μA741	
MC1328		μA746C	MC1514		μA711	MC1748	μA748	
MC1339		μA749C	MC1519		μA733	MC75107A	75107A	
MC1350		μA757C	MC1520		101	MC75108A	75108A	
MC1351		3065	MC1525		μA730	MC75109	75109	
MC1352		μA757C	MC1526		μA730	MC75110	75110	
MC1353		μA757C	MC1529		μA730	MC75325	75325	
MC1355		3065	MC1530		μA702	MC55107A	55107A	
MC1357	2136		MC1531		μA702	MC55108A	55108A	
MC1358	3065		MC1533		101	MC55109	55109	
MC1364	3064		MC1535		μA749	MC55110	55110	
MC1370	μA780C		MC1536		μA741	MFC4060		μA723
MC1371	μA781C		MC1537		μA749	MFC6010		μA703
MC1410		μA733C	MC1539		101	MFC8000		μA739
MC1414		μA711C	MC1540		7525	MFC8001		μA739
MC1420		μA733C	MC1541		7524	MFC8002		μA739
MC1429		μA730C	MC1543		7524	MFC8030		μA703
MC1430		μA702C	MC1545		μA733	MFC8040		μA791
MC1431		μA702C	MC1546		μA733	MFC8070		μA742
MC1433		301	MC1550		μA757	MLM101A	101A	
MC1435		μA749C	MC1552		μA715	MLM105	105	
MC1436		301	MC1553		μA715	MLM107	107	
MC1437		μA749C	MC1556		μA725	MLM109	109	
MC1438		μA749C	MC1558	1558		MLM201	201	
MC1439		301	MC1560		μA723	MLM205	205	
MC1440		7525	MC1561		μA723	MLM207	207	
MC1441		7524	MC1563		μA723	MLM209	209	
MC1445		μA733C	MC1566		μA723	MLM301	301	
MC1446		μA733C	MC1569		μA723	MLM305	305	
MC1456		μA725C	MC1580		9615	MLM307	307	
MC1458	1458		MC1582		9614	MLM309	309	
MC1460		μA723C	MC1583		9615			
MC1461		μA723C	MC1584		9615			
MC1463		μA723C	MC1590		μA757			

* See specific data sheet for complete order part number.

NATIONAL

DEVICE ORDER NUMBER FORMAT



PACKAGE CROSS REFERENCE

PACKAGE	NATIONAL	FAIRCHILD
Dual In-line HERMETIC	D,J	D
Dual In-line MOLDED	N	T,P
Flatpak	F,W	F
TO-3 Can	K	K
TO-5 Can	H,G	H

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE‡	NATIONAL	FAIRCHILD
COMMERCIAL	3,2	C
MILITARY	1	M

‡ See Order Information for values

NATIONAL	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	NATIONAL	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	NATIONAL	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT
DM7820		9615	LM100		μA723	LM304	304	
DM7820A		9615	LM101	101		LM305	305	
DM7822		9617	LM101A	101A		LM306		μA710C
DM7830		9614	LM102	102		LM307	307	
DM7831		9614	LM104	104		LM308	308	
DM7832		9614	LM105	105		LM308A	308A	
DM8820		9615	LM106		μA760	LM309	309	
DM8820A		9615	LM107	107		LM310	310	
DM8822		9617	LM108	108		LM311	311	
DM8830		9614	LM108A	108A		LM312		μA776C
DM8831		9614	LM109	109		LM316		μA740C
DM8832		9614	LM110	110		LM316A		μA740C
LH0002	μA791	LM111	111			LM318		μA772C
LH0002C	μA791C	LM112			μA776	LM320-05		μA78N05
LH0020	μA725	LM118			μA772	LM340-05	μA7805C	
LH0020C	μA725C	LM119			μA760	LM340-06	μA7806C	
LH0021	μA791	LM120	μA78N00			LM340-08	μA7808C	
LH0021C	μA791C	LM121			μA727	LM340-12	μA7812C	
LH0041	μA791	LM160	μA760			LM340-15	μA7815C	
LH0041C	μA791C	LM161			μA760	LM340-18	μA7818C	
LH0042	μA740	LM200			μA723C	LM340-24	μA7824C	
LH0042C	μA740C	LM201	201			LM350	75325	
LH0052	μA740	LM202	202			LM376	376	
LH0052C	μA740C	LM204	204			LM709	μA709	
LH101	107	LM205	205			LM709A	μA709A	
LH201	207	LM206			μA710C	LM709C	μA709C	
LH2101A	101A	LM207	207			LM710	μA710	
LH2201A	201A	LM208	208			LM710C	μA710C	
LH2301A	301A	LM208A	208A			LM711	μA711	
LH2108	108	LM209	209			LM711C	μA711C	
LH2208	208	LM210	210			LM723	μA723	
LH2308	308	LM211	211			LM723C	μA723C	
LH2110	110	LM216			μA740	LM725	μA725	
LH2210	210	LM216A			μA740	LM725A	μA725A	
LH2310	310	LM218			μA772	LM725C	μA725C	
LH2111	111	LM219			μA760	LM733	μA733	
LH2211	211	LM219			μA760	LM733C	μA733C	
LH2311	311	LM300			μA723	LH740A	μA740	
LH24250	μA776	LM301A	301A			LH740AC	μA740C	
LH24250C	μA776C	LM302	302			LM741	μA741	

* See specific data sheet for complete order part number.

NATIONAL (Cont'd)

NATIONAL	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	NATIONAL	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	NATIONAL	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT
LM741C	μA741C		LM4250	μA776		LM7539		7524
LM747	μA747		LM4250C	μA776C		LM75325	75325	
LM747C	μA747C		LM7520		7524	LM75450A	75450A	
LM748	μA748		LM7521		7524	LM75451A	75451A	
LM748C	μA748C		LM7522		7524	LM75452	75452	
LM1488		9616	LM7523		7524	LM75453	75453	
LM1489		9617	LM7524	7524		LM75454	75454	
LM1489A		9617	LM7525	7525		LMDAC-01		μA722
LM1414		μA711C	LM7528	7528		NH00011	SH2001	
LM1458	1458		LM7529	7529		NH00011CN	SH2002	
LM1514		μA711	LM7534	7534		NH00013	SH0013	
LM1558	1558		LM7535	7535	7524	NH00016	SH2200	
			LM7538		7524	NH00017	SH2200	
						NH00018	SH2200	

RCA

PACKAGE CROSS REFERENCE

PACKAGE	RCA	FAIRCHILD
Dual In-line HERMETIC	D	D
Dual In-line MOLDED	E	P
TO-5 Can MOLDED	T	H
DICE	H	X

DEVICE ORDER NUMBER FORMAT

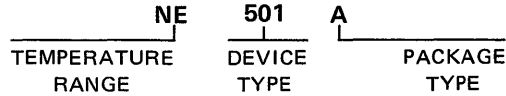
CA 3045	
MANUFACTURER IDENTIFICATION	DEVICE TYPE

RCA	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	RCA	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	RCA	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT
CA3000		μA702	CA3033		μA709	CA3067	3067	
CA3001		μA733	CA3033A		μA709	CA3070	μA780	
CA3002		μA703	CA3035		μA739	CA3071	μA781	
CA3004		μA703	CA3036	3036		CA3072	μA746	
CA3005		μA703	CA3037		μA709	CA3075	3075	
CA3006		μA703	CA3037A		μA709	CA3076	3076	
CA3007		μA716	CA3038		μA709	CA3078		μA776
CA3008		μA702	CA3038A		μA709	CA3079		μA742
CA3008A		μA702	CA3039	3039		CA3085		μA723
CA3010		μA702	CA3040		μA733	CA3085A		μA723
CA3010A		μA702	CA3041		3065	CA3085B		μA723
CA3011		μA753	CA3042		3065	CA3086	3086	
CA3012		μA753	CA3043		3065	CA3088		μA720
CA3013		μA753	CA3044	3064		CA3089		3075
CA3014		μA753	CA3045	3045		CA3090		μA758
CA3015		μA702	CA3046	3046		CA3091		μA795
CA3015A		μA702	CA3047		μA709	CA3118		3018
CA3016		μA702	CA3048		μA749	CA3118A		3018
CA3016A		μA702	CA3048H		μA749	CA3146		3046
CA3018	3018		CA3050		μA730	CA3146A		3046
CA3018A	3018A		CA3051		μA730	CA3458	1458	
CA3019	3019		CA3052		μA739	CA3541		7524
CA3021		μA757	CA3053		μA703	CA3558	1558	
CA3022		μA757	CA3054	3054		CA3741C	μA741C	
CA3023		μA757	CA3058		μA742	CA3741	μA741	
CA3026	3026		CA3059		μA742	CA3747C	μA747C	
CA3028		μA703	CA3060A		μA739	CA3747	μA747	
CA3028A		μA703	CA3060B		μA739	CA3748C	μA748C	
CA3029		μA702	CA3060		μA739	CA3748	μA748	
CA3029A		μA702	CA3064	3064		CA6741	μA741	
CA3030		μA702	CA3065	3065				
CA3030A		μA702	CA3066	3066				

* See specific data sheet for complete order part number.

SIGNETICS

DEVICE ORDER NUMBER FORMAT



PACKAGE CROSS REFERENCE

PACKAGE	SIGNETICS	FAIRCHILD
Dual In-line HERMETIC	F,I	D
Dual In-line MOLDED	A,B	P
Mini DIP	V	T
Flatpak	W,Q	F
TO-3 Can	DA	K
TO-5 Can	DB,K,T	H

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE‡	SIGNETICS	FAIRCHILD
COMMERCIAL	NE,N	C
MILITARY	SE,S	M

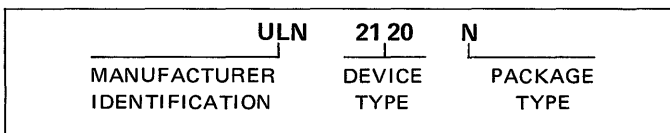
‡ See Order Information for values

SIGNETICS	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	SIGNETICS	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	SIGNETICS	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT
501		μA733	μA711	μA711		75451		75451A
510		μA730	μA723	μA723		75451A	75451A	
511		3045	μA733	μA733		LM101	101	
515		μA730	μA740	μA740		LM107	107	
516		μA740	μA741	μA741		LM108	108	
518		μA711	μA747	μA747		LM109	109	
526		μA710	μA748	μA748		LM201	201	
527		μA760	5556		μA776	LM207	207	
528		7524	5558	1458		LM209	209	
529		μA760	7520		7524	LM301	301	
531		μA715	7521		7524	LM307	307	
533		μA776	7522		7524	LM308	308	
536		μA740	7523		7524	LM309	309	
537		μA725	7524	7524		8T13	8T13	
550		μA723	7525	7525		8T14	8T14	
592		μA733	75450		75450A	8T23	8T23	
μA709	μA709		75450A	75450A		8T24	8T24	
μA710	μA710							

* See specific data sheet for complete order part number.

SPRAGUE

DEVICE ORDER NUMBER FORMAT



PACKAGE CROSS REFERENCE

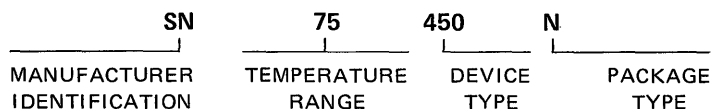
PACKAGE	SPRAGUE	FAIRCHILD
Dual In-Line MOLDED	A,N	P
TO-5 Can	K,W	H

SPRAGUE	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	SPRAGUE	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	SPRAGUE	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT
ULN2111	2136		ULN2124	μA780		ULN2136	2136	
ULN2113		3065	ULN2126	μA739		ULN2165	3065	
ULN2114	μA746		ULN2127	μA781		ULX2205		μA706
ULN2120	μA732		ULN2128	μA767		ULX2211		μA704
ULN2121		μA767	ULN2129		3075	ULX2275		μA705
ULN2122		μA732	ULN2131	μA753		ULX2277	μA705	

*See specific data sheet for complete order part number.

TEXAS INSTRUMENTS

DEVICE ORDER NUMBER FORMAT



PACKAGE CROSS REFERENCE

PACKAGE	T.I.	FAIRCHILD
Dual In-line HERMETIC	J	D
Dual In-line MOLDED	N	P
Mini DIP	P	T
Flatpak	H,U,Z,W	F
TO-5 Can	L	H

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE‡	T.I.	FAIRCHILD
COMMERCIAL	75,72	C
MILITARY	55,52	M

‡ See Order Information for values.

T.I.	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	T.I.	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT	T.I.	*FAIRCHILD DIRECT REPLACEMENT	*FAIRCHILD FUNCTIONAL EQUIVALENT
SN52101A	101A	μA710	SN72810		μA710C			
SN52107	107		SN72811		μA711C	SN75454	75454	
SN52510		μA710	SN72820		μA734C	SN75460	75460	
SN52558	1558		SN7510		μA733C	SN75461	75461	
SN52702	μA702		SN7511		μA733C	SN75462	75462	
SN52709	μA709		SN7512		μA733C	SN75463	75463	
SN52709A	μA709A		SN7514		μA733C	SN75464	75464	
SN52710	μA710		SN7520		7524	SN76001		μA706C
SN52711	μA711		SN7521		7524	SN76003		μA706C
SN52720		μA711	SN7522		7524	SN76005		μA706C
SN52733	μA733		SN7523		7524	SN76010		μA706C
SN52741	μA741		SN7524	7524		SN76013		μA706C
SN52747	μA747		SN7525	7525		SN76050		μA706C
SN52748	μA748		SN7526		7524	SN76104	μA732C	
SN52770		μA740	SN7527		7524	SN76105		μA732C
SN52771		μA740	SN7528		7524	SN76107	μA767C	
SN52810		μA710	SN7529		7524	SN76110	μA767C	
SN52811		μA711	SN75100L		9615	SN76131	μA739C	
SN52820		μA734	SN75107A	75107A		SN76149	μA749C	
SN5510		μA733	SN75108A	75108A		SN76177	μA705C	
SN5511		μA733	SN75109	75109		SN76242	μA780C	
SN5512		μA733	SN75110	75110		SN76243	μA781C	
SN5514		μA733	SN75114	9614C		SN76246	μA746C	
SN55107A	55107A		SN75115	9615C		SN76266	3066	
SN55108A	55108A		SN75150		9616C	SN76267	3067	
SN55109	55109		SN75152	9627C		SN76350		μA720C
SN55110	55110		SN75154		9617C	SN76550		μA723C
SN70024		μA706C	SN75182		9615	SN76552		μA723C
SN72301A	301		SN75183		9614	SN76553		μA723C
SN72307	307		SN75232	7534		SN76564	3064	
SN72400		μA723C	SN75233	7525		SN76603	μA703C	
SN72510		μA710C	SN75234	75234		SN76619		μA703C
SN72558	1458		SN75235	75235		SN76630	μA786C	
SN72702	μA702C		SN75238		7524	SN76640		3065
SN72709	μA709C		SN75239		7524	SN76642		3075
SN72710	μA710C		SN75324		75325	SN76643	2136	
SN72711	μA711C		SN75325	75325		SN76660		3065
SN72720		μA711C	SN75326		75325	SN76665	3065	
SN72733	μA733C		SN75327		75325	SN76666	3066	
SN72741	μA747C		SN75450		75450A	SN76670		3065
SN72748	μA748C		SN75451		75451A	SN76675	3075	
SN72770		μA740C	SN75452	75452		SN76676	3076	
SN72771		μA740C	SN75453	75453		SN76680		3065

* See specific data sheet for complete order part number

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CONTENTS AND SECTION SELECTOR

APPLICATION INFORMATION

14

The following is a list of currently available linear integrated circuits application notes. For your convenience, they are organized by application note number, product number and function. For application notes and the most recent Fairchild Semiconductor Application Literature Index write to:

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LINEAR INTEGRATED CIRCUITS APPLICATION NOTE INDEX BY NUMBER

APP-116	The Operation and Use of a Fast Integrated Circuit Comparator, 1966	APP-270	A Trapezoidal Deflection Circuit for Use with the 3250 Numeric Character Generator Using the $\mu A715$, 1969
117/2	Frequency Compensation Techniques for an Integrated Operational Amplifier, 1966	271	A High Speed Sample and Hold Using the $\mu A715$, 1969
123	Core Memory Sense Amplifier Designs Using an Integrated Circuit, 1966	276	More Voltage Regulator Applications Using the $\mu A723$, 1969
125	A Versatile Tester for Linear Integrated Circuits, 1966	277	A Low Drift, Low Noise Monolithic Operational Amplifier for Low Level Signal Processing, 1969
171	Applications of the $\mu A739$ and $\mu A749$ Dual Preamplifier Integrated Circuits in Home Entertainment Equipment, 1969	281	A Minimum Component $\mu A749$ Voltage-to-Frequency Converter with 1% Accuracy, 1970
175	The $\mu A739$, A Low Noise Dual Operational Amplifier, 1969	283	Even More Voltage Regulator Applications Using the $\mu A723$ - Number 2, 1970
186	Marker Beacon Receiver and Display, 1970	286	The $\mu A729$, $\mu A732$ and $\mu A767$ Integrated Circuit Stereo Multiplex Decoders, 1970
195	Radiation Testing of Linear Microcircuits, 1966	289	Applications of the $\mu A741$ Operational Amplifier, 1970
196	Space and Nuclear Environments and their Effects on Semiconductors, 1967	293	A Low Level Wideband Video Amplifier, 1971
203	A Comparison of Solid State Subcarrier Oscillators for Color TV Receivers, 1970	297	An Improved Sample and Hold Circuit Using the $\mu A740$, 1970
204	An Integrated Circuit AGC IF Amplifier, 1970	299	Proposed Integrated Circuit for Appliance or Process Control, 1969
205	Thermal Evaluation of Integrated Circuits, 1970	300	Applications of the $\mu A777$ 1971
208	A Monolithic Zero Crossing AC Trigger (TRIGAC) for Thyristor Power Controls, 1971	301	The Power Amplifier Using the $\mu A777$, 1971
210	Integrated TV Chroma Processing System, 1971	311	$\mu A760$, A High Speed Monolithic Comparator, 1971
218	The $\mu A776$, An Operational Amplifier with Programmable Gain, Bandwidth, Slew Rate, and Power Dissipation, 1971	312	The $\mu A7800$ Series Three Terminal Positive Voltage Regulators, 1971
225	Gated Pulse Rate Function Multiplier, 1967	315	The $\mu A750$ Dual High Current Comparator and Some of its Applications, 1972
229	Analog-to-Pulse Width Converter, 1968	317	A High Output Power (5 W), Low Distortion IC Audio Amplifier, 1972
243	Some Useful Signal Processing Circuits Using FETs and Operational Amplifiers, 1968	318	Integrated Circuits for FM Receivers, 1972
254	Black Level Considerations in High Quality TV Receivers, 1969	319	The $\mu A758$, Phase Locked Loop Stereo Multiplex Decoder, 1972
261	A High Speed, Zero Input Current Chopper Amplifier, 1969	320	$\mu A9616/9617$ EIA Interface Driver and Receiver, 1972
265	The $\mu A715$ - A Versatile High Speed Operational Amplifier, 1969	321	Operational Amplifiers as Inductors, 1972
267	The $\mu A746E$ Color TV Chroma Demodulator IC, 1969	323	Voltage Comparator Applications Using the $\mu A734$, 1972
268	Applications of the $\mu A749$ Dual Operational Amplifier, 1969	324	Applications of the 9650 4-Bit, High Speed, Precision Current Source, 1972
269	The $\mu A749$ Dual Operational Amplifier, 1969		

LINEAR INTEGRATED CIRCUITS APPLICATION NOTE INDEX BY FUNCTION

FUNCTIONAL CATEGORY	APPLICATION NOTES	FUNCTIONAL CATEGORY	APPLICATION NOTES
Amplifiers		Discriminators, Frequency	186, 318
AGC	204, 243	Displays, Numeric	270
Audio	171, 175, 301, 317	Division, Frequency	323
Chopper	261	Filters, Analog	
Comparator	116, 123, 268, 289	Active	243, 321
Compensation	117/2, 300	Band Pass	243
DC	269	Tunable	243
Differential	300	Generators	
Dual	268, 269	Clock	163
High Speed	265	Numeric Character	270
High Input Impedance	265	Instrumentation	
IF	112, 256, 318	Digital	324
Integrating	289	Indicator	
Low Noise	175, 277	Analog Status	315
Operational	117/2, 218, 265, 268, 269, 270, 277, 297, 300, 321	Malfunction	315
Power	116, 289, 301	Phase Meter	315, 323
Power-Audio	258, 259, 317	Line Drivers	320
Preamp	123, 171, 175, 243	Line Receivers	116, 311, 320
Sample and Hold	271, 297	Multivibrators, Monostable	116
Sense	123	Noise	
Video	265, 293	Immunity	116
Wideband	265, 293	Low Noise Techniques	229
Communication Systems		Measurement	229
FM Radio	318, 319	Oscillators	
Pulse Modulation	229, 320, 323	Audio	300
Data Transmission	320	Crystal Controlled	145
Comparators	116, 123, 311, 315, 323	Pulse	323
Compressors	243	Sinusoidal	230, 300
Controls	208	Subcarrier	203
Process	299	Voltage Controlled	323, 281
Remote	171	Wien Bridge	300
Converters		Parameter Measurement	195, 196
Analog to Digital	311, 324	Power Supplies, Regulators	116, 276, 283, 312
Analog to Pulse	229	Radiation Effects on	
Digital to Analog	324	Semiconductors	195, 196
Voltage to Frequency	281	Television — See also	
Data		Communication Systems	
Acquisition & Reduction	297	Color Signal Processing	210, 267
Systems		Section	
Transmission	320, 116, 311	Video Amplifier Section	254, 293
Decoders, Multiplex	286, 318, 319	Testers — See also	
Demodulators		Instrumentation	
FM	318	Linear	125
Pulse	172, 311, 323	Testing	205
Detectors		Transducer — See also Controls	229
Level	116, 311	Voltage Regulators	276, 283, 312
Minimum Frequency	315		
Peak, Peak to Peak	311		
Zero Crossing	208, 311		

LINEAR INTEGRATED CIRCUITS APPLICATION NOTE INDEX BY PRODUCT NUMBER

LINEAR INTEGRATED CIRCUITS APPLICATION NOTES

702	117/2, 125, 195
703	203
706	317, 318
709	125, 195, 229
710	116, 125, 195, 225
711	116, 123, 125
715	261, 265, 270
723	276, 283
725	277
727	290
734	323
739	171, 175, 186
740	297
741	186, 243, 289
742	208, 299
746	254, 267
747	210
749	171, 268, 269, 281
750	315
753	318
757	204
758	318, 319
760	311
776	218
777	300, 301, 321
780	210
781	210
3075	318
7800	312
9616	320
7617	320
9650	324

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